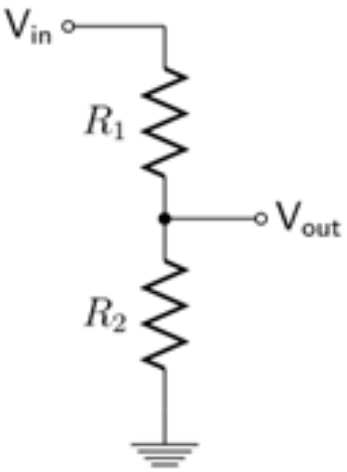
MCP-3204		
Clock at 5V	2	MHz
Clock Cycle (5V)	0.0000005	s
Sampling Time	1.5	Clock Cycles
Sampling Time	0.00000075	S
Sample Capacitor	20	pF
Internal Switch Resistance	1000	Ohm

	Typical RC Circuit Timing		
Resistance	Capacitor	Time Constant (T)	Charging Time
×	Ë	S	5T
100	2E-11	0.000000002	0.00000001
200	2E-11	0.000000004	0.00000002
400	2E-11	0.000000008	0.00000004
800	2E-11	0.000000016	0.00000008
1600	2E-11	0.000000032	0.00000016
3200	2E-11	0.000000064	0.00000032
6400	2E-11	0.000000128	0.00000064
12800	2E-11	0.000000256	0.00000128
25600	2E-11	0.000000512	0.00000256
51200	2E-11	0.000001024	0.00000512
102400	2E-11	0.000002048	0.00001024
204800	2E-11	0.000004096	0.00002048
409600	2E-11	0.000008192	0.00004096

Voltage Divider



From the Data Sheet (Page 17, bottom left)

For the A/D converter to meet specification, the charge holding capacitor (CSAMPLE) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

This diagram illustrates that the source impedance (RS) adds to the internal sampling switch (RSS) impedance, directly effecting the time that is required to charge the capacitor (CSAMPLE). Consequently, larger source impedances increase the offset, gain and integral linearity errors of the conversion (see Figure 4-2).

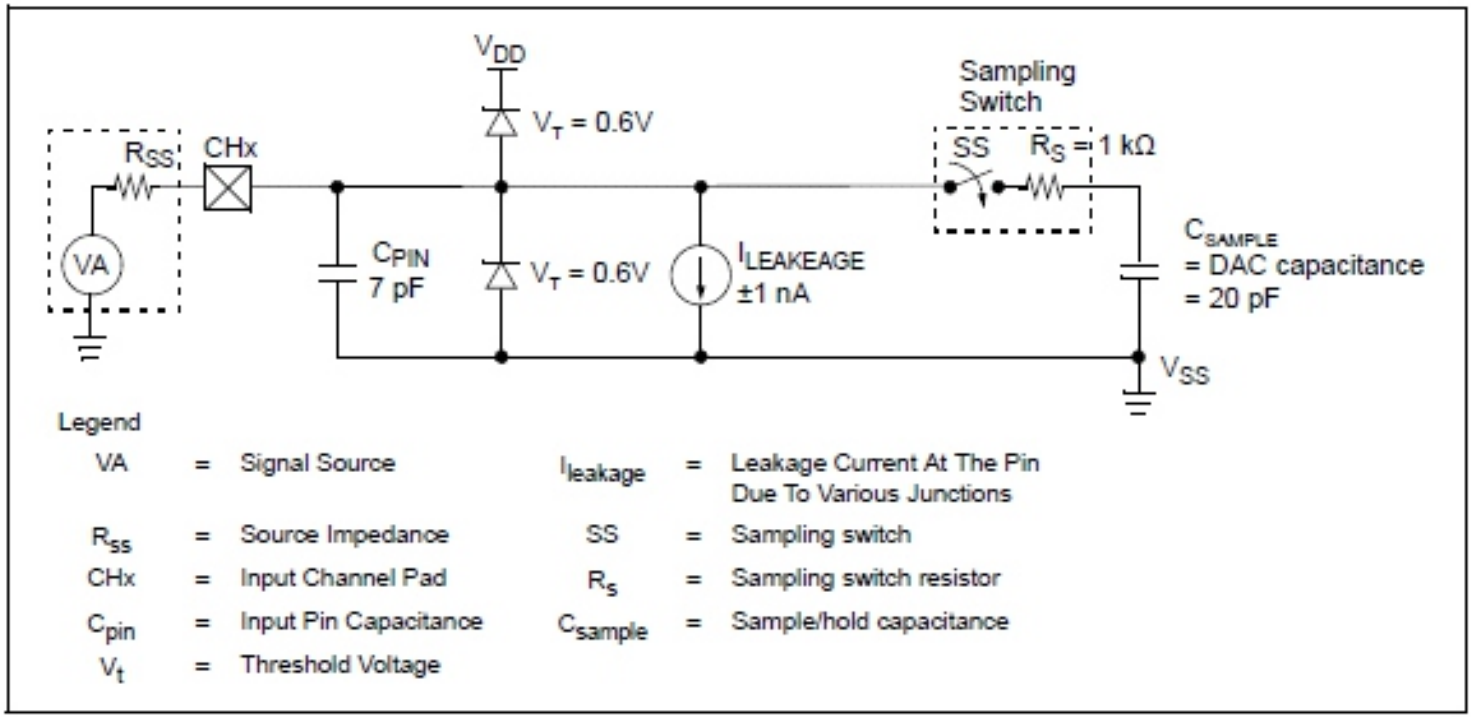


FIGURE 4-1: Analog Input Model.

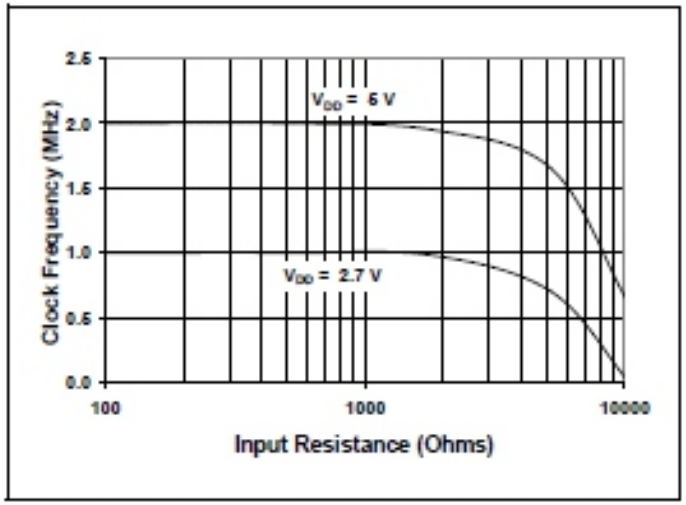


FIGURE 4-2: Maximum Clock Frequency vs. Input resistance (R_S) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.