

# Franklin Lightning Sensor Module

Figure 2: AS3935 functional block diagram. The diagram illustrates the internal architecture of the AS3935 chip, showing the flow of data and control signals between various functional blocks. Key components include the Register, POR (Power-On Reset), AFE (Analog Front End), LC Oscillator, Calibration, TRCO and SRCO (Clock Generators), Bit Block, and the core processing blocks: Noise Floor Level Generation, Noise Floor Evaluation, Signal Validation, Energy Calculation, Statistical Distance Estimation, and Lightning Algorithms. The chip is connected to a GND pin and a TEST pin. The diagram is labeled 'AS3935 機能ブロック図'.

Absolute Maximum Ratings 絶対最大定格

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	DC supply voltage	-0.5	7	V	
VIN	Input pin voltage	-0.5	5	V	
Iscr	Input current (latch up immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
Continuous Power Dissipation					
Pt	Total power dissipation (all supplies and outputs)		0.1	mW	
Temperature Ranges and Storage Conditions					
Tstrg	Storage temperature	-65	150	°C	
Tbody	Package body temperature		260	°C	Norm: IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".
	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

Figure 5:

Operating Conditions 動作条件

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Positive supply voltage	In case the voltage regulator is ON	2.4		5.5	V
		In case the voltage regulator is OFF	2.4		3.6	V
TAMB	Ambient temperature		-40		85	°C

Figure 6:

CMOS Input CMOS 入力仕様

Symbol	Parameter	Min	Typ	Max	Units
VIH	High level input voltage	0.6*VDD	0.7*VDD	0.9*VDD	V
VIL	Low level input voltage	0.125*VDD	0.2*VDD	0.3*VDD	V

Note: On ALL outputs, use the cells with the smallest drive capability which will do the job, in order to prevent current/spikes problems.

CMOS Output CMOS 出力仕様

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOH	High level output voltage	With a load current of 1mA	VDD-0.4			V
VOL	Low level output voltage				VSS+0.4	V
CL	Capacitive load	For a clock frequency of 1MHz			400	pF

Figure 8:

Tristate CMOS Output 3 ステート CMOS 出力仕様

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOH	High level output voltage	With a load current of 1mA	VDD-0.4			V
VOL	Low level output voltage				VSS+0.4	V
IOZ	Tristate leakage current	To VDD and VSS			400	nA

Figure 9:

Register Table レジスタテーブル

Register #	7	6	5	4	3	2	1	0
0x00	Reserved		AFE_GB					PWD
0x01	Reserved	NF_LEV			WDTH			
0x02	Reserved	CL_STAT	MIN_NUM_LIGH		SREJ			
0x03	LCO_FDIV		MASK_DIST	Reserved	INT			
0x04	S_LIG_L							
0x05	S_LIG_M							
0x06	Reserved			S_LIG_MM				
0x07	Reserved		DISTANCE					
0x08	DISP_LCO	DISP_SRCO	DISP_TRCO	Reserved	TUN_CAP			
0x3A	TRCO_CALIB_DONE	TRCO_CALIB_NOK	Reserved					
0x3B	SRCO_CALIB_DONE	SRCO_CALIB_NOK	Reserved					

詳細な資料は秋月電子通商の商品ページ  
http://akizukidenshi.com/catalog/g/gK-08685/ にございます。  
なお、本資料内の Figure xx: は ams Datasheet, Confidential: 2014-Jan[1-03] の  
図番号を示しています。

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Electrical System Specifications 電気の仕様

Symbol	Parameter	Min	Typ	Max	Units	Note
Input Characteristic						
RIN	Input AC impedance		200		kΩ	
Current Consumption						
IPWDROFF	Power-down current when VREG is OFF		1	2	μA	
IPWDRON	Power-down current when VREG is ON		8	15	μA	
ILSMROFF	Current consumption in listening mode when VREG is OFF		60	80	μA	
ILSMRON	Current consumption in listening mode when VREG is ON		70		μA	
ISVM	Current Consumption in signal verification mode		350		μA	
Timing						
Tlightning	Duration in signal verification mode once lightning is detected		1		s	
Tdisturber	Duration in signal verification mode once disturber is detected		1.5		s	
Oscillators						
LCOsUT	LCO Start-up Time			2	ms	Time needed by the LCO to start-up
TSRCO	SRCO frequency after calibration	1.065	1.125	1.19	MHz	Assuming FLCO = 500 kHz
TRCO	TRCO frequency after calibration	30.5	32.26	34.0	kHz	
TRCOCAL	Calibration time for the RC oscillators			2	ms	The calibration of the RC oscillators starts after the LCO settles
Voltage Regulator						
VROUT	Voltage regulator output voltage	2.7	3.0	3.3	V	

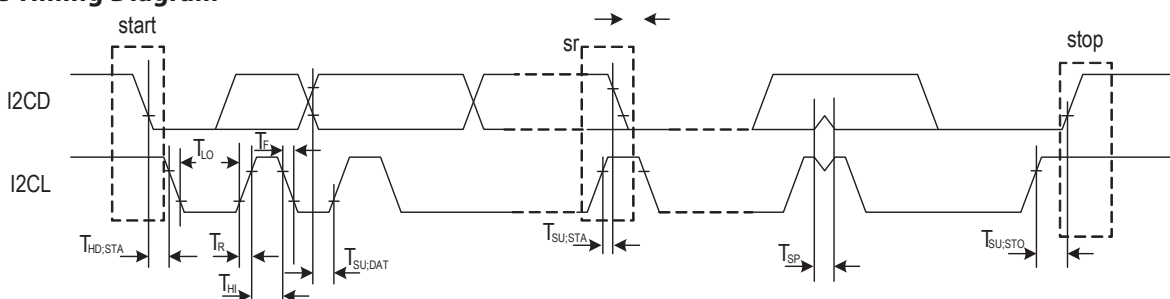
Figure 10:

Detailed Register Map レジスタ詳細マップ

Figure 23:

Address	Register Name	Bit	Type	Default Value	Description
0x00	Reserved	[7:6]		0	Reserved
	AFE_GB	[5:1]	R/W	10010	AFE Gain Boost
	PWD	[0]		0	Power-down
0x01	NF_LEV	[6:4]	R/W	010	Noise Floor Level
	WDTH	[3:0]		0010	Watchdog threshold
0x02	Reserved	[7]	R/W	1	Reserved
	CL_STAT	[6]		1	Clear statistics
	MIN_NUM_LIGH	[5:4]		00	Minimum number of lightning
	SREJ	[3:0]		0010	Spike rejection
0x03	LCO_FDIV	[7:6]	R/W	00	Frequency division ration for antenna tuning
	MASK_DIST	[5]		0	Mask Disturber
	Reserved	[4]		0	Reserved
	INT	[3:0]		0000	Interrupt (see Figure 43)
0x04	S_LIG_L	[7:0]	R	00000000	Energy of the Single Lightning LSBYTE
0x05	S_LIG_M	[7:0]	R	00000000	Energy of the Single Lightning MSBYTE
0x06	Reserved	[7:5]			Reserved
	S_LIG_MM	[4:0]	R	00000	Energy of the Single Lightning MMSBYTE
0x07	Reserved	[7:6]			Reserved
	DISTANCE	[5:0]	R	000000	Distance estimation
0x08	DISP_LCO	[7]	R/W	0	Display LCO on IRQ pin
	DISP_SRCO	[6]		0	Display SRCO on IRQ pin
	DISP_TRCO	[5]		0	Display TRCO on IRQ pin
	TUN_CAP	[3:0]		0000	Internal Tuning Capacitors (from 0 to 120pF in steps of 8pF)
0x3A	TRCO_CALIB_DONE	[7]	R	0	Calibration of TRCO done (1=successful)
	TRCO_CALIB_NOK	[6]	R	0	Calibration of TRCO unsuccessful (1=not successful)
	Reserved	[5:0]	R	000000	Reserved
0x3B	SRCO_CALIB_DONE	[7]	R	0	Calibration of SRCO done (1=successful)
	SRCO_CALIB_NOK	[6]	R	0	Calibration of SRCO unsuccessful (1=not successful)
	Reserved	[5:0]	R	000000	Reserved

Figure 31:



## I<sup>2</sup>C Parameters I<sup>2</sup>C パラメータ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TSP	Spike intensity		50	100		ns
THI	High Clock Time	400 kHz Clock speed	330			ns
TLO	Low Clock Time		660			ns
TSU		I2CD has to change Tsetup before rising edge I2CL	30			ns
THD		No hold time needed for I2CD relative to rising edge of I2CL	-40			ns
THD:STA	Within start condition, after low going I2CD, I2CL has to stay constant for specified hold time		300			ns
TSU:STO	After high going edge of I2CL, I2CD has to stay constant for the specified setup time before STOP or repeated start condition is applied		100			ns
TSU:STA			100			ns

Figure 32:

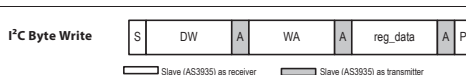


Figure 33:

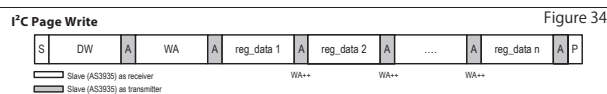


Figure 34:

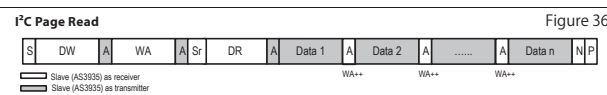


Figure 36:

I<sup>2</sup>C Abbreviations I<sup>2</sup>C 関連の略語と意味

Figure 35:

Symbol	Description
S	START condition after STOP
Sr	Repeated START
DW	Device Address for write
DR	Device Address for read
WA	Word address
A	Acknowledge
N	No acknowledge
P	STOP condition
WA++	Internal address increment

## Registers 0x3C, 0x3D 直接コマンド

Figure 37:

Direct Command	Register
PRESET_DEFAULT	0x3C
CALIB_RCO	0x3D

**Interrupts**    インターラプト

Figure 43:

Interrupt Name	REG0x03[3:0]	Description
INT_NH	0001	Noise level too high
INT_D	0100	Disturber detected
INT_L	1000	Lightning interrupt

## Settings for the Noise Floor Threshold ノイズフロア閾値の設定

Figure 40:

Continuous Input Noise Level [μVrms] (Outdoor)	Continuous Input Noise Level [μVrms] (Indoor)	REG0x01[6]	REG0x01[5]	REG0x01[4]
390	28	0	0	0
630	45	0	0	1
<b>860</b>	62	0	1	0
1100	78	0	1	1
1140	95	1	0	0
1570	112	1	0	1
1800	130	1	1	0
2000	146	1	1	1

## Distance Estimation 距離算定結果

Figure 42:

REG0x07[5:0]	Distance [km]
111111	Out of range
101000	40
100101	37
100010	34
011111	31
011011	27
011000	24
010100	20
010001	17
001110	14
001100	12
001010	10
001000	8
000110	6
000101	5
000001	Storm is Overhead

## Minimum Number of Lightning Detection 雷検出の最低数

Figure 44:

Minimum Number of Lightning	REG0x02[5]	REG0x02[4]
1	0	0
5	0	1
9	1	0
16	1	1

## AFE Setting, Outdoor vs. Indoor 屋外と屋内の AFE 設定

Figure 38:

AFE Setting	REG0x00[5:1]
Indoor	10010
Outdoor	01110

## Analog Front-end (AFE) and Watchdog アナログフロントエンドとウォッチドッグ

The AFE amplifies and demodulates the AC-signal picked up by the antenna. The AS3935 is based on narrowband receiving techniques with a center frequency of 500 kHz and a bandwidth of about 33 kHz. The AFE gain can be considered as constant within the antenna's bandwidth. This is achieved by making the AFE bandwidth greater than the antenna bandwidth.

The AFE gain has been optimized for two operating environments as shown in Figure 38. By default the gain is set to Indoor. It is of paramount importance that the gain is set according to the surrounding environment, otherwise the sensor will not yield the desired results.

Frequency Division Ratio for the Antenna Tuning アンテナチューニングの周波数分割比

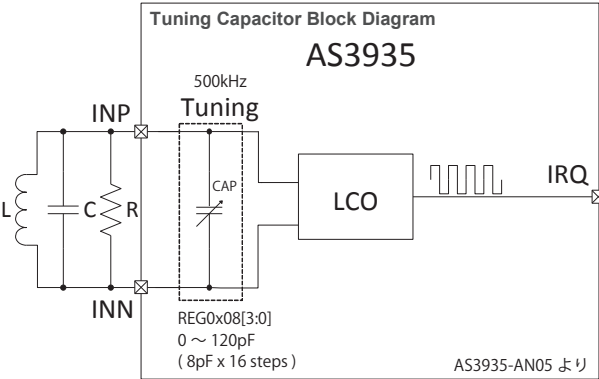
Division Ratio	REG0x03[7]	REG0x03[6]
16	0	0
32	0	1
64	1	0
128	1	1

The antenna tuning algorithm can be performed in the following way: アンテナチューニングの実行方法:

1. Measure actual resonance frequency of the antenna on the IRQ pin.
2. Add additional internal capacitance in parallel to the external LC.
3. Repeat this sequence until the resonance frequency is tuned to 500 kHz.

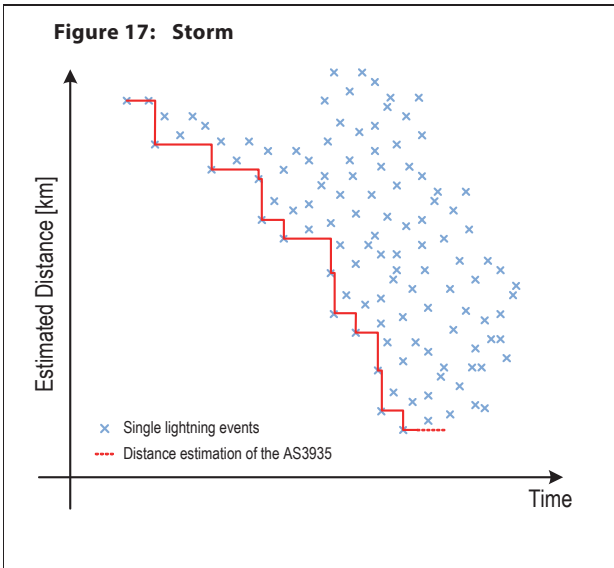
**Measure LCO Frequency** LCO 周波数の測定  
Connect the LCO to the IRQ pin setting register REG0x08[7] = 1. Select the division ratio of the LCO frequency defined in register REG0x03[7:6]. Based on the division ratio the theoretical period can be calculated. Wait 2ms for the LCO to start up and to be settled before measuring the frequency.

Figure 45:



Detailed Description 詳細説明

The AS3935 can detect the presence of an approaching storm with lightning activities and provide an estimation of the distance to the leading edge of the storm, where the leading edge of the storm is defined as the minimum distance from the sensor to the closest edge of the storm. The embedded hardwired distance estimation algorithm of the AS3935 issues an interrupt on the IRQ pin (see Interrupt Management on page 34) every time a lightning is detected. The estimated distance which is displayed in the distance estimation register does not represent the distance to the single lightning but the estimated distance to the leading edge of the storm. A graphical representation is shown in the Figure 17.



Lightning Algorithm 雷検知アルゴリズム

The lightning algorithm consists of hardwired logic. False events (man-made disturbers) which might trigger the AS3935 are rejected, while lightning events initiate calculations to estimate the distance to the head of the storm.

The Lightning algorithm is broken up into three sub blocks:

1. **Signal validation:** Verification that the incoming signal can be classified as lightning.
2. **Energy calculation:** Calculation of the energy of the single event.
3. **Statistical distance estimation:** According to the number of stored events (lightning), a distance estimate is calculated.

In case the incoming signal does not have the shape characteristic to lightning, the signal validation fails and the event is classified as disturber. In that case the energy calculation and statistical distance estimation are not performed and the sensor automatically goes back to listening mode.

The shortest time span between two lightning strikes that the AS3935 can resolve is approximately one second.

Once a signal is classified as disturber the sensor is deactivated for a further 1.5s time period. As the duration of disturber signals can vary, this sensor down time will prevent the sensor from triggering repeatedly due to longer disturber events.

Signal Validation 信号評価

During the signal validation phase the shape of the incoming signal is analyzed. The sensor can differentiate between signals that show the pattern characteristic of lightning strikes and man-made disturbers such as random impulses. Besides the watchdog threshold the spike rejection settings SREJ in REG0x02[3:0] can be used to increase the robustness against false alarms from such disturbers. By default the value is set to REG0x02[3:0] = 0010. Larger values in REG0x02[3:0] correspond to more robust disturber rejection, yet with the drawback of a decrease in detection efficiency. In Figure 41 the detection efficiency is illustrated as function of distance for various settings of SREJ.

At the end of the signal verification, the AS3935 automatically returns to listening mode.

Energy Calculation 強度の演算

If the received signal is classified as lightning, the energy is calculated. The result of the energy calculation is then stored in the registers REG0x06[4:0], REG0x05[7:0] and REG0x04[7:0]. This value is just a pure number and has no physical meaning.

Detection Efficiencies vs. Distance for Different Setting of SREJ, if WDT=0001

