AN1043

Unique Features of the MCP23X08/17 GPIO Expanders

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INTRODUCTION

GPIO expanders provide easy I/O expansion using standard serial interfaces. GPIO products are used to increase the I/O on an MCU or provide remote I/O using a serial interface.

This application note discusses the feature set and use of the MCP23X08/17 (8-bit and 16-bit) GPIO Expanders.

The MCP23X08 are 8-bit GPIO Expanders:

- MCP23008: I^2C™ Interface
- MCP23S08: SPI Interface

The MCP23X17 are 16-bit GPIO Expanders:

- MCP23017: I^2C Interface
- MCP23S17: SPI Interface

The functions and features of the MCP23X08 and MCP23X17 are basically the same, except where otherwise noted.

FEATURES

This application note discusses some of the features of the MCP23X08/17 and how they may be used in an application:

- I/O Port Description
- 8/16-Bit Mode (MCP23X17 only)
- Interrupt Features
  - Mapping Interrupts
  - Mirroring Interrupts (MCP23X17 only)
  - Servicing Interrupts
- Internal Address Pointer Control
- Hardware Address Pin on SPI

I/O PORT DESCRIPTION

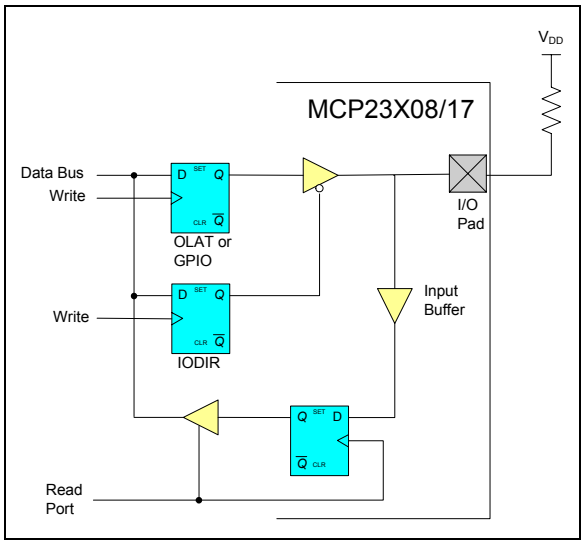
The I/O port is highly configurable for maximum flexibility. Figure 1 is a simplified block diagram of an I/O port pin. The port can either drive logic levels on the pin, or read logic levels from the pad. The level on the pad can be read at any time, regardless if the pin is configured as an input or an output.

The IODIR register controls the direction of the pins (input or output). More specifically, the IODIR registers simply enables/disables the output driver. When the driver is activated (IODIR = 0), the pad is driven to the state in the latch register (OLAT). When deactivated (IODIR = 1), the driver is high impedance.

The I/O port has multiple, individual configurations. Each pin can ...

- ...be configured as an input. The output driver is disabled (high impedance)
- ...be configured as an output. The output driver is enabled and the value in the latch is driven on the pin.
- ...enable a weak pull-up resistor
- ...emulate an open-drain configuration. This is accomplished by clearing the output latch (OLAT) bit to a zero and using the direction register (IODIR) to set the level on the pin. A pull-up resistor is required to pull the pin to voltage when the pin is an input
  - To drive a 0: configure the pin as an output (IODIR = 0) so the port drives whatever is in OLAT (logic 0 in this case)
  - To float a 1: set the pin as an input (IODIR = 1). The output driver is disabled and the pull-up resistor pulls the pin to a logic 1

FIGURE 1: I/O PORT BLOCK DIAGRAM



8/16 BIT MODE (MCP23X17 ONLY)

The MCP23X17 has the unique ability to appear to the MCU as either two (2) 8-bit GPIO expanders, or as a single 16-bit GPIO expander.

This is accomplished by splitting the 16 I/O ports into two separate 8-bit I/O ports (Port A and Port B) via IOCON.bank.

Each port has a group of dedicated registers. Table 1 shows how the register groups (Port A and Port B) are mapped when in 8-bit or 16-bit mode.

Note:	Unlike all other registers which are not shared between the two ports (Port A and Port B), there is one register (IOCON). which is shared between the ports and affects both equally.

8-Bit Mode:

When in 8-bit mode, the ports' registers are separated:

- Port A register addresses range from 00h – 0Ah
- Port B register addresses range from 10h – 1Ah

16-bit Mode:

When in 16-bit mode, the ports' registers are interleaved to emulate 16-bit wide registers:

- Port A and Port B register addresses range from 00h – 15h. The registers are still addressed as 8-bit ports, meaning that the 16-bit mapping pair is always an even number (e.g., IODIR starts at 00h, IPOL starts at 02h, etc.)

TABLE 1: MEMORY MAP

8-bit Mode		16-bit Mode	
Register Name	**Address (hex)**	**Register Name**	**Address (hex)**
IODIRA	00	IODIRA	00
IPOLA	01	IODIRB	01
GPINTENA	02	IPOLA	02
DEFVALA	03	IPOLB	03
INTCONA	04	GPINTENA	04
IOCON	05	GPINTENB	05
GPPUA	06	DEFVALA	06
INTFA	07	DEFVALB	07
INTCAPA	08	INTCONA	08
GPIOA	09	INTCONB	09
OLATA	0A	IOCON	0A
IODIRB	10	IOCON	0B
IPOLB	11	GPPUA	0C
GPINTENB	12	GPPUB	0D
DEFVALB	13	INTFA	0E
INTCONB	14	INTFB	0F
IOCON	15	INTCAPA	10
GPPUA	16	INTCAPB	11
INTFB	17	GPIOA	12
INTCAPB	18	GPIOB	13
GPIOB	19	OLATA	14
OLATB	1A	OLATB	15

INTERRUPT FEATURES

The MCP23X08 has one interrupt pin and the MCP23X17 has two interrupt pins.

For the MCP23X17, each interrupt pin is associated with an 8-bit port. INTA is associated with Port A and INTB is associated with Port B.

Interrupt Mapping

The MCP23X17 interrupt pins can be mapped in two ways (see Figure 2) as controlled by IOCON.MIRROR:

1. Interrupt pins operate independently. INTA reflects interrupt conditions on Port A and INTB reflects interrupt conditions on Port B.
2. Both interrupt pins go active when an interrupt occurs on either port.

Interrupt Polarity and Open-Drain

The interrupts can be configured to operate in three modes:

1. Active-High.
2. Active-Low.
3. Open-Drain.

The interrupt polarity and open-drain is configured via INTPOL and ODR bits in the IOCON register.

Note:	For the MCP23X17, the polarity and open-drain configuration of the INTA and INTB pins are not independent. Both pins are configured the same.

Interrupt Conditions

There are several configurable interrupt conditions which allow flexible configurations.

INTERRUPT-ON-PIN-CHANGE

Pins configured for **interrupt-on-pin-change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt is serviced. For example, an interrupt occurs by an input changing from `1` to `0`. The interrupt is then serviced while the pin state is still `0` by reading GPIO or INTCAP register. The **new** initial state for the pin is a logic `0`. Likewise, if the pin is toggled back to a logic `1` before servicing the interrupt, the new default state is a logic `1`.

The interrupt condition is cleared by reading either INTCAP or GPIO register. The new pin state default is set when the interrupt is cleared.

INTERRUPT-ON-CHANGE FROM DEFVAL REGISTER VALUE

Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTCAP or GPIO is read.

For example, if DEFVAL<b0> = `0`. An interrupt will occur if the pin changes to a logic `1` and the interrupt will remain as long as the pin remains a logic `1`. The interrupt condition will clear if the pin changes back to a logic `0` and INTCAP or GPIO is read.

FIGURE 2: INTERRUPT BLOCK DIAGRAM

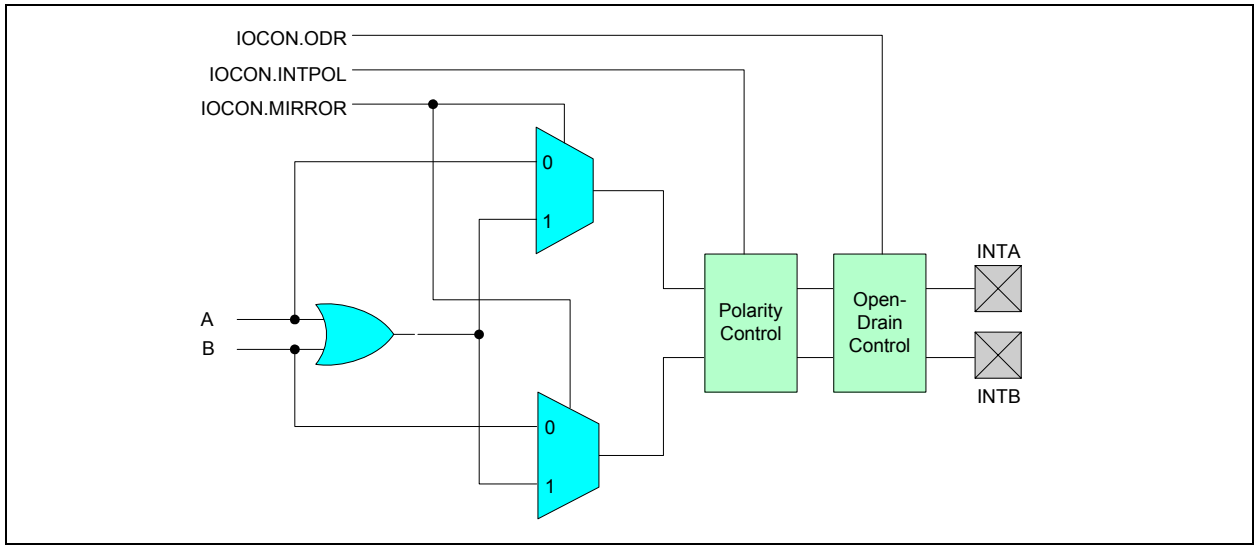


FIGURE 3: INTERRUPT-ON-PIN-CHANGE EXAMPLE

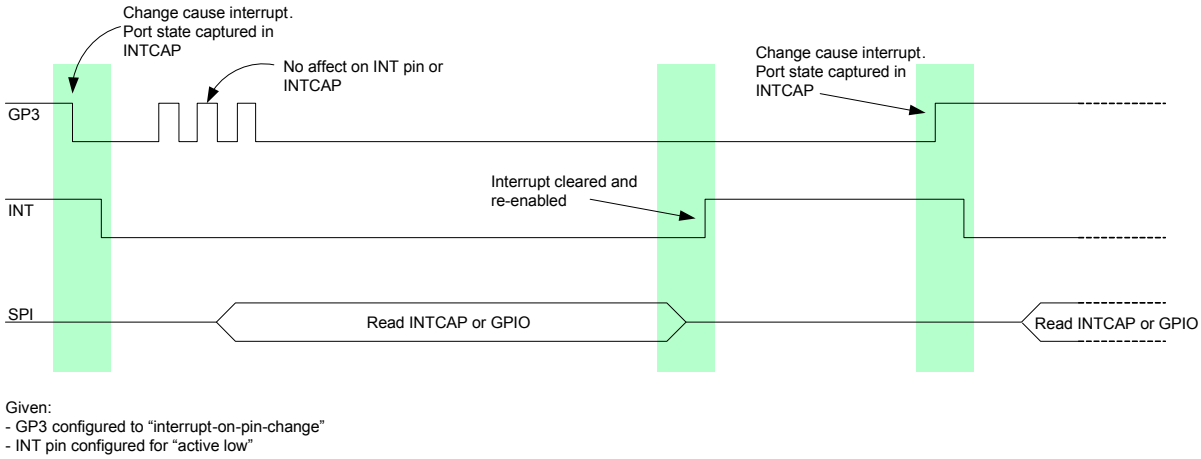


FIGURE 4: INTERRUPT-ON-CHANGE-FROM-DEFVAL EXAMPLE

GPINTEN – GPIO Interrupt-on-Change Enable Register

GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
X	X	X	X	1	X	X	X

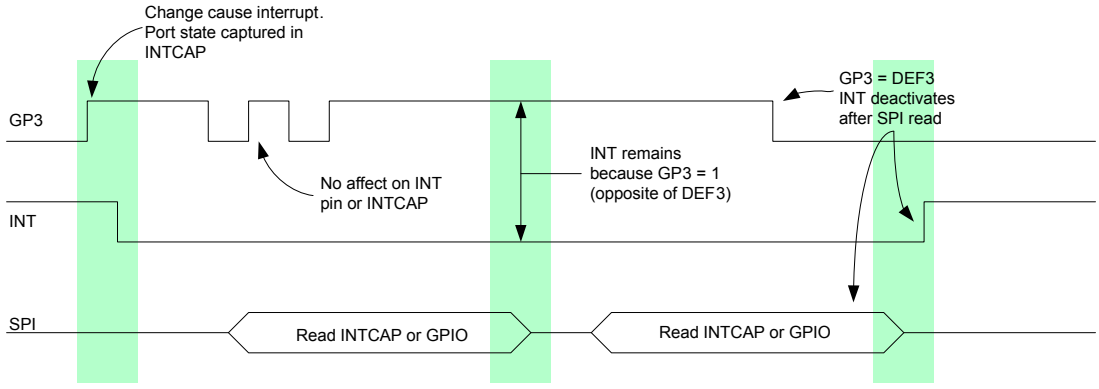
INTCON – Interrupt Control Register

IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
X	X	X	X	1	X	X	X

DEFVAL – Default Value Register

DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
X	X	X	X	0	X	X	X

Interrupt will occur if GP3 logic level = 1



INTERNAL ADDRESS POINTER CONTROL

Some slave serial devices automatically increment their internal address pointer after each byte is clocked by the master. This allows the master to sequentially access multiple registers without re-sending the write or read command.

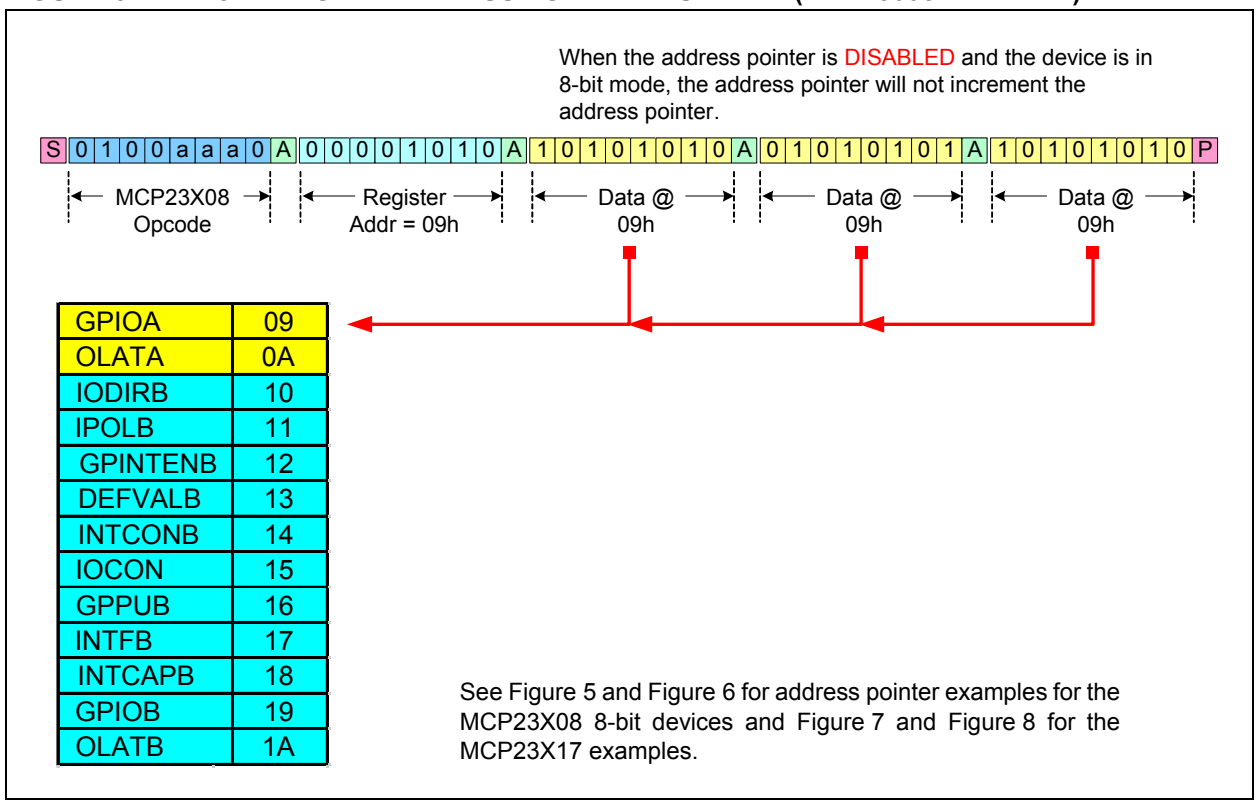
Other slave devices do not automatically increment their internal address pointer.

The MCP23X08/17 family of devices have the ability to do either by configuring a control bit (IOCON.SEQOP). This allows maximum flexibility when accessing the registers.

For example, when configuring the device, it may be desirable to allow the address pointer to automatically increment so the device does not have to be re-addressed after every byte.

Likewise, when performing a continuous operation on a register (e.g., changing the outputs on a regular basis by writing to GPIO or OLAT), it may be beneficial to disable the address incrementing feature so that the register is always accessed without re-addressing the register.

FIGURE 5: 8-BIT MODE: ADDRESS POINTER DISABLED (MCP23008 EXAMPLE)



See Figure 5 and Figure 6 for address pointer examples for the MCP23X08 8-bit devices and Figure 7 and Figure 8 for the MCP23X17 examples.

FIGURE 6: 8-BIT MODE: ADDRESS POINTER ENABLED (MCP23008 EXAMPLE)

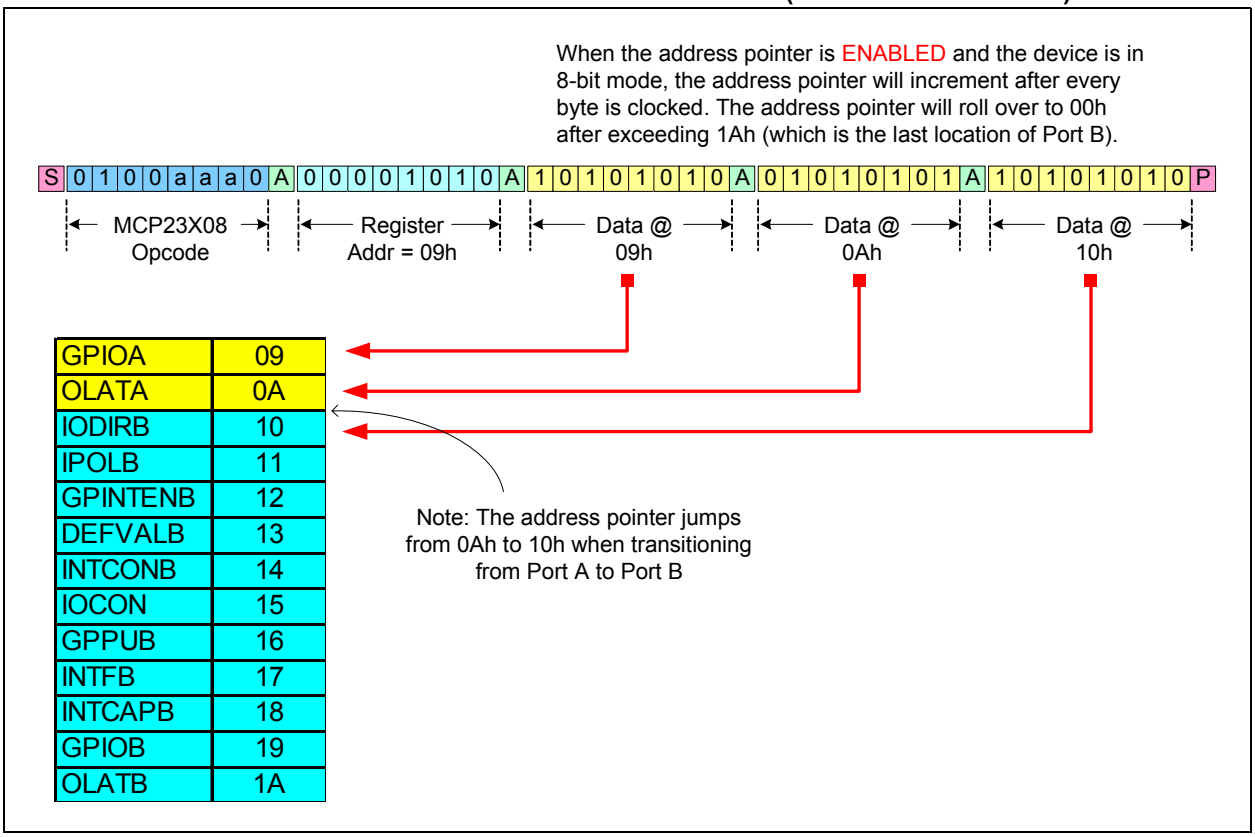


FIGURE 7: 16-BIT MODE: ADDRESS POINTER DISABLED (MCP23017 EXAMPLE)

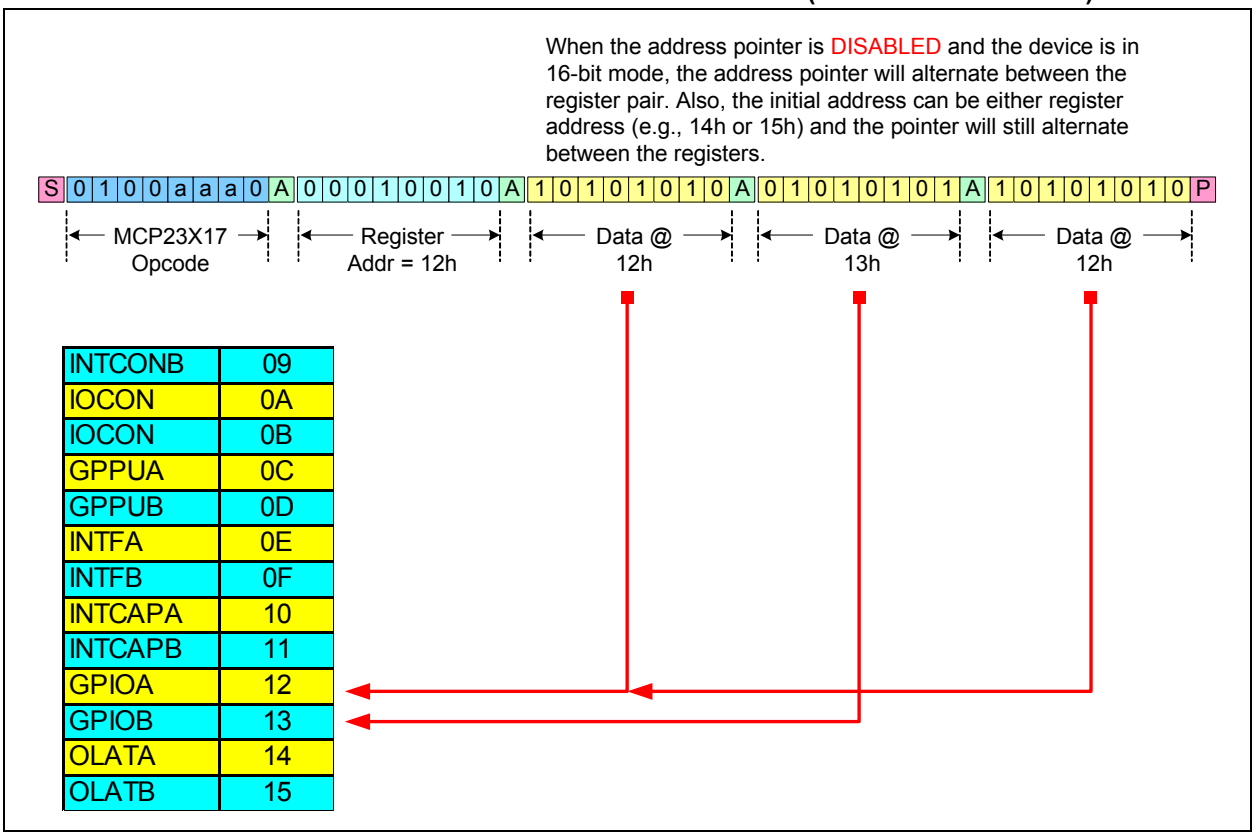
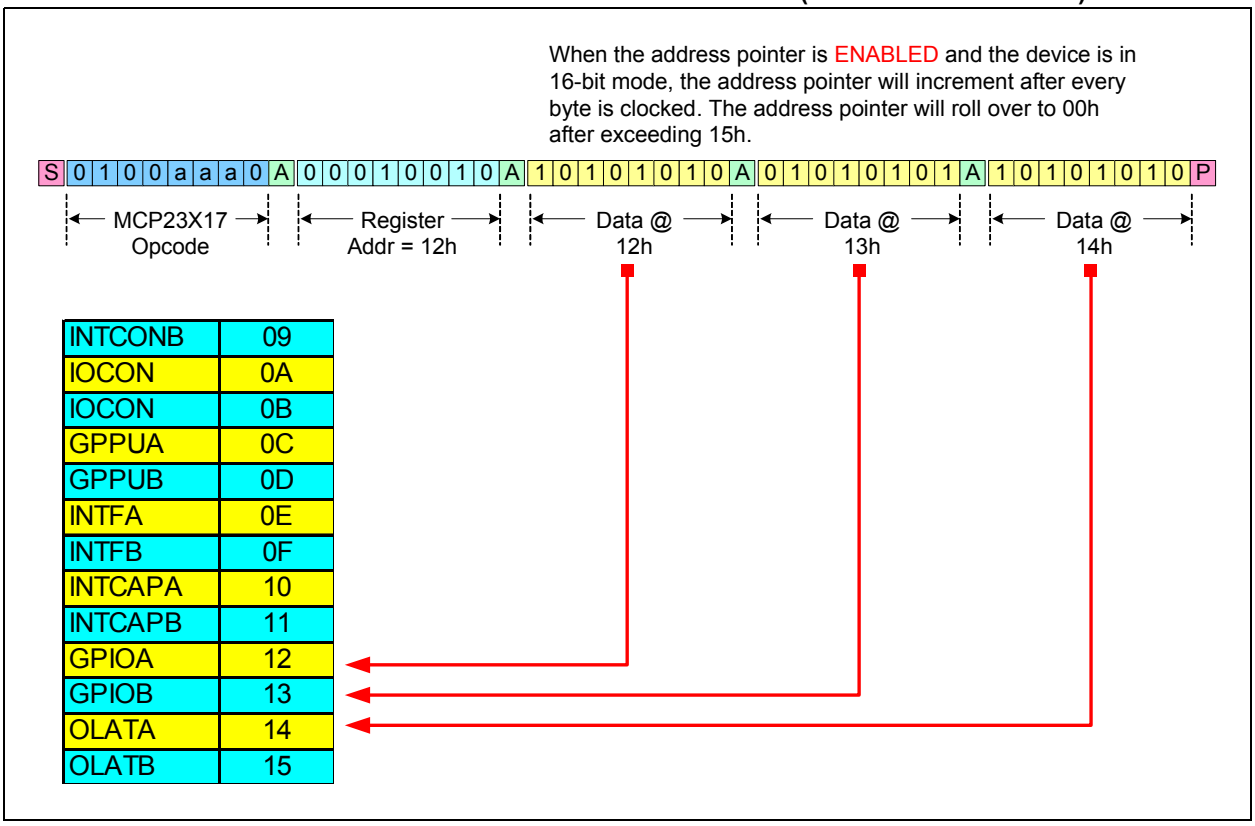


FIGURE 8: 16-BIT MODE: ADDRESS POINTER ENABLED (MCP23017 EXAMPLE)



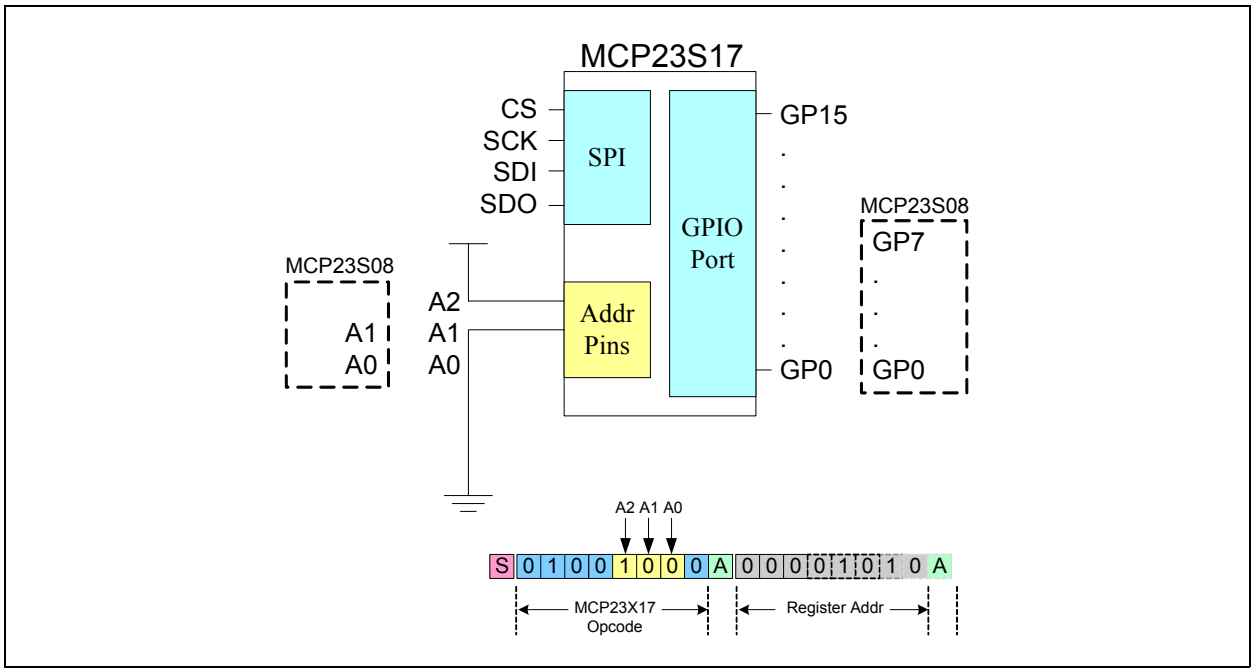
HARDWARE ADDRESS PINS

Address pins are typically used on I^2C devices to allow multiple devices with the same base slave address to operate on the bus.

Slave devices with SPI interfaces typically use only a chip select pin to select the device. This requirement consumes one MCU pin for every SPI device on the bus.

The “S” devices (MCP23S08 and MCP23S17) have SPI interfaces. These devices use a chip select for selecting the part, however, these parts also have hardware address pins, thereby giving the advantage of attaching multiple devices on the bus while only consuming one MCU pin for chip select (see Figure 9).

FIGURE 9: ADDRESS PINS ON SPI DEVICES



SUMMARY

The MCP23X08/17 family of GPIO Expanders have some unique features, giving the system and module engineer maximum flexibility when designing with the MCP23X08/17.

Note the following details of the code protection feature on Microchip devices:

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