1.2 Operational and Application Notes

The serial bus, or Multi-Drop Bus (MDB) is configured for Master-Slave operation. There is one Master with capability of communicating with up to thirty-two peripherals. The Master is defined as the Vending Machine Controller (VMC).

Each peripheral is assigned a unique address and command set. The master will "poll" the Bus for peripheral activity. That is, each peripheral is asked for activity, and responds with either an acknowledge, negative acknowledgment, or specific data dependent on its current activity. If a peripheral does not respond within a predefined time, (t-non-response as defined in the peripheral sections) it is assumed that it is not present on the Bus.

Bus interference, or "crashes" are prevented because each peripheral only responds upon being polled. Since there is only one master, and all communication is initiated by the Master, Bus "crashes" are easily precluded.

All peripherals will recognize a disable command, or commands, sent by the Master. This allows for disabling of individual peripherals for various reasons, for example, power management techniques.

Error checking and correction is accomplished by using checksums (CHK) and a retransmit command.

2.1 Byte Format

Baud Rate: 9600 NRZ

Serial Bit Format:
1 Start Bit
8 Data Bits
1 Mode Bit
1 Stop Bit

11 Bits Total

LSB									MSB
Start	0	1	2	3	4	5	6	7	Mode	Stop

Mode Bit: Master-to-Peripheral

The mode bit differentiates between ADDRESS bytes and DATA bytes. ADDRESS bytes must be read by all peripherals, DATA bytes are only read by the peripheral that has been addressed.

The mode bit is set (logic one) to indicate an ADDRESS byte, and not set (logic zero) to indicate a DATA byte.

Mode Bit: Peripheral-to-Master

The mode bit must be set on the last byte sent when data is sent from a Slave to the Master.

2.2 Block Format

Master-to-Peripheral

A Communication Block for Master-to-Slave transmissions is defined as an Address byte, optional data bytes, and a CHK byte. A block is limited to a maximum of thirty-six (36) bytes.

The upper five bits (MSB) of the Address Byte will be used for addressing. That is, bits 7,6,5,4,3 of the previous byte description will be used for addressing.

The lower three bits (i.e. 2,1,0) of the Address Byte will contain peripheral specific commands. This will allow up to eight instructions to be embedded in the first byte of a block.

The VMC Master will respond to data from a peripheral with an Acknowledgment (ACK), Negative Acknowledgment (NAK), or Retransmit (RET). These are defined later in the document. The 5 mS time-out (t-response) described in the Bus Timing section of this document is the equivalent of a NAK.

If the addressed Slave does not respond within the 5 mS time-out (silence), the Master may repeat the same command, or send a different command, until it receives an answer or until the end of the Non-Response time, as defined in the peripheral sections. See Example in 2.5D. The RESET command should not be used as a recovery method to a 5 mS time-out (t-response) until after exceeding the Non-response time. The VMC may send commands to any other peripheral during this time.

Peripheral-to-Master

A Communication Block for Slave-to-Master transmissions consists of either a data block and a CHK byte, a acknowledgment (ACK), or a negative acknowledgment (NAK).

The 5 mS time-out (t-response) described in the Bus Timing section of this document is the equivalent of a NAK command. In addition, it is recommended that the peripheral use this time-out as the NAK when a reception error of the ADDRESS byte occurs. This will prevent several peripherals from trying to simultaneously respond with a NAK.

A data block consists of one or more data bytes followed by a CHK byte. The CHK byte is defined later in this document.

The data block and CHK byte are limited to a maximum size of 36 bytes.

A CHK byte is not required when a peripheral responds with NAK or ACK byte. ACK and NAK are defined later in this document.

The peripheral must set the mode bit on the last byte sent to signify end of transmission. This will be either the CHK byte of a block, a NAK byte, or an ACK byte. The mode bit must not be set except for the conditions above.

A peripheral response of ACK or NAK signifies the end of the exchange.

When a peripheral responds with a data block, the VMC must respond with an ACK, NAK or RET. If the Master cannot respond within the 5 mS time-out (t-response) the peripheral must repeat the data block, or append it, at the next possible occasion (i.e. to a later POLL). The same behavior is to apply when the Master responds with NAK.

CHK Byte

A CHK byte must be sent at the end of each block of data. The CHK byte is a checksum calculated by adding the ADDRESS byte and all DATA bytes. The CHK byte is not included in the summation. The carry bit for CHK additions is ignored since the CHK byte is limited to eight bits.