Opto-electrical isolation of the I^{2}C bus

Introduction

The Inter Integrated Circuit (I^{2}C) bus provides an attractive maintenance and control communication interface between parts of a system since it uses only two signal wires yet has powerful addressing and a reasonably fast, up to 400 kHz , bi-directional data handling capability. Some of these systems require control modules to be connected to telephone lines, or to electronic switches that are directly connected to the high voltage AC main power supply, and need to be electrically isolated. Additionally, medical patient monitoring equipment needs to operate without any common physical interconnection wiring to form a safety isolation barrier to prevent any chance of electrocution.

In these and similar applications there is a need for galvanic isolation, so including opto-couplers in I²C-bus signal wires is obviously attractive. Unfortunately it is not so simple to provide opto-isolation of the I²C-bus because the I²C clock and data signals are both bi-directional signals while opto-couplers can only handle uni-directional signals. The challenge to optically isolate the I²C-bus has always been to effectively split the bi-directional I^{2}C signals into uni-directional data streams and recombine them again.

There have been many circuits published over the last decade attempting to opto-isolate parts of an I²C-bus system. All result in, and most admit to, problems with glitches resulting from signal propagation delays. All the circuits are based upon the concept of temporarily blocking the bi-directional I^{2}C signal propagation in one direction in order to prevent bus latch-up caused by feedback of the logic signals. As a result they all produce a bus 'glitch' during the propagation time of the logic signals that must clear the blocking process when the bus driving signals change. Figure 1 shows a circuit from a National Semiconductor Application, typical of published circuits for opto-isolating the I²C-bus.
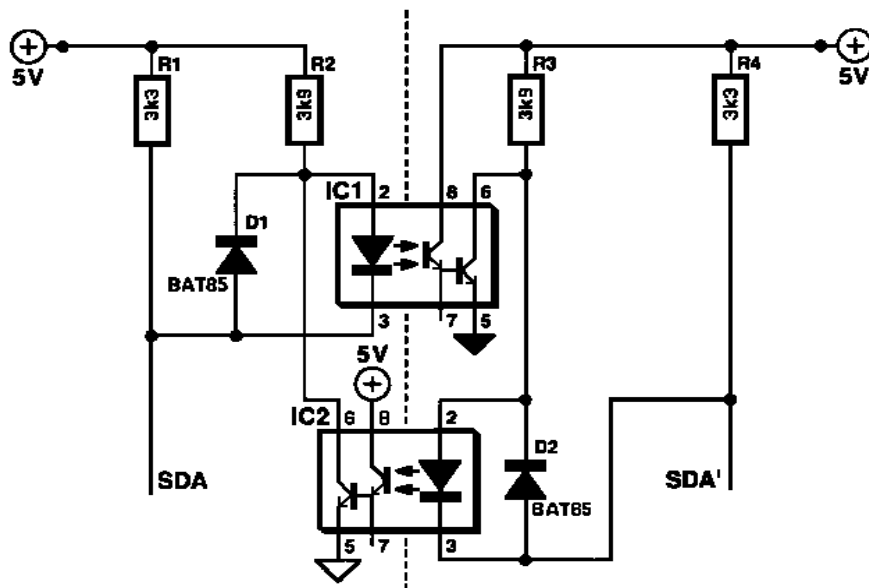

Figure 1 National Semiconductor Application circuit ca.1998.

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To check whether an isolating circuit will generate unwanted glitches on the bus, there is a very simple test that can be applied. Drive one side of the isolating circuit low, then, holding that first side low, drive the other side low. Then release the drive on the first side. If the system conforms to the I^{2}C protocol the first side should just stay low, held low by the second side.

Let's try this test on the circuit of Figure 1. Drive the left side SDA low. Current in R2 turns on the LED in opto-coupler IC1. The photo-transistor in IC1 turns on and the isolated SDA$^|$ is pulled low via diode D2. Now drive the right hand side SDA$^|$ low. It is already low so the SDA$^|$ bus does not change state. The photo-transistor in IC1 remains on, so there is no current in the LED of IC2. Now release SDA. SDA immediately goes high because there is nothing to hold it low; the photo-transistor in IC2 isn't on. This represents the start of an unwanted 'glitch' of the I²C-bus at SDA. With SDA high, the LED of opto-coupler IC1 turns off and after some delay time its photo-transistor turns off. After IC1 turns off, R3 can source current to pin 2 of the LED in opto-coupler IC2 and current flows, via the LED, to SDA$^|$ which is being held low. After another switch-on delay the photo-transistor in IC2 turns on and SDA is pulled down again to the correct state, ending the unwanted 'glitch'. But notice SDA was high during the time taken for IC2 to turn off plus the time taken for IC1 to turn on. This is a false bus signal that can lead to problems.

Eliminating unwanted bus 'glitches'

The way to eliminate these glitches is by using the P82B96 I^{2}C buffer IC. It introduces special logic voltage levels on one of its inputs to prevent bus latching. It never blocks any signals, it uses instead different logic voltage levels that are all placed below the normal bus logic 'low' level and are therefore transparent to the connected I^{2}C chips. False bus glitches are eliminated, but of course some bus signal propagation delays are still introduced and these delays can act to limit the maximum bus clock speed.

Figure 2 shows the simple circuit contained in Philips' Application note AN460 that uses the P82B96 for opto-isolation of I²C-bus signals using low cost 4N36 opto-couplers. This simple circuit allows saturation of the photo-transistor in the opto-coupler, resulting in long turn-off delays caused by charge storage effects. The total switching delays will be around 50 microseconds and this limits the bus speed of this circuit to around the 5 kHz clock rate.
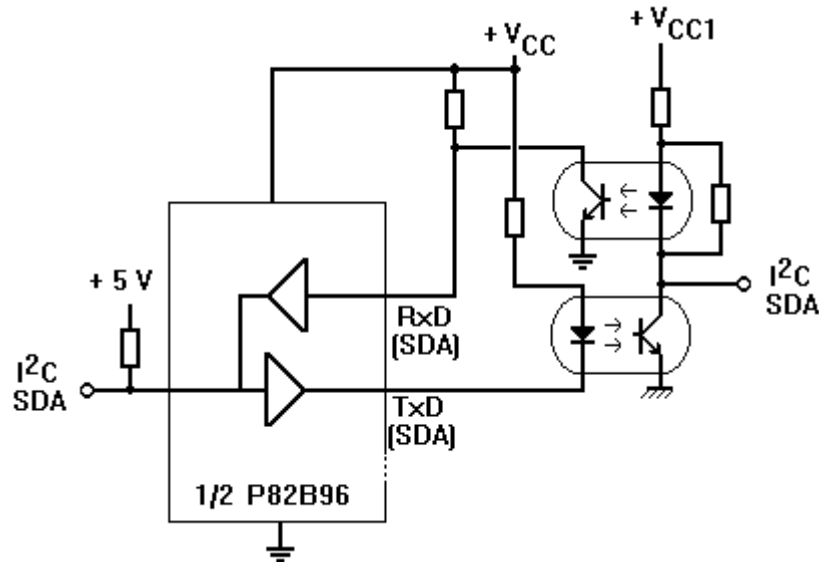
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Figure 2. Simple 5 kHz Opto-electrical isolation circuit.

Achieving higher bus speeds

Increasing the LED drive current can reduce the turn-on delay of an opto-coupler, but unless steps are taken to prevent the consequent deeper saturation of its photo-transistor, the turn-off delay will increase and the total signal delays will increase. To reduce the turn-off delay a traditional technique to prevent saturation of the photo-transistor is to apply a Schottky diode clamp between its collector and base, as used in Schottky TTL logic.

An alternative approach is to apply feedback to regulate (limit) the current in the photo-transistor so it will be unsaturated and operating in a linear mode, with a relatively higher collector-emitter voltage, at the instant when it is required to switch off. The circuit of Figure 3 shows a low cost dual transistor added to each opto-coupler to prevent saturation of the photo-transistor and reduce the turn-on and turn-off delays to less than 5 microseconds each, extending bus operation to 50 kHz. The circuit can be adapted to a wide range of couplers, providing a choice of isolating voltage specification. It offers reasonable bus speed for lower cost than using true high speed couplers.
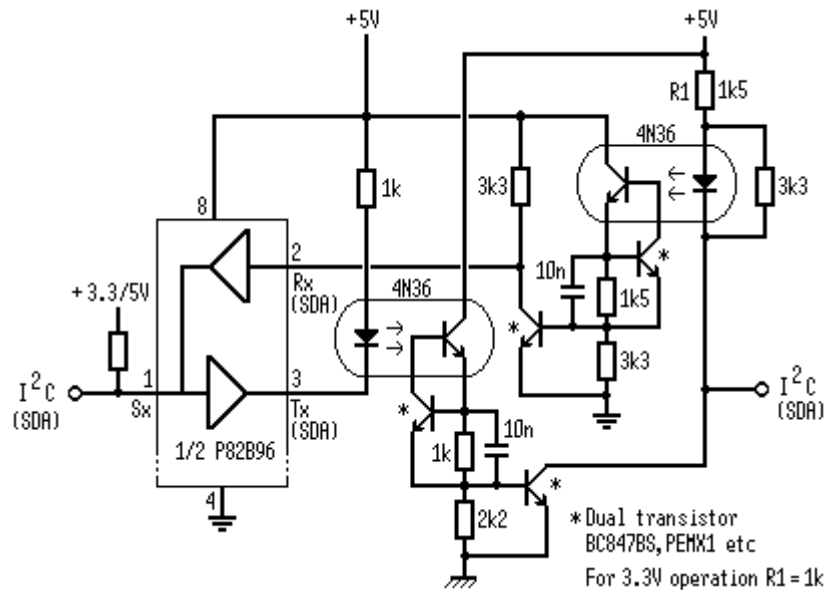
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Figure 3. 50 kHz application with general purpose low speed opto-couplers

The resistor values in Figure 3 are selected for 5 V operation, setting LED drive to around 2 mA to stay within the 3 mA maximum sink allowed in an I²C system. For operation on 3.3 V, only resistor R1needs to be reduced to maintain the 2 mA drive, taking account of the published diode voltage drop for the opto used. For 4N36, R1 should be reduced to 1kΩ.

Figure 3 shows two 10 nF capacitors added to the feedback path to further improve switching times. During turn-on of the photo-transistor this capacitor delays the feedback, increasing the drive and improving the turn-on time. When the photo-transistor drive is removed the delay caused by the 10 nF again delays the removal of the feedback. This causes an excess base current to be drawn out of the base of the photo-transistor by the current regulating transistor during switch-off, further improving the fall-time of the current. The opto-coupler propagation delays measured with 4N36 were reduced to around 2 - 3 us each, giving some safety margin on the recommended 50 kHz bus speed to take account of different components that might be used. The bus speed recommendation is also based on conforming to 100 kHz Standard mode bus timings when using ICs specified for use in 100 kHz systems.   The allowed clock speed specification is calculated by simply adding the delay introduced by P82B96 and the opto-couplers to the minimum SCL 'low' period and calculating a new frequency based on a symmetrical clock. The typical system performance may be found to be much better, especially when using components specified for 400 kHz bus operation because their maximum response delays are smaller, but 100 kHz operation remains theoretically impossible with these low cost couplers.

This speed-up technique should prove economical when applied to any opto switching application where a higher speed is an advantage but higher speed couplers cannot be justified. If there is no restriction on the available LED drive then even smaller turn-on delays can be achieved. Turn-off delays remain limited by the fall-time of the current in the photo-transistor.

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Achieving the full 100 kHz bus speed

Obviously faster system speeds require faster opto-couplers and parts such as 6N137 reduce the switching delays to less than 100 ns each when operating in a 5 V bus system as shown in Figure 4.
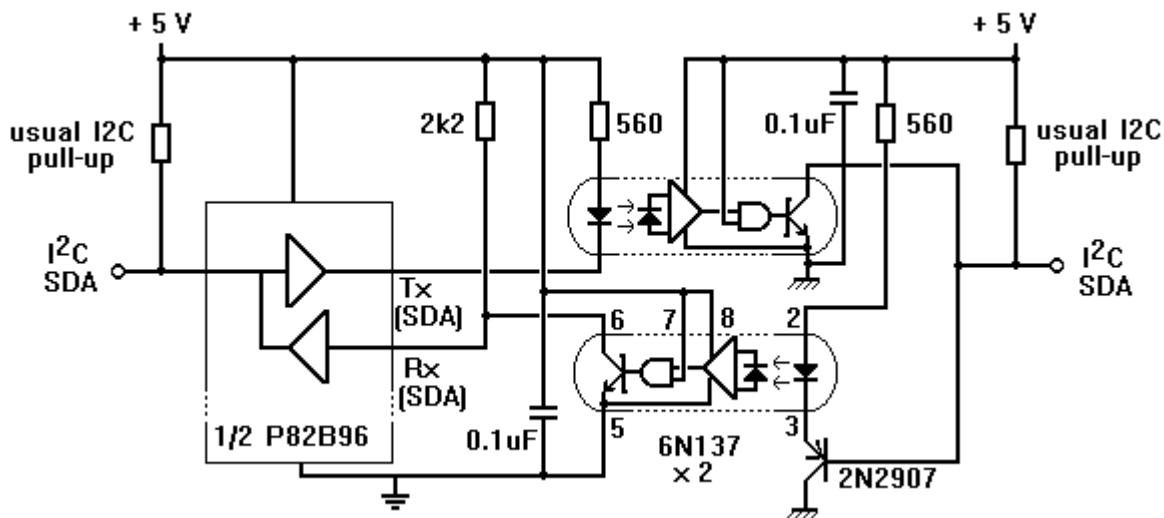
Figure 4. High speed opto-couplers achieve 100 kHz operation.

Is 400kHz operation possible?

Because the original I^{2}C specifications did not envisage the development of bus buffering components or the possibilities for signal propagation delays in the system, it is strictly not allowed to introduce any delays other than those anticipated in the bus rise and fall times. In practice typical I^{2}C parts do not use up all of the allowed response time that can be calculated from the bus specifications. For example, the typical response time for ICs specified for 400 kHz application are mostly under 700 ns while the bus specifications allow for 1.3 us delays. This means that in practice delays up to 600 ns can be tolerated. P82B96 introduces delays around 400 ns and fast couplers will have delays less than 100 ns so in practical systems, when the designer checks the actual bus timings, 400 kHz opto-coupling can be achieved. The fastest circuit, designed for interfacing 3.3 V logic, is shown in Figure 5. The P82B96 data sheet also gives examples of modifying the duty cycle of the clock when attempting to reach the highest speeds and those techniques are also applicable to delays introduced by opto isolation.

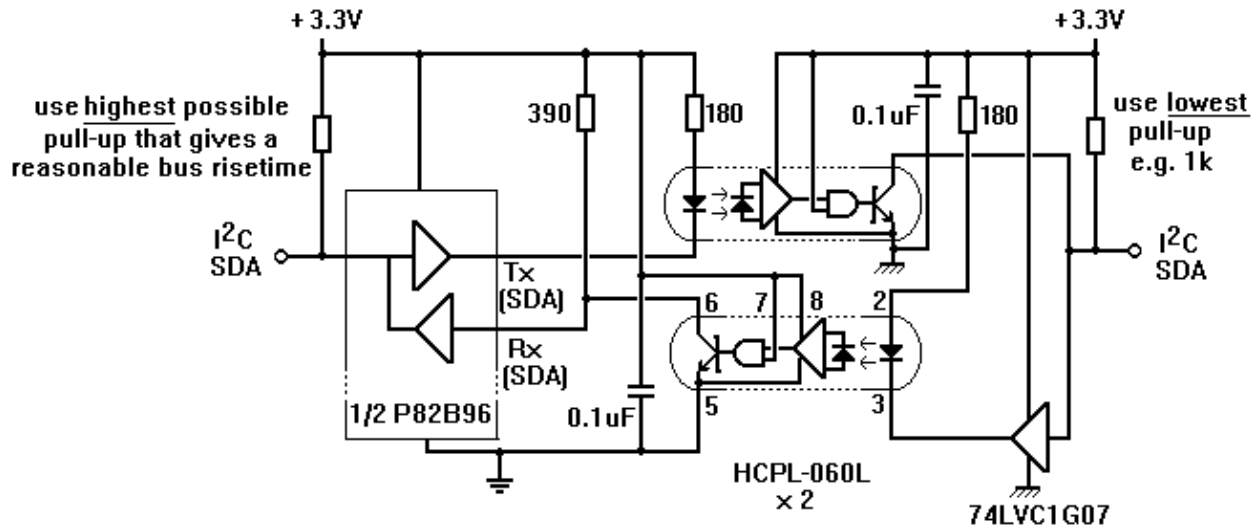# Opto-electrical isolation of the I^{2}C bus

Figure 5 Suggested circuit for 400 kHz applications

Multi-node Opto-electrical Isolation

The examples so far have considered only a single isolated module connected to a normal bus. When more than one module must be isolated, or when a lower impedance or higher voltage distribution bus is required then care must be taken to run those distribution buses at normal logic signal levels. In particular the Sx levels must never be distributed because they have lower tolerance to noise. That means the Optocoupler must always be connected to the distribution bus.
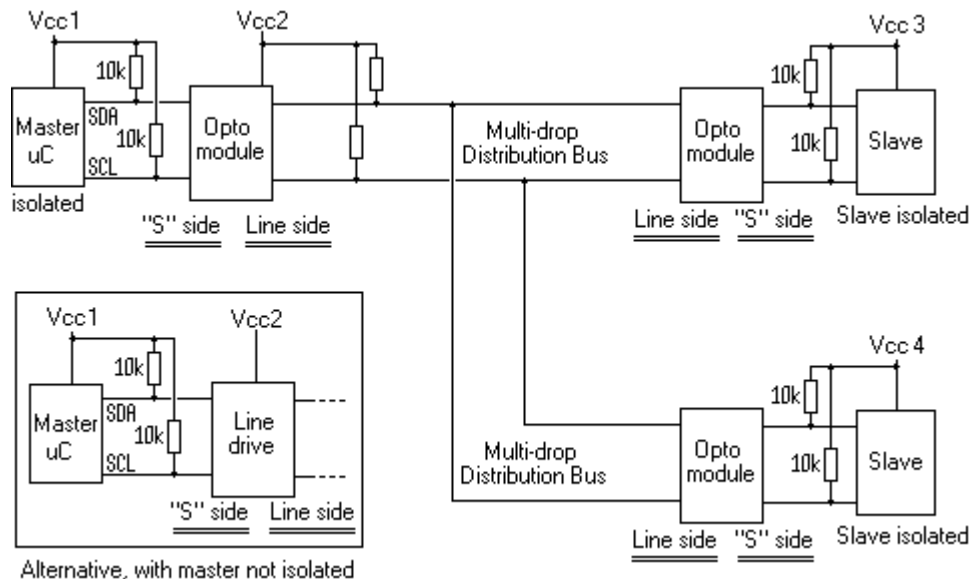

Figure 6 Suggested circuit for Multi-point Applications
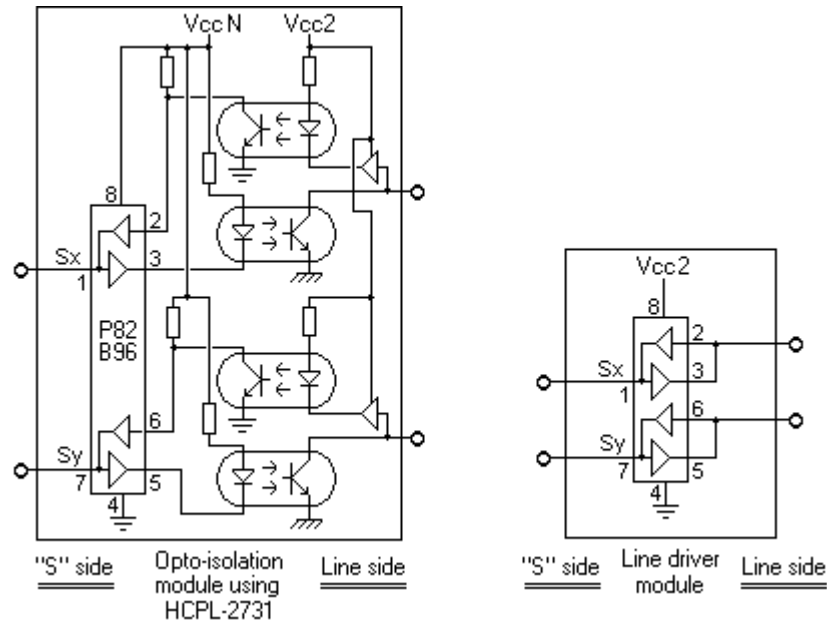
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Figure 7 Suggested modules for use in the system of Fig. 6

Fig. 6 shows a general arrangement for a multi-drop system in which isolated and non-isloated modules can be mixed as required. The coupler shown in the example in Fig. 7 is the Darlington type HCPL-2731 with an 18V rating and guarantees when sinking 24mA. It can be used to directly drive lower impedance higher voltage distribution bus lines in exactly the same way P82B96 is used. It can interface with other isolated modules or with a simple P82B96 line driver module as also shown in Fig. 7 when isolation is not required. Both isolated and non-isolated modules can be used to connect the master(s) or any slaves to the distribution bus wiring. When many isolation modules are used in a system it is convenient to build the opto modules as shown in Fig. 7 with a logic buffer (e.g. HEF 4050B) driving the LED on the line side. That ensures each module imposes no load on the distribution bus and saves making calculations about loading. When only a small number of modules is used then a buffer is not needed, but just remember to include the LED drive current when calculating the pull-up resistor(s) for the line side distribution bus to remain under 24mA.

When using the HCPL-2731 the distribution bus pull-ups should be calculated for no more than the 24mA guaranteed rating of that part. That still allows 510Ω pull-ups to 12 V and should be OK for about 2 nF (say < 20 meters) of wiring capacitance. If the bus and its capacitance is small then it is not necessary to waste energy and larger resistance pull-ups can be used. The cheapest, simplest, opto interface as shown in Fig 7 is very slow and the warnings about 5 kHz maximum as for Fig. 2 should be taken seriously. It's wise to monitor the waveforms around the opto devices and check they are doing what the data sheet implies.
For higher bus speeds it's necessary to adapt the faster opto circuits in Fig 3, 4, 5. In every case note it must be the opto-coupled side of the module that interfaces to the distribution bus because this side has normal I2C characteristics and full noise margins. Do not connect the Sx sides of an opto module to a distribution bus because that interface has lower noise margins. The Sx interface is intended for connection only to standard I²C parts and not to other buffers. For details see AN255-03.

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Fig. 8 gives one example of how the 100kHz circuit might be adapted to driving a lower impedance buffered bus. LVC gates are specified to sink 32mA with a 5V supply so they allow the same pull-ups as the direct P82B96 line drive module. Keep in mind when running at higher speeds that low value pull-ups may be required to keep reasonable risetimes. Lower value pull-ups in turn can force the use of lower supply voltages on the buffered bus. For this reason, and the 7V limitation of the 6N137, the circuit shown in Fig 8 is suitable for only for 5V buses.

Adapting higher speed buses to higher voltages, while working with the lower voltage ratings of faster optocouplers, will require some level shifting technique e.g. a FET such as 2N7002 in common-gate configuration as the driver, and a resistive voltage divider on the receiver as shown in Fig 9. The resistive divider should be made high impedance, compared to the bus pull-up, to avoid any significant lowering of the bus 'high' logic level. (This divider technique obviously has limitations if very many modules are needed. Then an alternative is to replace the 1G07s by 3-state high voltage logic, e.g. HEF40244B, using the active-low enable pins as the inputs)

In these examples Picogates are shown as the logic buffers because they simplify layout. A Hex device like 74LVC07A will be lower cost but, with gates effectively connected in series, care should then be taken with stray capacitance coupling that could cause instability.
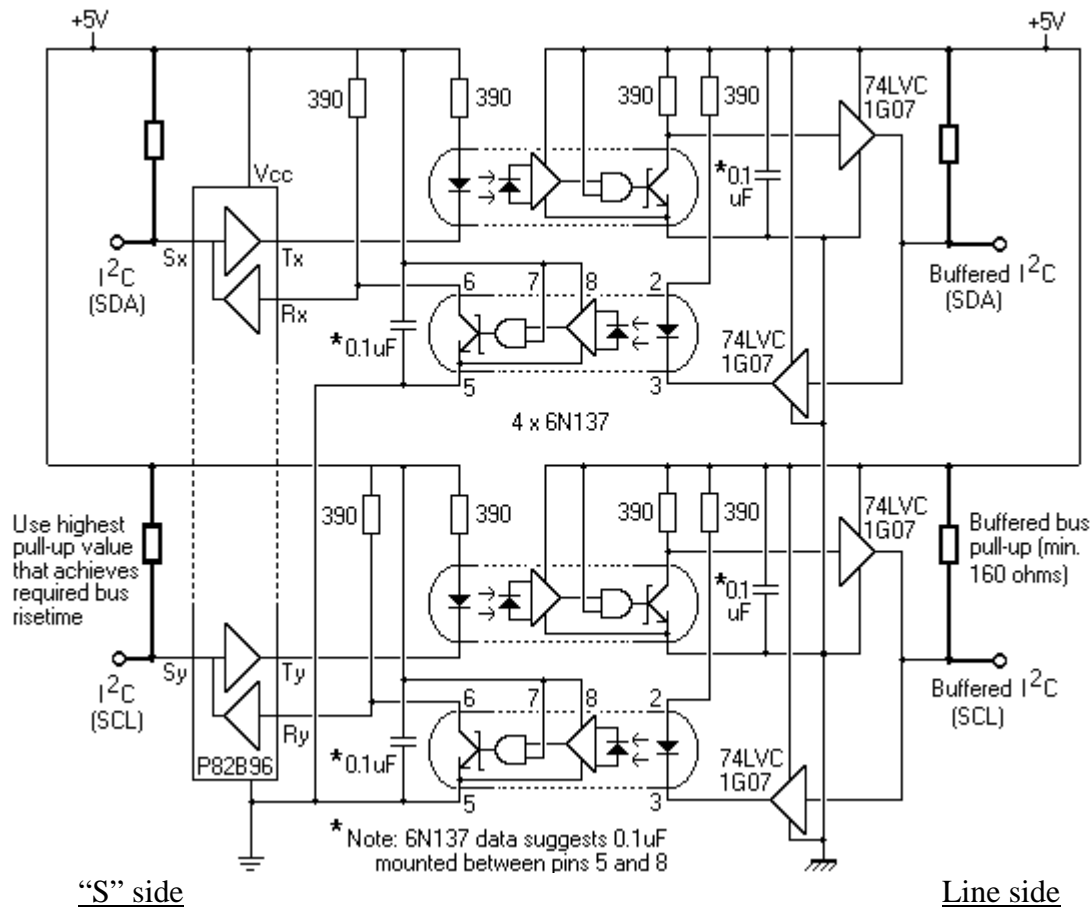

Figure 8   Suggested 5V/100kHz distribution bus module with isolation
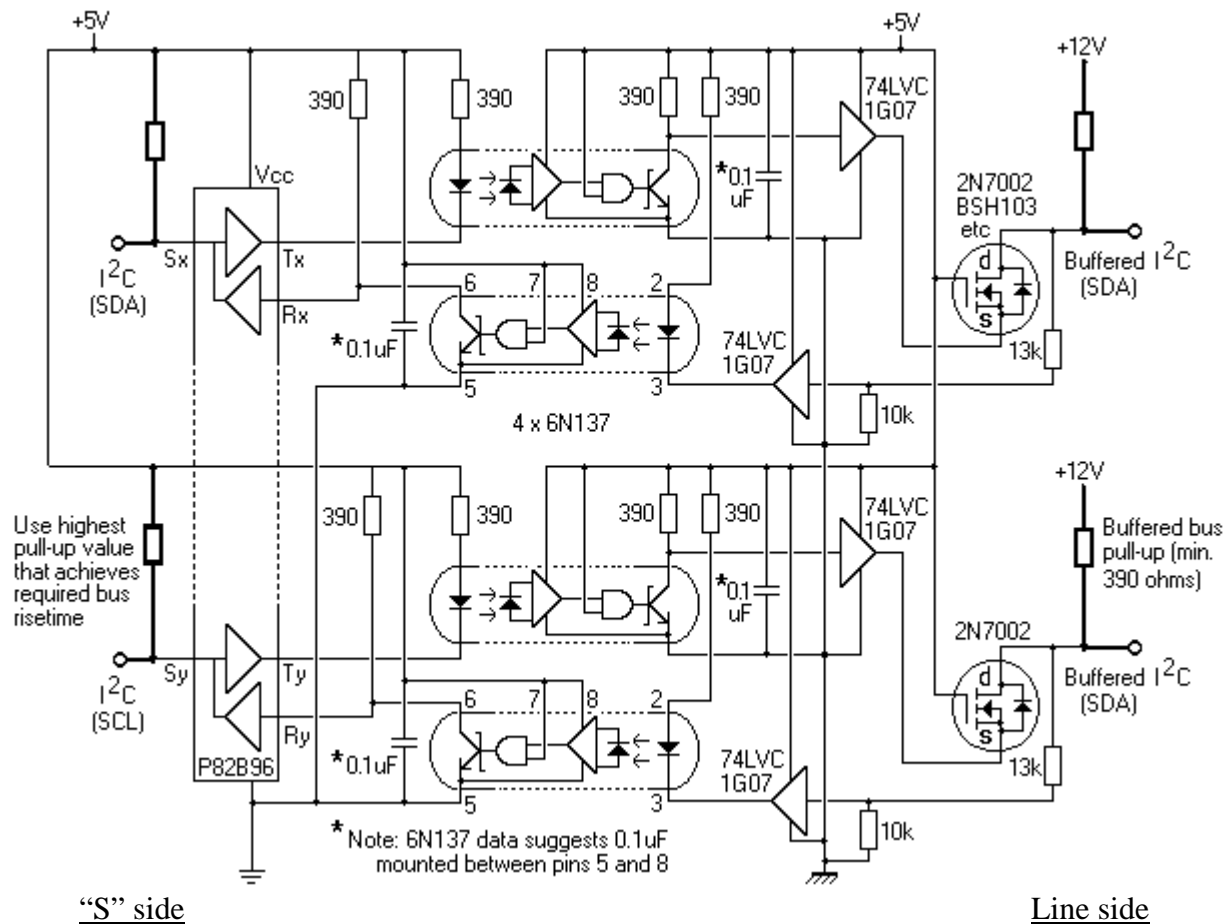
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"S" side   Line side

Figure 9   Suggested 12V/100kHz distribution bus module with isolation

Conclusion

Using P82B96 to split the bi-directional I^{2}C signals into unidirectional signals enables simple opto-isolation of an I²C-bus, without generating any spurious glitches, and offering various cost/speed performance levels.

Further background to the design of special buffered or isolated I²C-bus design can be found at the Philips Semiconductors website http://www.philips.com/i2c or the Philips Semiconductors Logic Products Group website at http://www.philips.com/i2clogic.