DOCUMENT NUMBER AND REVISION

VL-PS-COG-C144MVGD-04 REV.A

(1.44"CSTN CGA+FPA+BL)

DOCUMENT TITLE:

PRELIMINARY SPECIFICATION

OF

LCD MODULE TYPE

MODEL NUMBER: COG-C144MVGD-04

DEPARTMENT	NAME	SIGNATURE	DATE
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DISTRIBUTION LIST: MARKETING

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2008.06.19	First Release.	XIAO LI LAN	LUO CHENG

CONTENTS

VARITRONIX LIMITED

Preliminary Specification
of
LCD Module Type
Model No.: COG-C144MVGD-04

1. General Description

- 1.44" CSTN, 128 x RGB x 128 dots, 65K, Negative, Transmissive, dot matrix LCD module.
- Driving scheme: 1/128 duty.
- Viewing angle: 6 O'clock.
- Driving IC: 'SITRONIX' ST7687S (COG) LCD Controller / Driver or equivalent.
- Data interface: 8080/6800 system 8-bit parallel bus.
- Logic voltage: ~2.8V.
- FPC connection.
- White LED backlight.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig.1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		32.36(W) x 53.3(H) x 3.25(D) (Include FPC, the terminal of backlight, component area)	mm
Color STN 128 x RGB x 128	Viewing area	28.10(W) x 28.20(H)	mm
	Active area	25.49(W) x 26.49(H)	mm
	Display format	128 x RGB x 128	dots
	Color configuration	RGB stripe	-
	Dot size	0.1892 (RGB)(W) x 0.197 (H)	mm
	Dot spacing	0.01 (W) x 0.01 (H)	mm
	Dot pitch	0.1992(RGB)(W) x 0.207(H)	mm
Weight		TBD	gram

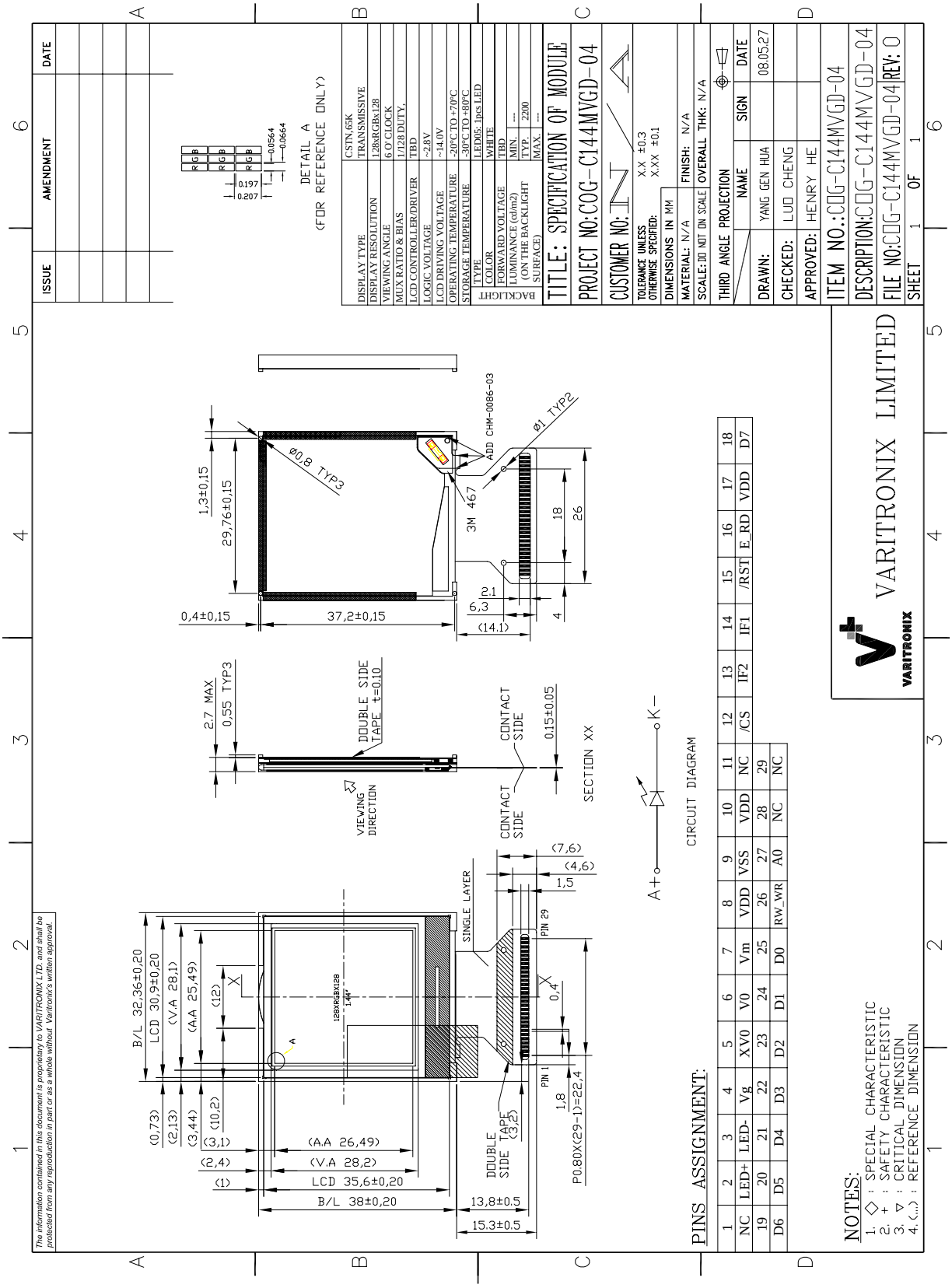


Figure 1: Module Specification

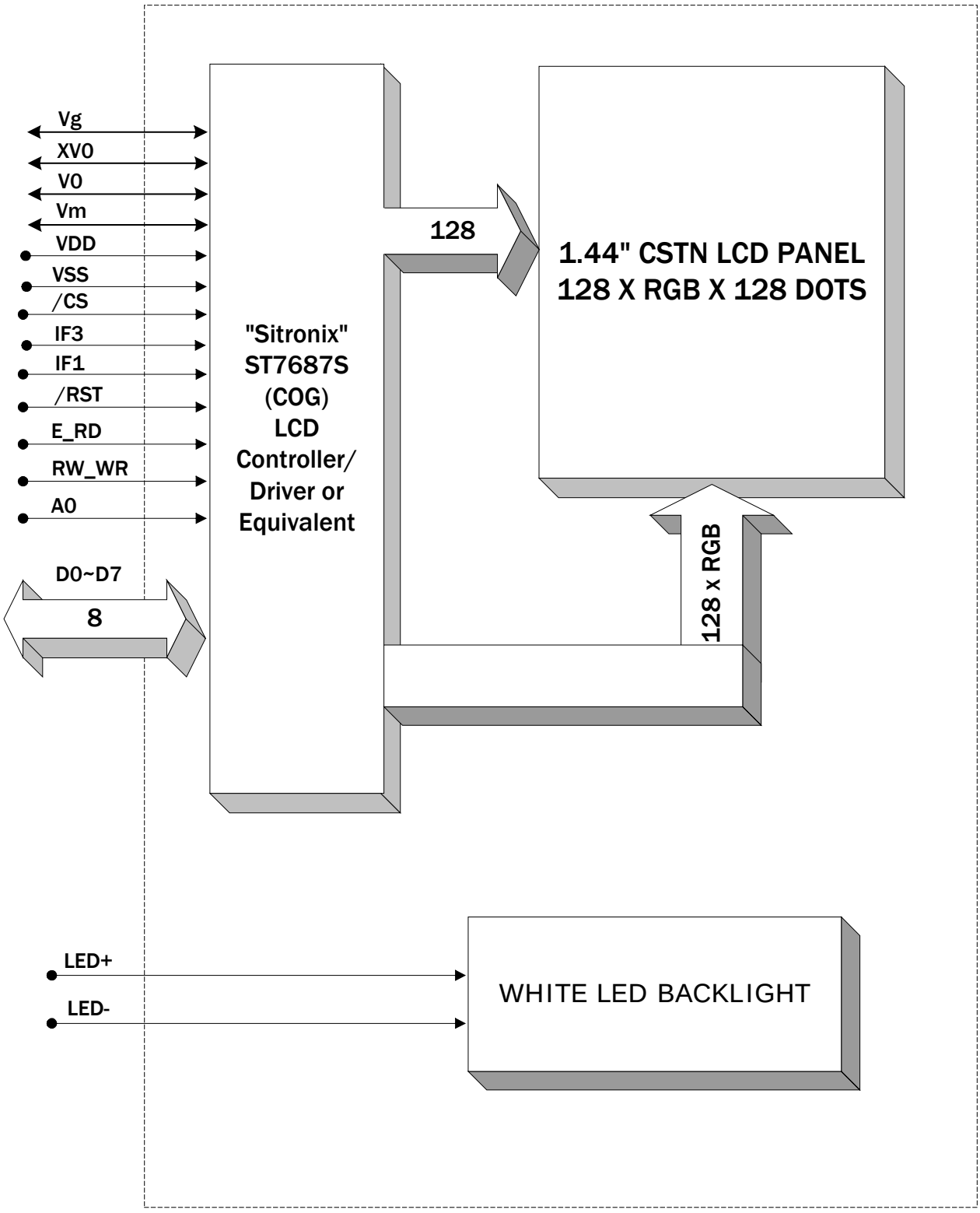


Figure 2: Block Diagram.

3. Interface signals

Table 2(a): Pin assignment

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>NC</td><td>No connection.</td></tr>
<tr><td>2</td><td>LED+</td><td>Anode of backlight input.</td></tr>
<tr><td>3</td><td>LED-</td><td>Cathode of backlight input.</td></tr>
<tr><td>4</td><td>Vg</td><td rowspan="2">Bias LCD driver supply voltages.
Vg_{OUT} is the output voltage of Vg generated by ST7687S.
Vg_{IN} is the input pin of power supply to generate Vg voltage for LCD.
Vg_S is the input pin of power supply to sense the Vg voltage.
Vg_{OUT}、Vg_{IN} & Vg_S should be connected together by FPC.
Vm is the I/O pin of LCD bias supply voltage.
Voltages should have the following relationship;
V0 ＞ Vg ＞ Vm ＞ VSS ＞ XV0.
VDDA-0.7V＞Vm＞0.7V , 2 x VDDA≧Vg＞1.8V
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><th>LCD bias</th><th>Vg</th><th>Vm</th><th>Note</th></tr>
<tr><td>1/N bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td><td>N= 5 to 12</td></tr>
</table></td></tr>
<tr><td>5</td><td>Vm</td></tr>
<tr><td>6</td><td>XV0</td><td>Negative LCD driver supply voltages.
$XV0_{OUT}$ is the output voltage of XV0 generated by ST7687S.
$XV0_{IN}$ is the input pin of power supply to generate XV0 voltage for LCD.
$XV0_S$ is the input pin of power supply to sense the XV0 voltage.
$XV0_{OUT}$、$XV0_{IN}$ & $XV0_S$ should be connected together by FPC.</td></tr>
<tr><td>7</td><td>V0</td><td>Positive LCD driver supply voltages.
$V0_{OUT}$ is the output voltage of V0 generated by ST7687S.
$V0_{IN}$ is the input pin of power supply to generate V0 voltage for LCD.
$V0_S$ is the input pin of power supply to sense the V0 voltage.
$V0_{OUT}$、$V0_{IN}$ & $V0_S$ should be connected together by FPC.</td></tr>
<tr><td>8</td><td>VDD</td><td>Power supply.</td></tr>
<tr><td>9</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>10</td><td>VDD</td><td>Power supply.</td></tr>
<tr><td>11</td><td>NC</td><td>No connection.</td></tr>
<tr><td>12</td><td>/CS</td><td>Chip select input pins.
Data / Instruction I/O is enabled only when /CS is "L".
When chip select is non-active, D0 to D7 become high impedance.</td></tr>
<tr><td>13</td><td>IF3</td><td rowspan="2">Parallel / Serial data input select input
<table>
<tr><th>IF3</th><th>IF1</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>68 series 8-bit parallel</td></tr>
</table></td></tr>
<tr><td>14</td><td>IF1</td></tr>
</table>

Table 2(b): Pin assignment

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>15</td><td>/RST</td><td>Reset input pin. When RST is “L”, initialization is executed.</td></tr>
<tr><td>16</td><td>E_RD</td><td>E_RD pin is only used in parallel interface.
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Enable clock pin:
Write status: The data on D0 to D7 are latched at the falling edge of the E signal.
Read status: The data on D0 to D7 are latched at the rising edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
The data on D0 to D7 are latched at the falling edge of the /RD signal.</td></tr>
</table></td></tr>
<tr><td>17</td><td>VDD</td><td>Power supply.</td></tr>
<tr><td>18</td><td>D7</td><td rowspan="8">Data pins.</td></tr>
<tr><td>19</td><td>D6</td></tr>
<tr><td>20</td><td>D5</td></tr>
<tr><td>21</td><td>D4</td></tr>
<tr><td>22</td><td>D3</td></tr>
<tr><td>23</td><td>D2</td></tr>
<tr><td>24</td><td>D1</td></tr>
<tr><td>25</td><td>D0</td></tr>
<tr><td>26</td><td>RW_WR</td><td>RW_WR pin is only used in parallel interface.
<table>
<tr><th>MPU Type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin.
Write status: RW = “L”.
Read status: RW = “H”.</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>27</td><td>A0</td><td>Register select input pin.
In parallel interface.
A0= “H”: D0 to D7 is display data.
A0= “L”: D0 to D7 is control command.</td></tr>
<tr><td>28</td><td>NC</td><td>No connection.</td></tr>
<tr><td>29</td><td>NC</td><td>No connection.</td></tr>
</table>

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage (2)	VDD	-0.3	+3.6	V
Supply Voltage (2)	VDD2,VDD3,VDD4,VDD5	-0.3	+3.6	V
Supply Voltage (3)	VLCD (V0-XV0)	-0.3	+18.0	V
Input voltage range	Vin	-0.3	VDD+0.5	V

Note: 1. The modules may be destroyed if they are used beyond the absolute maximum ratings.
2. Voltages are all based on VSS = 0V.
3. Voltage relationship: V0. Vg. Vm. VSS. XV0 must always be satisfied.

4.2 Environmental Conditions

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature (Ta)	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 2.8V, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VDD-VSS		-	2.8	-	V
Supply voltage (LCD)	VLCD	At Ta = -20 °C, VDD=2.8V, Note 1	-	TBD	-	V
		At Ta =25 °C, VDD=2.8V,Note 1	-	~14.0	-	V
		At Ta =70 °C, VDD=2.8V, Note 1	-	TBD	-	V
Input signal voltage	V_{IH}	"H" level	0.7VDD	-	VDD	V
	V_{IL}	"L" level	VSS	-	0.3VDD	V
Supply Current (Logic & LCD)	IDD		-	TBD	-	mA
Supply voltage of white LED backlight	VLED	Forward current =20mA Number of LED dies = 1	3.0	3.2	3.4	V
Luminance (on the backlight surface)			-	2200	-	cd/m^2

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

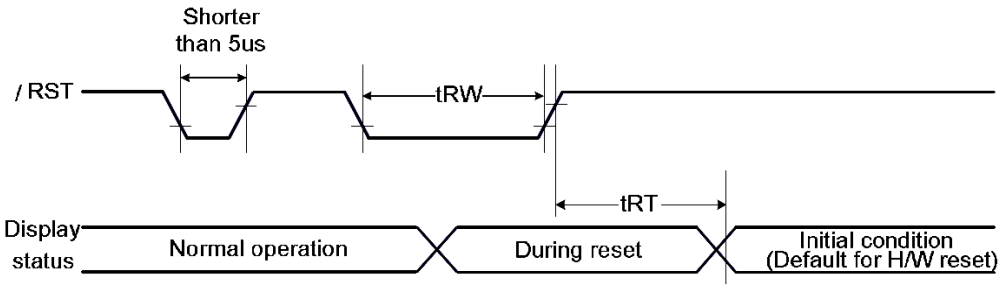
5.2 Timing Characteristics

5.2.1 Reset Timing

At Ta =-20 °C To +70 °C, VDD = 2.8V, VSS=0V.

Table 6

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset "L" pulse width	/RST	tRW		TBD	—	us
Reset time		tRT		TBD (*note 5)	—	ms
Reset time		tRT		TBD (*note 6,7)	—	ms

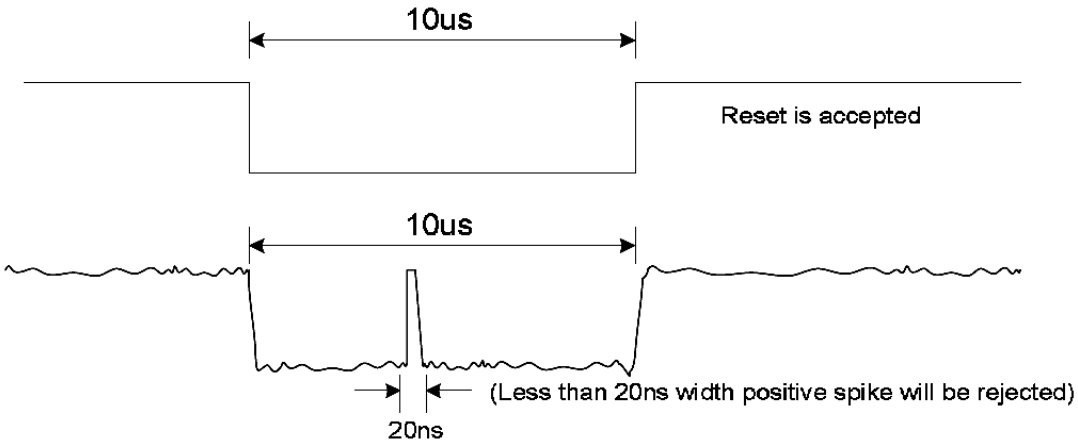


Notes:

1. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below:

RST Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

2. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
3. Spike Rejection also applies during a valid reset pulse as shown below:



4. When Reset applied during Sleep In Mode.
5. When Reset applied during Sleep Out Mode.
6. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.2.2 System Bus Read / Write Characteristics (8080-series MPU)

At Ta =-20 °C To +70 °C, VDD = 2.8V, VSS=0V.

Table 7

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		TBD	—	ns
Address setup time		tAW8		TBD	—	
System cycle time (WRITE)	WR	tCYC8		TBD	—	
/WR L pulse width (WRITE)		tCCLW		TBD	—	ns
/WR H pulse width (WRITE)		tCCHW		TBD	—	
System cycle time (READ)	RD (ID)	tCYC8	When read ID data	TBD	—	
/RD L pulse width (READ)		tCCLR		TBD	—	
/RD H pulse width (READ)		tCCHR		TBD	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	TBD	—	
/RD L pulse width (READ)		tCCLR		TBD	—	
/RD H pulse width (READ)		tCCHR		TBD	—	
WRITE data setup time	D0 to D7	tDS8		TBD	—	
WRITE data hold time		tDH8		TBD	—	
READ access time (ID)		tACC8 (ID)		—	TBD	
READ access time (FM)		tACC8 (FM)	CL = 100 pF	—	TBD	
READ Output disable time		tOH8	CL = 100 pF	—	TBD	

Note 1: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr+tf)≦(tCYC8-tCCLW-tCCHW) for (tr +tf)≦(tCYC8-tCCLR-tCCHR) are specified.

Note 2: All timing is specified using 20% and 80% of VDD as the reference.

Note 3: tCCLW and tCCLR are specified as the overlap between /CS being "L" and WR and RD being at the "L" level.

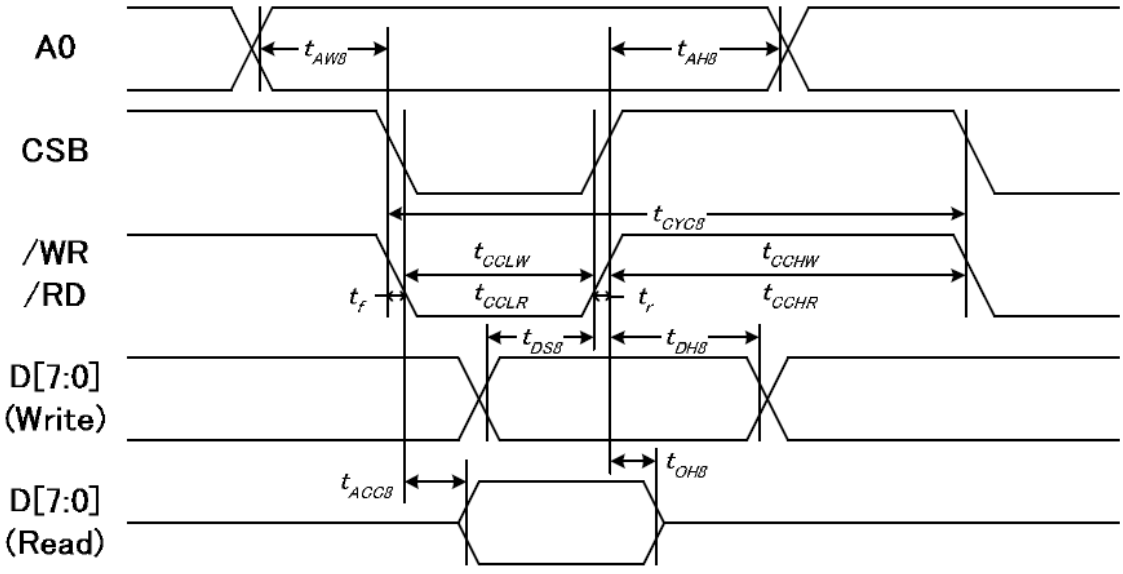


Figure 3: Parallel Interface Characteristics bus (8080-series MCU)

5.2.2 System Bus Read / Write Characteristics (6800-series MPU)

At Ta =-20 °C To +70 °C, VDD = 2.8V, VSS=0V.

Table 8

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		TBD	—	ns
Address setup time		tAW8		TBD	—	
System cycle time (WRITE)	E	tCYC8		TBD	—	
/WR L pulse width (WRITE)		tCCLW		TBD	—	ns
/WR H pulse width (WRITE)		tCCHW		TBD	—	
System cycle time (READ)	RD (ID)	tCYC8	When read ID data	TBD	—	
/RD L pulse width (READ)		tCCLR		TBD	—	
/RD H pulse width (READ)		tCCHR		TBD	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	TBD	—	
/RD L pulse width (READ)		tCCLR		TBD	—	
/RD H pulse width (READ)		tCCHR		TBD	—	
WRITE data setup time	D0 to D7	tDS8		TBD	—	
WRITE data hold time		tDH8		TBD	—	
READ access time (ID)		tACC8 (ID)		—	TBD	
READ access time (FM)		tACC8 (FM)	CL = 100 pF	—	TBD	
READ Output disable time		tOH8	CL = 100 pF	—	TBD	

Note 1: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr+tf)≦(tCYC6-tEWLW-tEWHW) for (tr+tf)≦(tCYC6-tEWLR-tEWHR) are specified.

Note 2: All timing is specified using 20% and 80% of VDD as the reference.

Note 3: tEWLW and tEWLR are specified as the overlap between /CS being "L" and E.

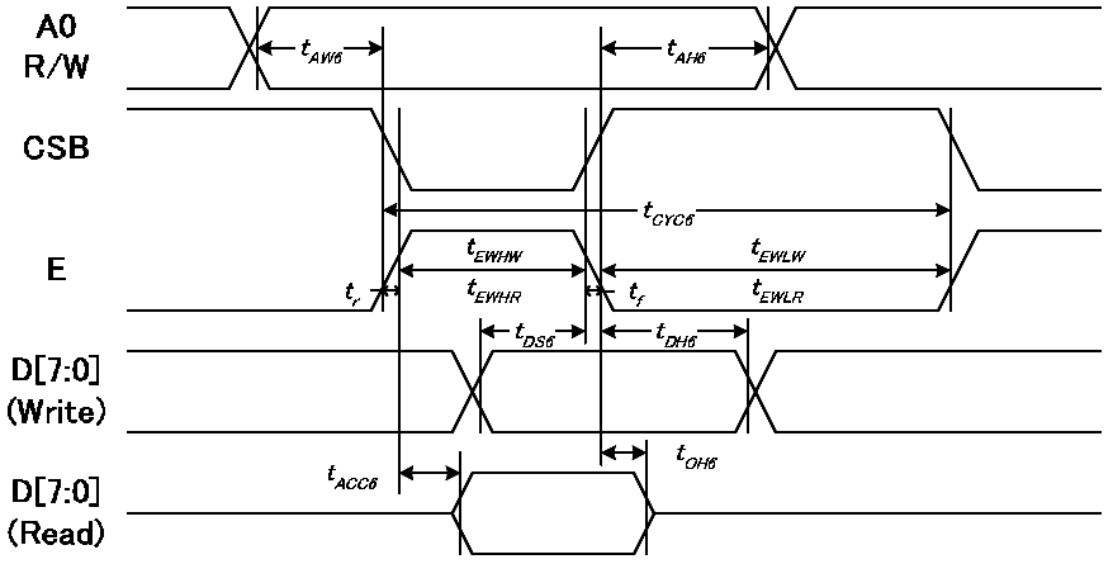


Figure 4: Parallel Interface Characteristics bus (6800-series MCU)

5.3 Power ON/OFF sequence

(TBD)

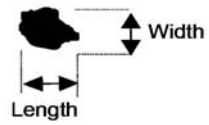
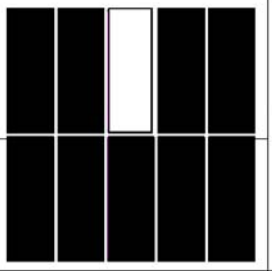
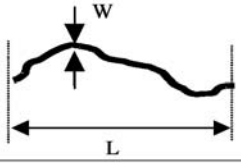
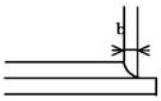
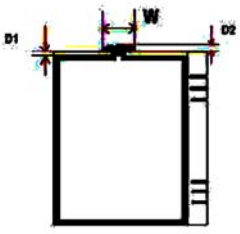
5.4 Power Flow Chart For Different Power Modes

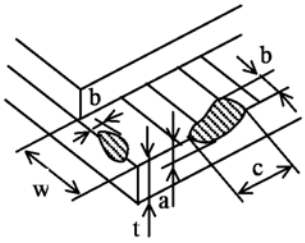
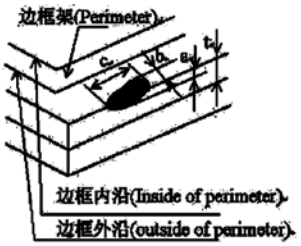
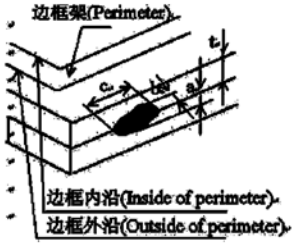
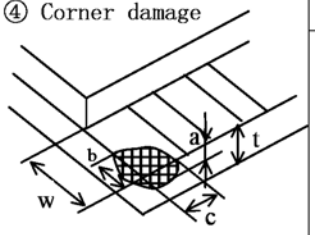
(TBD)

6. Electrical & Optical Characteristics

(TBD)

7. CSTN Panel Inspection Specifications

Failure mode	Illustration	Category(Unit: mm)		Acceptable count	
				Viewing area	non-Viewing area
Black spot White spot	 Φ= (Length+width)/2	A	Φ≦0.10	Not count	Not count
		B	0.10<Φ≦0.15	2, The gap between the two spots should be 5 mm and above.	
		C	0.15<Φ≦0.20	1	
		D	0.20<Φ	0	
Bright spot(Red spot,green spot and blue spot caused by damaged colour filter)		A	Area≦1 sub-pixel	1	N/A
Black line White line		A	W≦0.03	Not count	Not count
		B	0.03<W≦0.05, L≦3.0	2	
		C	0.05<W	Judged by spot spec	
Below are cosmetic inspection specifications					
Excess glass		b≤1.0, this defect shall not affect the outline dimension or assembly process.(Remarks: For COG process, the defect size is decided by the dimension of LCD panel.)			
		This defect shall not affect the outline dimension or assembly process.			
The depth of UV glue entered in LCD cell		a. D1≥0.2, not enter into viewing area b. D2≤0.8, c. W=End mouth width + (2~6 mm)			

<table>
<tr><td rowspan="6">Glass defect(scratch ,damage)</td><td>① LCD ledge damage
 
</td><td colspan="2">Category</td></tr>
<tr><td></td><td>A</td><td>The defect shall not affect the outline dimension or assembly process at non ITO zone.</td></tr>
<tr><td></td><td>B</td><td>b≦1/4w, a & c not count (at ITO zone)</td></tr>
<tr><td></td><td>C</td><td>Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td>② Outside of perimeter damage
 
</td><td colspan="2">b can't reach inside of perimeter.</td></tr>
<tr><td>③ Joint glass damage
 
</td><td colspan="2">b can't reach outside of perimeter or ITO layout.</td></tr>
<tr><td>④ Corner damage
 
</td><td>A</td><td>a ≦ t, b ≦ 3.0, c ≦ 3.0</td></tr>
<tr><td colspan="2">B. Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td colspan="4">Remark: a stands for thickness of damage, b for width, c for length and t for glass thickness. (Unit: mm)</td></tr>
</table>

8. Remark

HANDLING LCD AND LCD MODULES

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling:

(1) Keep the temperature within range for use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel-off or bubble generation. When storage for a long period over 40° C is required, the relative humidity should be kept below 60%.
(2) Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin. Never scrub hard.
(3) Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display
(4) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.
(5) PETROLEUM BENZIN is recommended to remove adhesives used to attach front/rear polarizers and reflectors, while chemicals like acetone, toluene, ethanol and isopropyl alcohol will cause damage to the polarizer. Avoid oil and fats. Avoid lacquer and epoxies which might contain solvents and hardeners to cause electrode errosion. Some solvents will also soften the epoxy covering the DIL pins and thereby weakening the adhesion of the epoxy on glass. This will cause the exposed electrodes to erode electrochemically when operating in high humidity and condensing environment.
(6) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.
(7) Do not drive LCD with DC voltage.
(8) When soldering DIL pins, avoid excessive heat and keep soldering temperature between 260°C to 300°C for no more than 5 seconds. Never use wave or reflow soldering.

2. Liquid Crystal Display Modules (MDL)

2.1 Mechanical Considerations

MDL's are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
(1) Do not tamper in any way with the tabs on the metal frame.
(2) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
(3) Do not touch the elastomer connector (conductive rubber), especially when inserting an EL panel.
(4) When mounting a MDL make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
(5) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.
(6) If FPCA need to be bent, please refer the suggested bending area on the specification. The stiffener and component area on FPC/FFC/COF must not be bent during or after assembly (Note: for those models with FPC/FFC/COF +stiffener).
(7) Sharp bending should be avoided on FPC to prevent track cracking.

2.2 Static Electricity

MDL contains CMOS LSI's and the same precaution for such devices should apply, namely:

(1) The operator should be grounded whenever he comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any part of the human body.
(2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
(3) Only properly grounded soldering irons should be used.
(4) If an electric screwdriver is used it should be well grounded and shielded from commutator sparks.
(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.
(6) Since dry air is inducive to statics, a relative humidity of 50 - 60% is recommended.

2.3 Soldering

(1) Solder only to the I/O terminals.
(2) Use only soldering irons with proper grounding and no leakage.
(3) Soldering temperature is 280°C ± 10°C .
(4) Soldering time: 3 to 4 seconds.
(5) Use eutectic solder with resin flux fill.
(6) If flux is used. the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.
(7) Use proper de-soldering methods (e.g. suction type desoldering irons) to remove lead wires from the I/O terminals when necessary. Do not repeat the soldering/ desoldering process more than three times as the pads and plated through holes may be damaged.

2.4 Label

Identification labels will be stuck on the module without obstructing the viewing area of display.

3. Operation

(1) The viewing angle can be adjusted by varying the LCD driving voltage Vo.
(2) Driving voltage should be kept within specified range, excess voltage shortens display life.
(3) Response time increases with decrease in temperature.
(4) Display may turn black or dark Blue at temperatures above its operational range; this is however not destructive and the display will return to normal once the temperature falls back to range.
(5) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured". They will recover once the display is turned off.
(6) Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.
(7) Display performance may vary out of viewing area. If there is any special requirement on performance out of viewing area, please consult Varitronix.

4. Storage and Reliability

(1) LCD's should be kept in sealed polyethylene bags while MDL's should use antistatic ones. If properly sealed, there is no need for desiccant.
(2) Store in dark places and do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C and the relative humidity low. Please consult VARITRONIX for other storage requirements.
(3) Water condensation will affect reliability performance of the display and is not allowed.
(4) Semi-conductor device on the display is sensitive to light and should be protected properly.
(5) Power up/down sequence.
   a) Power Up: in general, LCD supply voltage, Vo must be supplied after logic voltage, VDD becomes steady. Please refer to related IC data sheet for details.
   b) Power Down: in general, LCD supply voltage, Vo must be removed before logic voltage, VDD turns off. Please refer to related IC data sheet for details.

5. Safety

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all times.

LIMITED WARRANTY

VARITRONIX LCDs and modules are not consumer products, but may be incorporated by VARITRONIX's customers into consumer products or components thereof. VARITRONIX does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of VARITRONIX is limited to repair or replacement on the terms set forth below. VARITRONIX will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user.

   Unless otherwise agreed in writing between VARITRONIX and the customer, VARITRONIX will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with VARITRONIX LCD Acceptance Standards (copies available on request), for a period of one year from the date of shipment. Confirmation of such date shall be based on freight documents.

2. No warranty can be granted if any of the precautions stated in HANDLING LCD and LCD Modules above have been disregarded. Broken glass, scratches on polarizers, mechanical damages as well as defects that are caused by accelerated environmental tests are excluded from warranty.
3. In returning the LCD and Modules, they must be properly packaged and there should be detailed description of the failures or defects.

IMPORTANT NOTICE

The information presented in this document has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies. VARITRONIX reserves the right to make changes to any specifications without further notice for performance, reliability, production technique and other considerations, VARITRONIX does not assume any liability arising out of the application or use of products herein. Please see Limited Warranty in the previous section.