SX Instruction Set Summary

Instruction		Affects	W	C
ADD	fr,W	fr C DC Z	1	1
ADD	fr1,[#lit|fr2]	fr1 W C DC Z	2	2
ADD	W,fr	W C DC Z	1	1
ADDB	fr,{/}op.bit	fr Z	2	2
AND	fr,W	fr Z	1	1
AND	fr1,[#lit|fr2]	fr1 W Z	2	2
AND	W,[#lit|fr]	W Z	1	1
BANK	fr	FSR	1	1
CALL	addr8	PC	1	3
CJA	fr1,[#lit|fr2],addr9	W C DC Z	4	4|6
CJAE	fr1,[#lit|fr2],addr9	W C DC Z	4	4|6
CJB	fr1,[#lit|fr2],addr9	W C DC Z	4	4|6
CJBE	fr1,[#lit|fr2],addr9	W C DC Z	4	4|6
CJE	fr1,[#lit|fr2],addr9	W C DC Z	4	4|6
CJNE	fr1,[#lit|fr2],addr9	W C DC Z	4	4|6
CLC		C	1	1
CLR	[fr|W|!WDT]	Z[fr|W|(*1)]	1	1
CLRB	op.bit	op.bit	1	1
CLZ		Z	1	1
CSA	fr1,[#lit|fr2]	W C DC Z	3	3|4
CSAE	fr1,[#lit|fr2]	W C DC Z	3	3|4
CSB	fr1,[#lit|fr2]	W C DC Z	3	3|4
CSBE	fr1,[#lit|fr2]	W C DC Z	3	3|4
CSE	fr1,[#lit|fr2]	W C DC Z	3	3|4
CSNE	fr1,[#lit|fr2]	W C DC Z	3	3|4
DEC	fr	fr Z	1	1
DECSZ	fr	fr PC	1	1
DJNZ	fr,addr9	fr Z PC	2	2|4
IJNZ	fr,addr9	fr Z PC	2	2|4
INC	fr	fr Z	1	1
INCSZ	fr	fr PC	1	1
IREAD		M W	1	4
JB	op.bit,addr9	PC	2	2|4
JC	addr9	PC	2	2|4
JMP	[addr9,W]	PC	1	3
JMP	[W|PC+W]	PC	1	3
JNB	op.bit,addr9	PC	2	2|4
JNC	addr9	PC	2	2|4
JNZ	addr9	PC	2	2|4
JZ	addr9	PC	2	2|4
MODE	lit	M	1	1
MOV	fr,W	fr	1	1
MOV	fr1,[#lit|fr2]	fr1 [W|W Z]	2	2
MOV	fr,M	fr W	2	2
MOV	W,{/|++|--}fr	W Z	1	1
MOV	W,{/|<<|>>}fr	W C	1	1
MOV	W,<>fr	W	1	1
MOV	W,fr-W	W C DC Z	1	1
MOV	W,[#lit|M]	W	1	1
MOV	M,fr	W M Z	2	2
MOV	M,[#lit|W]	M	1	1
MOV	!OPTION,[fr,#lit]	W [Z Opt|Opt]	2	2
MOV	!OPTION,W	Opt	1	1
MOV	!port,[fr,#lit]	[W Z !port]	2	2
MOV	!port,W	W !port [Z|-]	1	1
MOVB	op1.bit,{/}op2.bit	op1.bit	4	4

SX Instruction Set Summary (continued)

Instruction		Affects	W	C
MOVSZ	W, [++fr |-- fr]	W PC	1	1|4
NOP		none	1	1
NOT	[fr|W]	[fr|W] Z	1	1
OR	fr,W	fr Z	1	1
OR	fr1,[#lit|fr2]	fr1 W Z	2	2
OR	W,[fr, #lit]	W Z	1	1
PAGE	addr12	PAx	1	1
RET		PC	1	3
RETI		(*2)	1	3
RETIW		(*2) RTCC	1	3
RETP		PAx, PC	1	3
RETW	#lit{,#lit…}	PC W	x	3*x
RL	fr	fr C	1	1
RR	fr	fr C	1	1
SB	op.bit	PC	1	1|2
SC		PC	1	1|2
SETB	op.bit	op.bit	1	1
SKIP		PC	1	2
SLEEP		WDT TO PD	1	1
SNB	op.bit	PC	1	1|2
SNC		PC	1	1|2
SNZ		PC	1	1|2
STC		C	1	1
STZ		Z	1	1
SUB	fr1,[#lit|fr2]	fr1 W C DC Z	2	2
SUB	fr,W	fr C DC Z	1	1
SUBB	fr,{/}op.bit	fr Z	2	2
SWAP	fr	fr	1	1
SZ		PC	1	1|2
TEST	[fr|W]	Z	1	1
XOR	fr1,[#lit|fr2]	fr1 W Z	2	2
XOR	fr,W	fr Z	1	1
XOR	W,[fr|#lit]	W Z	1	1
Column **W**: Number of instruction words				
Column **C**: Number of clock cycles				
(*1) Resets the watchdog timer				
(*2) Restores PC, W, STATUS, FSR (and MODE on SX48)				

MODE and Port Control Reg. Access (SX20/28)

MODE	mov !RA,W	mov !RB,W	mov !RC,W
$08	n.a.	CMP (*1)	n.a
$09	n.a.	WKPND (*2)	n.a
$0a	n.a.	WKED	n.a
$0b	n.a.	WKEN	n.a
$0c	n.a.	ST	ST
$0d	LVL	LVL	LVL
$0e	PLP	PLP	PLP
$0f	DIR	DIR	DIR
(*1) Exchanges W and the CMP register contents			
(*2) Exchanges W and the WKPND_B register contents			
Reset default for MODE register is $0f (DIR)			

MODE and Port Control Reg. Access (SX48)

MODE	mov !RA, W	mov !R[B|C|D|E], W
$0c	n.a.	Read ST_[B|C|D|E]
$0d	Read LVL_A	Read LVL_[B|C|D|E]
$0e	Read PLP_A	Read PLP_[B|C|D|E]
$0f	Read DIR_A	Read DIR_[B|C|D|E]
$1c	n.a.	Write ST_[B|C|D|E]
$1d	Write LVL_A	Write LVL_[B|C|D|E]
$1e	Write PLP_A	Write PLP_[B|C|D|E]
$1f	Write DIR_A	Write DIR_[B|C|D|E]
MODE	**mov !RB, W**	**mov !RC, W**
$00	Read T1CPL	Read T2CPL
$01	Read T1CPH	Read T2CPH
$02	Read T1R2CML	Read T2R2CML
$03	Read T1R2CMH	Read T2R2CMH
$04	Read T1R1CML	Read T2R1CML
$05	Read T1R1CMH	Read T2R1CMH
$06	Read T1CNTB	Read T2CNTB
$07	Read T1CNTA	Read T2CNTA
$08	CMP_B←→W	n.a.
$09	WKPND_B←→W	n.a.
$0a	Write WKED_B	n.a.
$0b	Write WKEN_B	n.a.
$10	Clear Timer T1	Clear Timer T2
$11	n.a.	n.a.
$12	Write T1R2CML	Write T2R2CML
$13	Write T1R2CMH	Write T2R2CMH
$14	Write T1R1CML	Write T2R1CML
$15	Write T1R1CMH	Write T2R1CMH
$16	Write T1CNTB	Write T2CNTB
$17	Write T1CNTA	Write T2CNTA
$18	CMP_B←→W	n.a.
$19	WKPND_B←→W	n.a.
$1a	Write WKED_B	n.a.
$1b	Write WKEN_B	n.a.
Reset default for MODE register is $1f (DIR)		

OPTION Register

RTW	RTE_IE	RTS	RTE_ES	PSA	PS2	PS1	PS0
Bit 7							Bit 0

7 RTW	0 = Register 01 addresses W, 1 = RTCC
6 RTE_IE	0 = RTCC rollover interrupt enabled, 1 = disabled
5 RTS	0 = RTCC increments on internal instr. cycle, 1 = RTCC increments on RTCC input transition
4 RTE_ES	0 = RTCC increments on rising edges on RTCC pin 1 = RTCC increments on falling edges on RTCC pin
3 PSA	0 = Prescaler assigned to RTCC 1 = Prescaler assigned to Watchdog timer
2 PS2	Prescaler divider setting
1 PS1	1:2 … 1:256 for RTCC, 1:1…1:128 for WDT
0 PS0	WD timeout: 0.016 … 2.0 seconds

Port Configuration registers		
Name	Meaning	Def.
DIR	Direction 0 = Out, 1 = In (high-Z)	1
PLP	Weak Pull-Up 0 = Pull-Up, 1 = off	1
LVL	Threshold Level 0 = CMOS, 1 = TTL	1
ST (*1)	Schmitt Trigger inputs 0 = enabled, 1 = disabled	1
WKEN (*2)	0 = Interrupt/Wakeup enabled 1 = disabled	1
WKED (*2)	0 = rising, 1 = falling edge	1
WKPND (*2)	Wakeup Pending (Edge-Detect) Bits. MOV !RB, w exchanges the contents of W and WKPND.	0
CMP (*2)	Comparator Bit 7: 0 = enabled, 1 = disabled Bit 6: 0 = Result on RB0, 1 = off MOV !RB, W exchanges the contents of W and CMP.	1
Remarks	Each bit in a configuration register controls the function of its associated port bit. Set the MODE register to select any of the configuration register sets (see tables on opposite side).	
(*1)	Not available on port RA	
(*2)	Only available on port RB	

STATUS Register							
PA2	PA1	PA0	TO	PD	Z	DC	C
Bit 7							Bit 0

7-5: Program memory page select bits
4: Time Out bit
1 on power up, CLR !WDT, or SLEEP
0 on watchdog time-out
3: Power Down bit
1 on power up and on CLR !WDT
0 on SLEEP
2: Zero Bit (Z) (affected by many logical, arithmetic and data movement instructions
1 = result is zero
0 = result is <> zero
1: Digit Carry (DC)
After Addition: 1 = carry from bit 3 occurred
0 = no carry from bit 3
After Subtract.: 1 = no borrow from bit 3
0 = borrow from bit 3 occurred
0: Carry (C)
After Addition: 1 = carry from bit 7 of the result
0 = no carry from bit 7
After Subtract.: 1 = no borrow from bit 7 of the result
0 = borrow from bit 7 occurred

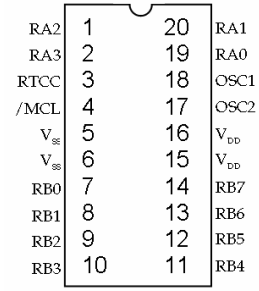
Bank 0 Memory Map		
Addr.	Name	Meaning
$00	IND(F)	This address actually refers to the register whose address is currently contained in the FSR
$01	RTCC/ WREG	When OPTION.7 (RTW) is 1, the RTCC is mapped here, else the W register.
$02	PC	Lower 8 bits of the internal program counter
$03	STATUS	Status register (see separate table)
$04	FSR	Used to indirectly address a register, or to select a register bank (upper 4 bits for SX48/52, upper 3 bits for other SX types
$05	RA	I/O port A
$06	RB	I/O port B
$07	RC / fr7	I/O port C (not available on the SX20, can be used as general purpose register)
$08	RD /fr8	I/O port D (only available on the SX48/52, can be used as general purpose register on other types)
$09	RE / fr9	I/O port E (only available on the SX48/52, can be used as general purpose register on other types)
$0A… $0F	General purpose registers. Registers in Bank 0 (special function, and general purpose) can always be accessed, independently of the current bank selected by the upper FSR bits.	

Notes:

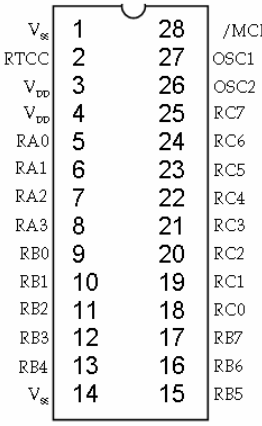
The SX Quick-Reference Card

Author: Günther Daubach, 2007

SX Pin-Assignments



SX20AC/SS



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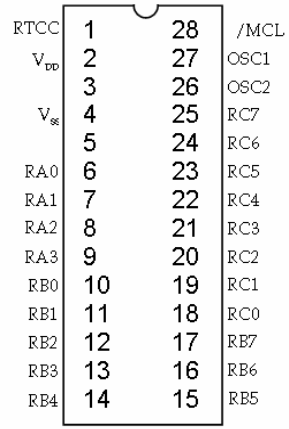
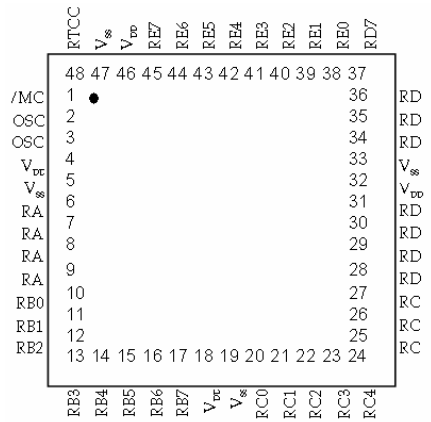


SC28AC/DP



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