

LM139/LM239/LM339 A Quad of Independently Functioning Comparators

National Semiconductor
Application Note 74
January 1973



INTRODUCTION

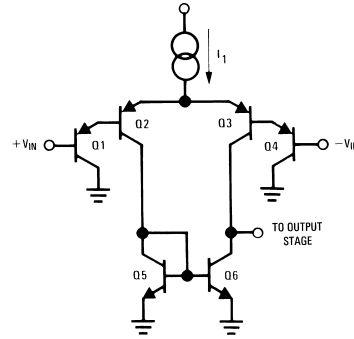
The LM139/LM239/LM339 family of devices is a monolithic quad of independently functioning comparators designed to meet the needs for a medium speed, TTL compatible comparator for industrial applications. Since no antisaturation clamps are used on the output such as a Baker clamp or other active circuitry, the output leakage current in the OFF state is typically 0.5 nA. This makes the device ideal for system applications where it is desired to switch a node to ground while leaving it totally unaffected in the OFF state.

Other features include single supply, low voltage operation with an input common mode range from ground up to approximately one volt below V_{CC} . The output is an uncommitted collector so it may be used with a pull-up resistor and a separate output supply to give switching levels from any voltage up to 36V down to a $V_{CE\ SAT}$ above ground (approx. 100 mV), sinking currents up to 15 mA. In addition it may be used as a single pole switch to ground, leaving the switched node unaffected while in the OFF state. Power dissipation with all four comparators in the OFF state is typically 4 mW from a single 5V supply (1 mW/comparator).

CIRCUIT DESCRIPTION

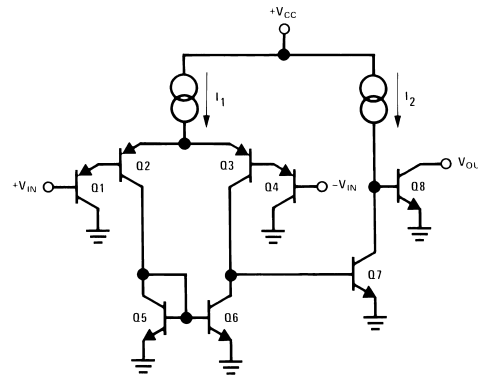
Figure 1 shows the basic input stage of one of the four comparators of the LM139. Transistors Q_1 through Q_4 make up a PNP Darlington differential input stage with Q_5 and Q_6 serving to give single-ended output from differential input with no loss in gain. Any differential input at Q_1 and Q_4 will be amplified causing Q_6 to switch OFF or ON depending on input signal polarity. It can easily be seen that operation with an input common mode voltage of ground is possible. With both inputs at ground potential, the emitters of Q_1 and Q_4 will be at one V_{BE} above ground and the emitters of Q_2 and Q_3 at $2 V_{BE}$. For switching action the base of Q_5 and Q_6 need only go to one V_{BE} above ground and since Q_2 and Q_3 can operate with zero volts collector to base, enough voltage is present at a zero volt common mode input to insure comparator action. The bases should not be taken more than several hundred millivolts below ground; however, to prevent forward biasing a substrate diode which would stop all comparator action and possibly damage the device, if very large input currents were provided.

Figure 2 shows the comparator with the output stage added. Additional voltage gain is taken through Q_7 and Q_8 with the collector of Q_8 left open to offer a wide variety of possible applications. The addition of a large pull-up resistor from the collector of Q_8 to either $+V_{CC}$ or any other supply up to 36V both increases the LM139 gain and makes possible output switching levels to match practically any application. Several outputs may be tied together to provide an ORing function or the pull-up resistor may be omitted entirely with the comparator then serving as a SPST switch to ground.



AN007385-1

FIGURE 1. Basic LM139 Input Stage

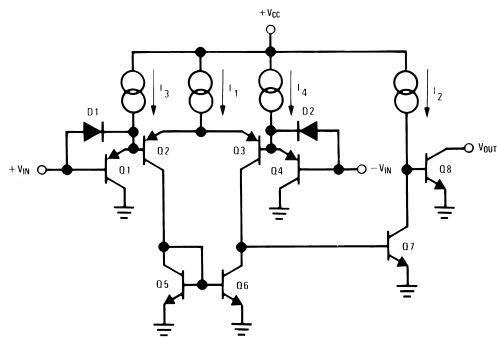


AN007385-2

FIGURE 2. Basic LM139 Comparator

Output transistor Q_8 will sink up to 15 mA before the output ON voltage rises above several hundred millivolts. The output current sink capability may be boosted by the addition of a discrete transistor at the output.

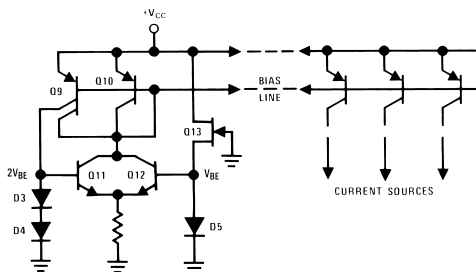
The complete circuit for one comparator of the LM139 is shown in Figure 3. Current sources I_3 and I_4 are added to help charge any parasitic capacitance at the emitters of Q_1 and Q_4 to improve the slew rate of the input stage. Diodes D_1 and D_2 are added to speed up the voltage swing at the emitters of Q_1 and Q_2 for large input voltage swings.



AN007385-3

FIGURE 3. Complete LM139 Comparator Circuit

Biasing for current sources I_1 through I_4 is shown in *Figure 4*. When power is first applied to the circuit, current flows through the JFET Q_{13} to bias up diode D_5 . This biases transistor Q_{12} which turns ON transistors Q_9 and Q_{10} by allowing a path to ground for their base and collector currents.



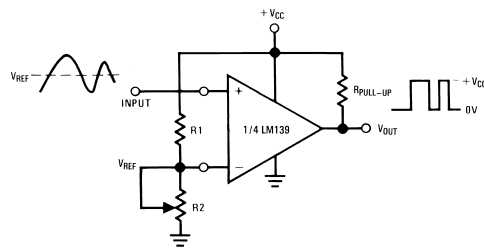
AN007385-4

FIGURE 4. Current Source Biasing Circuit

Current from the left hand collector of Q_9 flows through diodes D_3 and D_4 bringing up the base of Q_{11} to $2 V_{BE}$ above ground and the emitters of Q_{11} and Q_{12} to one V_{BE} . Q_{12} will then turn OFF because its base emitter voltage goes to zero. This is the desired action because Q_9 and Q_{10} are biased ON through Q_{11} , D_3 and D_4 so Q_{12} is no longer needed. The "bias line" is now sitting at a V_{BE} below $+V_{CC}$ which is the voltage needed to bias the remaining current sources in the LM139 which will have a constant bias regardless of $+V_{CC}$ fluctuations. The upper input common mode voltage is V_{CC} minus the saturation voltage of the current sources (approximately 100 mV) minus the $2 V_{BE}$ of the input devices Q_1 and Q_2 (or Q_3 and Q_4).

COMPARATOR CIRCUITS

Figure 5 shows a basic comparator circuit for converting low level analog signals to a high level digital output. The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. Resistors R_1 and R_2 are used to set the input threshold trip voltage (V_{REF}) at any value desired within the input common mode range of the comparator.



AN007385-5

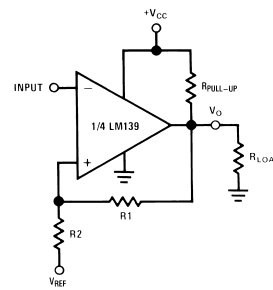
FIGURE 5. Basic Comparator Circuit

COMPARATORS WITH HYSTERESIS

The circuit shown in *Figure 5* suffers from one basic drawback in that if the input signal is a slowly varying low level signal, the comparator may be forced to stay within its linear region between the output high and low states for an undesirable length of time. If this happens, it runs the risk of oscillating since it is basically an uncompensated, high gain op amp. To prevent this, a small amount of positive feedback or hysteresis is added around the comparator. *Figure 6* shows a comparator with a small amount of positive feedback. In order to insure proper comparator action, the components should be chosen as follows:

$$R_{PULL-UP} < R_{LOAD} \text{ and} \\ R_1 > R_{PULL-UP}$$

This will insure that the comparator will always switch fully up to $+V_{CC}$ and not be pulled down by the load or feedback. The amount of feedback is chosen arbitrarily to insure proper switching with the particular type of input signal used. If the output swing is 5V, for example, and it is desired to feedback 1% or 50 mV, then $R_1 \approx 100 R_2$. To describe circuit operation, assume that the inverting input goes above the reference input ($V_{IN} > V_{REF}$). This will drive the output, V_O , towards ground which in turn pulls V_{REF} down through R_1 . Since V_{REF} is actually the noninverting input to the comparator, it too will drive the output towards ground insuring the fastest possible switching time regardless of how slow the input moves. If the input then travels down to V_{REF} , the same procedure will occur only in the opposite direction insuring that the output will be driven hard towards $+V_{CC}$.



AN007385-6

FIGURE 6. Comparator with Positive Feedback to Improve Switching Time

Putting hysteresis in the feedback loop of the comparator has far more use, however, than simply as an oscillation suppressor. It can be made to function as a Schmitt trigger with presettable trigger points. A typical circuit is shown in *Figure 7*. Again, the hysteresis is achieved by shifting the reference voltage at the positive input when the output voltage V_O changes state. This network requires only three resistors and is referenced to the positive supply $+V_{CC}$ of the comparator. This can be modeled as a resistive divider, R_1 and R_2 , between $+V_{CC}$ and ground, with the third resistor, R_3 , alternately connected to $+V_{CC}$ or ground, paralleling either R_1 or R_2 . To analyze this circuit, assume that the input voltage, V_{IN} , at the inverting input is less than V_{A1} . With $V_{IN} \leq V_{A1}$ the output will be high ($V_O = +V_{CC}$). The upper input trip voltage, V_{A1} , is defined by:

$$V_{A1} = \frac{+V_{CC} R_2}{(R_1 \parallel R_3) + R_2}$$

or

$$V_{A1} = \frac{+V_{CC} R_2 (R_1 + R_3)}{R_1 R_2 + R_1 R_3 + R_2 R_3} \quad (1)$$

When the input voltage V_{IN} , rises above the reference voltage ($V_{IN} > V_{A1}$), voltage, V_O , will go low ($V_O = \text{GND}$). The lower input trip voltage, V_{A2} , is now defined by:

$$V_{A2} = \frac{+V_{CC} R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$

or

$$V_{A2} = \frac{+V_{CC} R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3} \quad (2)$$

When the input voltage, V_{IN} , decreases to V_{A2} or lower, the output will again switch high. The total hysteresis, ΔV_A , provided by this network is defined by:

$$\Delta V_A = V_{A1} - V_{A2}$$

or, subtracting equation 2 from equation 1

$$\Delta V_A \Delta \frac{+V_{CC} R_1 R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3} \quad (3)$$

To insure that V_O will swing between $+V_{CC}$ and ground, choose:

$$R_{\text{PULL-UP}} < R_{\text{LOAD}} \quad \text{and} \quad (4)$$

$$R_3 > R_{\text{PULL-UP}} \quad (5)$$

Heavier loading on $R_{\text{PULL-UP}}$ (i.e. smaller values of R_3 or R_{LOAD}) simply reduces the value of the maximum output voltage thereby reducing the amount of hysteresis by lowering the value of V_{A1} . For simplicity, we have assumed in the above equations that V_O high switches all the way up to $+V_{CC}$.

To find the resistor values needed for a given set of trip points, we first divide equation (3) by equation (2). This gives us the ratio:

$$\frac{\Delta V_A}{V_{A2}} = \frac{1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}}{1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}} \quad (6)$$

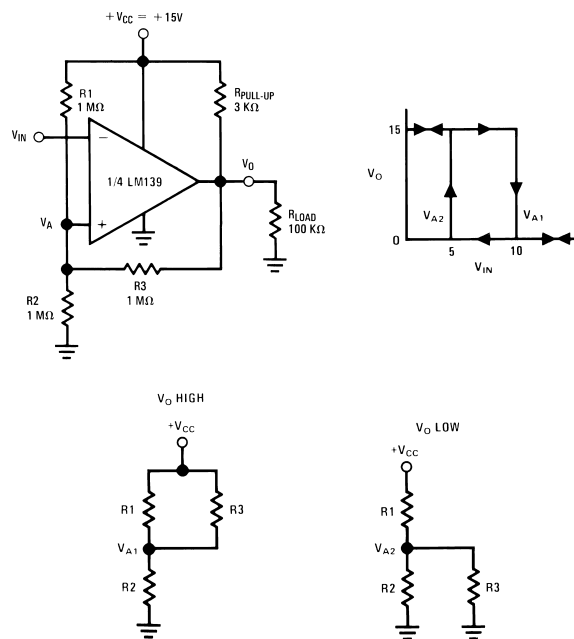


FIGURE 7. Inverting Comparator with Hysteresis

If we let $R_1 = n R_3$, equation (6) becomes:

$$\frac{\Delta V_A}{V_{A2}} = n \quad (7)$$

We can then obtain an expression for R_2 from equation (1) which gives

$$R_2 = \frac{R_1 \parallel R_3}{\frac{+V_{CC}}{V_{A1}} - 1} \quad (8)$$

The following design example is offered:

Given: $V^* = +15V$

$$R_{LOAD} = 100 \text{ k}\Omega$$

$$V_{A1} = +10V$$

$$V_{A2} = +5V$$

To find: $R_1, R_2, R_3, R_{PULL-UP}$

Solution:

From equation (4) $R_{PULL-UP} < R_{LOAD}$

$$R_{PULL-UP} < 100 \text{ k}\Omega$$

so let $R_{PULL-UP} = 3 \text{ k}\Omega$

From equation (5) $R_3 > R_{LOAD}$

$$R_3 > 100 \text{ k}\Omega$$

so let $R_3 = 1 \text{ M}\Omega$

$$\text{From equation (7)} \quad n = \frac{\Delta V_A}{V_{A2}} = \frac{10 - 5}{5} = 1$$

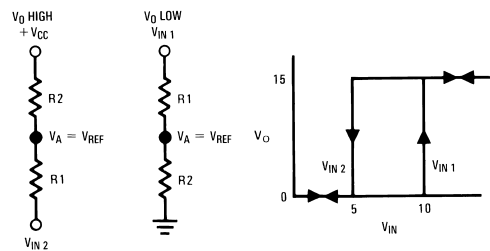
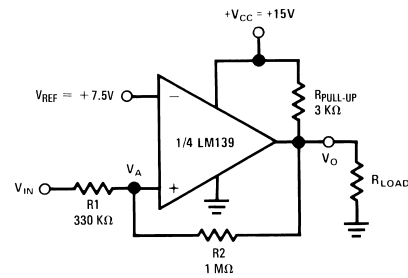
and since $R_1 = n R_3$

this gives $R_1 = 1 R_3 = 1 \text{ M}\Omega$

$$\text{From equation (8)} \quad R_2 = \frac{500 \text{ k}\Omega}{\frac{15}{10} - 1} = 1 \text{ M}\Omega$$

These are the values shown in *Figure 7*.

The circuit shown in *Figure 8* is a non-inverting comparator with hysteresis which is obtained with only two resistors, R_1 and R_2 . In contrast to the first method, however, this circuit requires a separate reference voltage at the negative input. The trip voltage, V_{A1} , at the positive input is shifted about V_{REF} as V_O changes between $+V_{CC}$ and ground.



AN007385-8

FIGURE 8. Non-Inverting Comparator with Hysteresis

Again for analysis, assume that the input voltage, V_{IN} , is low so that the output, V_O , is also low ($V_O = \text{GND}$). For the output to switch, V_{IN} must rise up to $V_{IN 1}$ where $V_{IN 1}$ is given by:

$$V_{IN 1} = \frac{V_{REF} (R_1 + R_2)}{R_2} \quad (9)$$

As soon as V_O switches to $+V_{CC}$, V_A will step to a value greater than V_{REF} which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN 1}) R_1}{R_1 + R_2} \quad (10)$$

To make the comparator switch back to its low state ($V_O = \text{GND}$) V_{IN} must go below V_{REF} before V_A will again equal V_{REF} . This lower trip point is now given by:

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (11)$$

The hysteresis for this circuit, ΔV_{IN} , is the difference between V_{IN1} and V_{IN2} and is given by:

$$\Delta V_{IN} = V_{IN1} - V_{IN2} = \frac{V_{REF}(R_1 + R_2)}{R_2} - \frac{V_{REF}(R_1 + R_2) - V_{CC}R_1}{R_2}$$

or

$$\Delta V_{IN} = \frac{V_{CC}R_1}{R_2} \quad (12)$$

As a design example consider the following:

$$\begin{aligned} \text{Given: } R_{LOAD} &= 100 \text{ k}\Omega \\ V_{IN1} &= 10 \text{ V} \\ V_{IN2} &= 5 \text{ V} \\ +V_{CC} &= 15 \text{ V} \end{aligned}$$

To find: V_{REF} , R_1 , R_2 and R_3

Solution:

Again choose $R_{PULL-UP} < R_{LOAD}$ to minimize loading, so let

$$R_{PULL-UP} = 3 \text{ k}\Omega$$

From equation (12)

$$\begin{aligned} \frac{R_1}{R_2} &= \frac{\Delta V_{IN}}{V_{CC}} \\ \frac{R_1}{R_2} &= \frac{10 - 5}{15} = \frac{1}{3} \\ R_1 &= \frac{R_2}{3} \end{aligned}$$

From equation (9)

$$\begin{aligned} V_{REF} &= \frac{10}{1 + \frac{R_1}{R_2}} \\ V_{REF} &= \frac{V_{IN}}{1 + \frac{1}{3}} = 7.5 \text{ V} \end{aligned}$$

To minimize output loading choose

$$R_2 > R_{PULL-UP}$$

or

$$R_2 > 3 \text{ k}\Omega$$

so let

$$R_2 = 1 \text{ M}\Omega$$

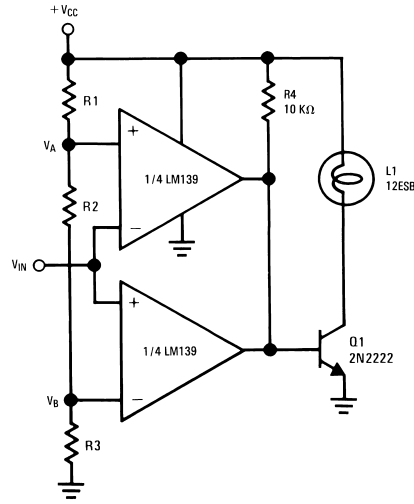
The value of R_1 is now obtained from equation (12)

$$\begin{aligned} R_1 &= \frac{R_2}{3} \\ R_1 &= \frac{1 \text{ M}\Omega}{3} \approx 330 \text{ k}\Omega \end{aligned}$$

These are the values shown in *Figure 8*.

LIMIT COMPARATOR WITH LAMP DRIVER

The limit comparator shown in *Figure 9* provides a range of input voltages between which the output devices of both LM139 comparators will be OFF.



AN007385-9

FIGURE 9. Limit Comparator with Lamp Driver

This will allow base current for Q_1 to flow through pull-up resistor R_4 , turning ON Q_1 , which lights the lamp. If the input voltage, V_{IN} , changes to a value greater than V_A or less than V_B , one of the comparators will switch ON, shorting the base of Q_1 to ground, causing the lamp to go OFF. If a PNP transistor is substituted for Q_1 (with emitter tied to $+V_{CC}$) the lamp will light when the input is above V_A or below V_B . V_A and V_B are arbitrarily set by varying resistors R_1 , R_2 and R_3 .

ZERO CROSSING DETECTOR

The LM139 can be used to symmetrically square up a sine wave centered around zero volts by incorporating a small amount of positive feedback to improve switching times and centering the input threshold at ground (see *Figure 10*). Voltage divider R_4 and R_5 establishes a reference voltage, V_1 , at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5 , the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$. The positive feedback resistor, R_6 , is made very large with respect to R_5 ($R_6 = 2000 R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10 \text{ mV}$) but it is sufficient to insure rapid output voltage transitions. Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately -100 mV . As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately -700 mV . This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1 .

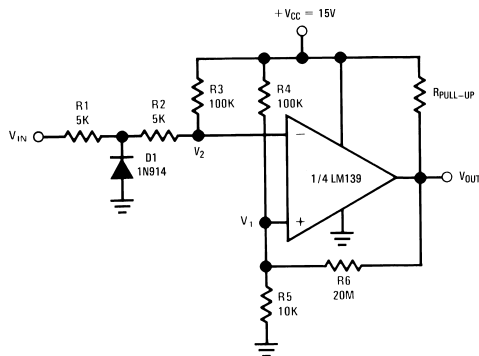


FIGURE 10. Zero Crossing Detector

COMPARING THE MAGNITUDE OF VOLTAGES OF OPPOSITE POLARITY

The comparator circuit shown in Figure 11 compares the magnitude of two voltages, V_{IN1} and V_{IN2} which have opposite polarities. The resultant input voltage at the minus input terminal to the comparator, V_A , is a function of the voltage divider from V_{IN1} and V_{IN2} and the values of R_1 and R_2 . Diode connected transistor Q_1 provides protection for the minus input terminal by clamping it at several hundred millivolts below ground. A 2N2222 was chosen over a 1N914 diode because of its lower diode voltage. If desired, a small amount of hysteresis may be added using the techniques described previously. Correct magnitude comparison can be seen as follows: Let V_{IN1} be the input for the positive polarity input voltage and V_{IN2} the input for the negative polarity. If the magnitude of V_{IN1} is greater than that of V_{IN2} the output will go low ($V_{OUT} = \text{GND}$). If the magnitude of V_{IN1} is less than that of V_{IN2} , however, the output will go high ($V_{OUT} = V_{CC}$).

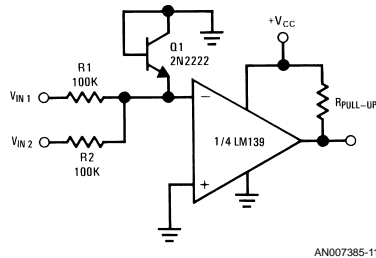


FIGURE 11. Comparing the Magnitude of Voltages of Opposite Polarity

MAGNETIC TRANSDUCER AMPLIFIER

A circuit that will detect the zero crossings in the output of a magnetic transducer is shown in Figure 12. Resistor divider, R_1 and R_2 , biases the positive input at $+V_{CC}/2$, which is well within the common mode operating range. The minus input is biased through the magnetic transducer. This allows large signal swings to be handled without exceeding the input voltage limits. A symmetrical square wave output is insured through the positive feedback resistor R_3 . Resistors R_1 and

R_2 can be used to set the DC bias voltage at the positive input at any desired voltage within the input common mode voltage range of the comparator.

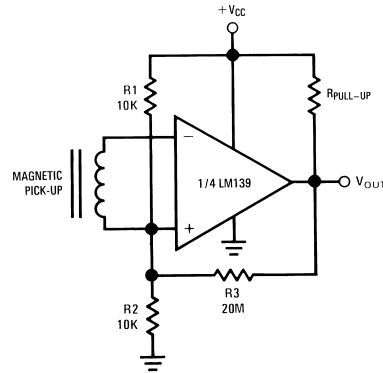


FIGURE 12. Magnetic Transducer Amplifier

OSCILLATORS USING THE LM139

The LM139 lends itself well to oscillator applications for frequencies below several megacycles. Figure 13 shows a symmetrical square wave generator using a minimum of components. The output frequency is set by the RC time constant of R_4 and C_1 and the total hysteresis of the loop is set by R_1 , R_2 and R_3 . The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which would degrade the output slew rate.

To analyze this circuit assume that the output is initially high. For this to be true, the voltage at the negative input must be less than the voltage at the positive input. Therefore, capacitor C_1 is discharged. The voltage at the positive input, V_{A1} , will then be given by:

$$V_{A1} = \frac{+V_{CC} R_2}{R_2 + (R_1 \parallel R_3)} \quad (13)$$

where if $R_1 = R_2 = R_3$
then

$$V_{A1} = \frac{2 V_{CC}}{3} \quad (14)$$

Capacitor C_1 will charge up through R_4 so that when it has charged up to a value equal to V_{A1} , the comparator output will switch. With the output $V_O = \text{GND}$, the value of V_A is reduced by the hysteresis network to a value given by:

$$V_{A2} = \frac{+V_{CC}}{3} \quad (15)$$

using the same resistor values as before. Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state ($V_O = +V_{CC}$) when the voltage across the capacitor has discharged to a value equal to V_{A2} . For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The period can be calculated from:

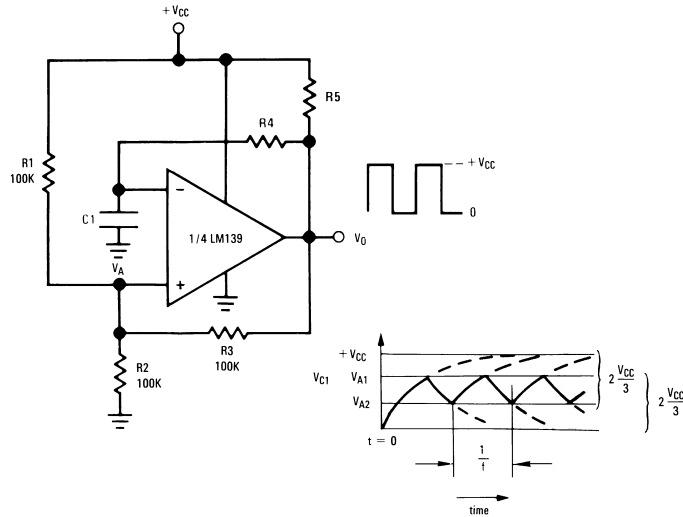
$$V_1 = V_{MAX} e^{-t_1/RC} \quad (16)$$

where

$$V_{MAX} = \frac{2 V_{CC}}{3} \quad (17)$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \quad (18)$$



AN007385-13

FIGURE 13. Square Wave Generator

One period will be given by:

$$\frac{1}{\text{freq.}} = 2t_1 \quad (19)$$

or calculating the exponential gives

$$\frac{1}{\text{freq.}} = 2 (0.694) R_4 C_1 \quad (20)$$

Resistors R_3 and R_4 must be at least 10 times larger than R_5 to insure that V_O will go all the way up to $+V_{CC}$ in the high state. The frequency stability of this circuit should strictly be a function of the external components.

PULSE GENERATOR WITH VARIABLE DUTY CYCLE

The basic square wave generator of Figure 13 can be modified to obtain an adjustable duty cycle pulse generator, as shown in Figure 14, by providing a separate charge and discharge path for capacitor C_1 . One path, through R_4 and D_1 will charge the capacitor and set the pulse width (t_1). The other path, R_5 and D_2 , will discharge the capacitor and set the time between pulses (t_2). By varying resistor R_5 , the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_4 , the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator, however. With the values given in Figure 14, the pulse width and time between pulses can be found from:

$$V_1 = V_{MAX} (1 - e^{-t_1/R_4 C_1}) \text{ risetime} \quad (21a)$$

$$V_1 = V_{MAX} e^{-t_2/R_5 C_1} \text{ falltime} \quad (21b)$$

where

$$V_{MAX} = \frac{2 V_{CC}}{3} \quad (22)$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \quad (23)$$

which gives

$$\frac{1}{2} = e^{-t_1/R_4 C_1} \quad (24)$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5 C_1} \quad (25)$$

These terms will have a slight error due to the fact that V_{MAX} is not exactly equal to $\frac{2}{3} V_{CC}$ but is actually reduced by the diode drop to:

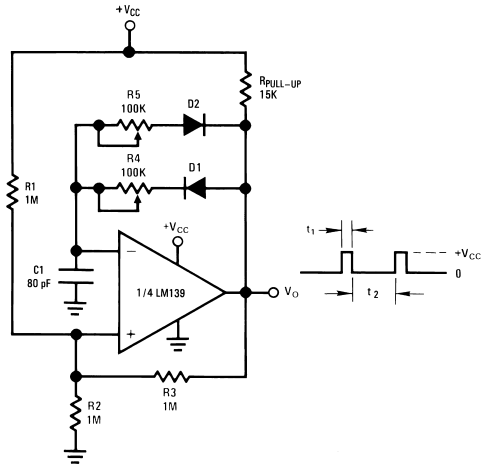
$$V_{MAX} = \frac{2}{3} (V_{CC} - V_{BE}) \quad (26)$$

therefore

$$\frac{1}{2(1 - V_{BE})} = e^{-t_1/R_4 C_1} \quad (27)$$

and

$$\frac{1}{2(1 - V_{BE})} = e^{-t_2/R_5 C_1} \quad (28)$$

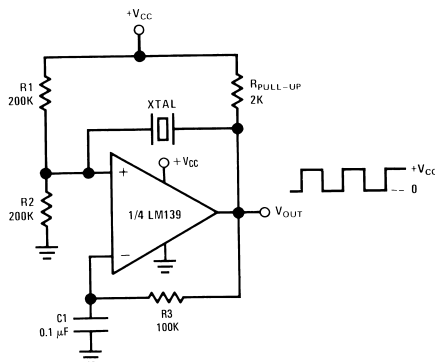


AN007385-14

FIGURE 14. Pulse Generator with Variable Duty Cycle

CRYSTAL CONTROLLED OSCILLATOR

A simple yet very stable oscillator can be obtained by using a quartz crystal resonator as the feedback element. *Figure 15* gives a typical circuit diagram of this. This value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC time constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.



AN007385-15

FIGURE 15. Crystal Controlled Oscillator

When specifying the crystal, be sure to order series resonant along with the desired temperature coefficient and load capacitance to be used.

MOS CLOCK DRIVER

The LM139 can be used to provide the oscillator and clock delay timing for a two phase MOS clock driver (see *Figure 16*). The oscillator is a standard comparator square wave generator similar to the one shown in *Figure 13*. Two other comparators of the LM139 are used to establish the desired phasing between the two outputs to the clock driver. A more detailed explanation of the delay circuit is given in the section under "Digital and Switching Circuits."

WIDE RANGE VCO

A simple yet very stable voltage controlled oscillator using a minimum of external components can be realized using three comparators of the LM139. The schematic is shown in *Figure 17a*. Comparator 1 is used closed loop as an integrator (for further discussion of closed loop operation see section on Operational Amplifiers) with comparator 2 used as a triangle to square wave converter and comparator 3 as the switch driving the integrator. To analyze the circuit, assume that comparator 2 is its high state ($V_{SQ} = +V_{CC}$) which drives comparator 3 to its high state also. The output device of comparator 3 will be OFF which prevents any current from flowing through R_2 to ground. With a control voltage, V_C , at the input to comparator 1, a current I_1 will flow through R_1 and begin discharging capacitor C_1 , at a linear rate. This discharge current is given by:

$$I_1 = \frac{V_C}{2R_1} \quad (29)$$

and the discharge time is given by:

$$I_1 = C_1 \frac{\Delta V}{\Delta t} \quad (30)$$

ΔV will be the maximum peak change in the voltage across capacitor C_1 , which will be set by the switch points of comparator 2. These trip points can be changed by simply altering the ratio of R_F to R_S , thereby increasing or decreasing the amount of hysteresis around comparator 2. With $R_F = 100 \text{ k}\Omega$ and $R_S = 5 \text{ k}\Omega$, the amount of hysteresis is approximately $\pm 5\%$ which will give switch points of $+V_{CC}/2 \pm 750 \text{ mV}$ from a 30V supply. (See "Comparators with Hysteresis").

As capacitor C_1 discharges, the output voltage of comparator 1 will decrease until it reaches the lower trip point of comparator 2, which will then force the output of comparator 2 to go to its low state ($V_{SQ} = \text{GND}$).

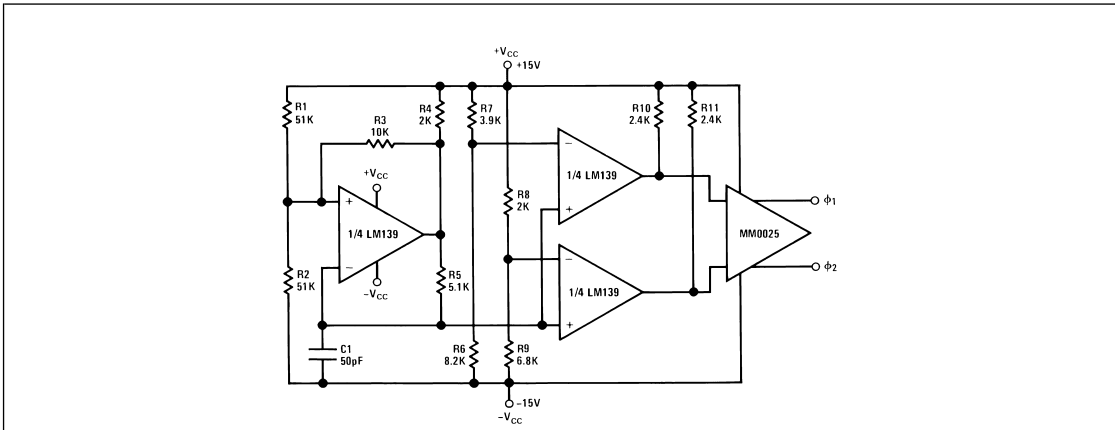


FIGURE 16. MOS Clock Driver

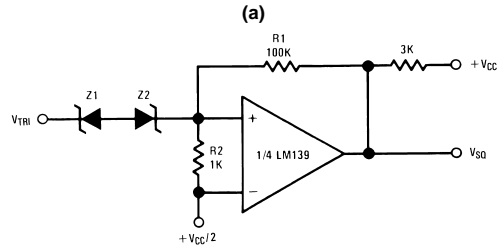
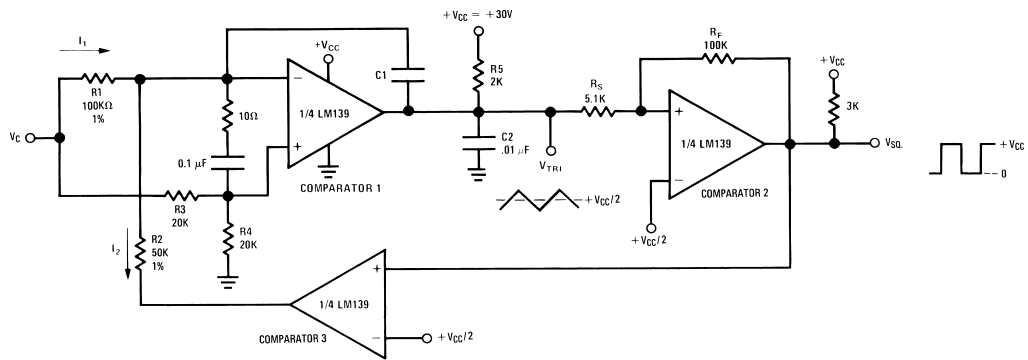


FIGURE 17. Voltage Controlled Oscillator

This in turn causes comparator 3 to go to its low state where its output device will be in saturation. A current I_2 can now flow through resistor R_2 to ground. If the value of R_2 is chosen as $R_1/2$ a current equal to the capacitor discharge current can be made to flow out of C_1 charging it at the same rate as it was discharged. By making $R_2 = R_1/2$, current I_2 will equal twice I_1 . This is the control circuitry which guarantees a constant 50% duty cycle oscillation independent of frequency or temperature. As capacitor C_1 charges, the output of comparator 1 will ramp up until it trips comparator 2 to its high state ($V_{SQ} = +V_{CC}$) and the cycle will repeat. The circuit shown in Figure 17a uses a +30V supply and gives a triangle wave of 1.5V peak-to-peak. With a timing capacitor, C_1 equal to 500 pF, a frequency range from approxi-

mately 115 kHz down to approximately 670 Hz was obtained with a control voltage ranging from 50V down to 250 mV. By reducing the hysteresis around comparator 2 down to ± 150 mV ($R_f = 100$ k Ω , $R_s = 1$ k Ω) and reducing the compensating capacitor C_2 down to .001 μ F, frequencies up to 1 MHz may be obtained. For lower frequencies ($f_o \leq 1$ Hz) the timing capacitor, C_1 , should be increased up to approximately 1 μ F to insure that the charging currents, I_1 and I_2 , are much larger than the input bias currents of comparator 1.

Figure 17b shows another interesting approach to provide the hysteresis for comparator 2. Two identical Zener diodes, Z_1 and Z_2 , are used to set the trip points of comparator 2. When the triangle wave is less than the value required to Zener one of the diodes, the resistive network, R_1 and R_2 , pro-

vides enough feedback to keep the comparator in its proper state, (the input would otherwise be floating). The advantage of this circuit is that the trip points of comparator 2 will be completely independent of supply voltage fluctuations. The disadvantage is that Zeners with less than one volt breakdown voltage are not obtainable. This limits the maximum upper frequency obtainable because of the larger amplitude of the triangle wave. If a regulated supply is available, *Figure 17a* is preferable simply because of less parts count and lower cost.

Both circuits provide good control over at least two decades in frequency with a temperature coefficient largely dependent on the TC of the external timing resistors and capacitors. Remember that good circuit layout is essential along with the 0.01 μF compensation capacitor at the output of comparator 1 and the series 10 Ω resistor and 0.1 μF capacitor between its inputs, for proper operation. Comparator 1 is a high gain amplifier used closed loop as an integrator so long leads and loose layout should be avoided.

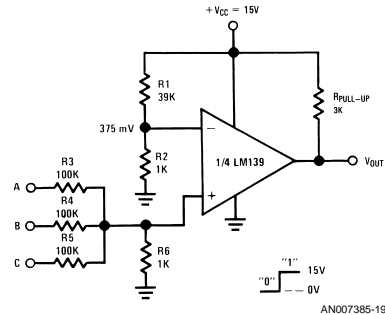
DIGITAL AND SWITCHING CIRCUITS

The LM139 lends itself well to low speed (<1 MHz) high level logic circuits. They have the advantage of operating with high signal levels, giving high noise immunity, which is highly desirable for industrial applications. The output signal level can be selected by setting the V_{CC} to which the pull-up resistor is connected to any desired level.

AND/NAND GATES

A three input AND gate is shown in *Figure 18*. Operation of this gate is as follows: resistor divider R_1 and R_2 establishes a reference voltage at the inverting input to the comparator.

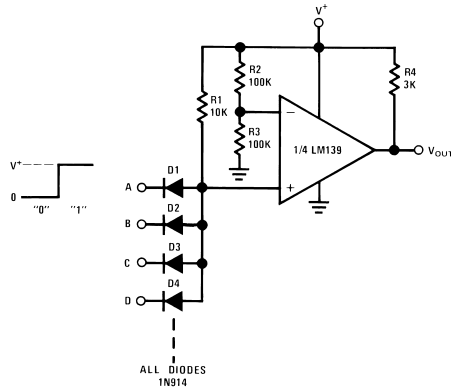
The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers comprised of R_3 , R_4 , R_5 and R_6 . The output will go high only when all three inputs are high, causing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a "0" equal to ground and a "1" equal +15V. The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are the "1" state. This circuit with increased fan-in is shown in *Figure 19*.



$$V_{OUT} = A \cdot B \cdot C$$

FIGURE 18. Three Input AND Gate

To convert these AND gates to NAND gates simply interchange the inverting and non-inverting inputs to the comparator. Hysteresis can be added to speed up output transitions if low speed input signals are used.



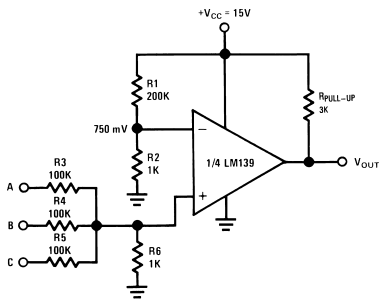
$$V_{OUT} = A \cdot B \cdot C \cdot D$$

FIGURE 19. AND Gate with Large Fan-In

OR/NOR GATES

The three input OR gate (positive logic) shown in *Figure 20* is achieved from the basic AND gate simply by increasing R_1 thereby reducing the reference voltage. A logic "1" at any of

the inputs will produce a logic "1" at the output. Again a NOR gate may be implemented by simply reversing the comparator inputs. Resistor R_6 may be added for the OR or NOR function at the expense of noise immunity if so desired.



$$V_{OUT} = A + B + C$$

FIGURE 20. Three Input OR Gate

AN007385-21

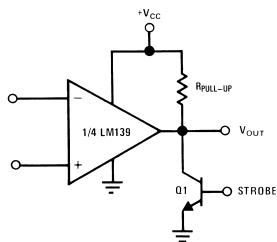


FIGURE 21. Output Strobing Using a Discrete Transistor

AN007385-22

OUTPUT STROBING

The output of the LM139 may be disabled by adding a clamp transistor as shown in Figure 21. A strobe control voltage at the base of Q_1 will clamp the comparator output to ground, making it immune to any input changes.

If the LM139 is being used in a digital system the output may be strobed using any other type of gate having an uncommitted collector output (such as National's DM5401/DM7401). In addition another comparator of the LM139 could also be used for output strobing, replacing Q_1 in Figure 21, if desired. (See Figure 22.)

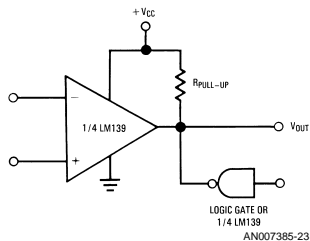


FIGURE 22. Output Strobing with TTL Gate

AN007385-23

ONE SHOT MULTIVIBRATORS

A simple one shot multivibrator can be realized using one comparator of the LM139 as shown in Figure 23. The output pulse width is set by the values of C_2 and R_4 (with $R_4 > 10 R_3$ to avoid loading the output). The magnitude of the input trigger pulse required is determined by the resistive divider R_1 and R_2 . Temperature stability can be achieved by balancing the temperature coefficients of R_4 and C_2 or by using

components with very low TC. In addition, the TC of resistors R_1 and R_2 should be matched so as to maintain a fixed reference voltage of $+V_{CC}/2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset the one shot at the end of its pulse. It also prevents the non-inverting input from being driven below ground. The output pulse width is relatively independent of the magnitude of the supply voltage and will change less than 2% for a five volt change in $+V_{CC}$.

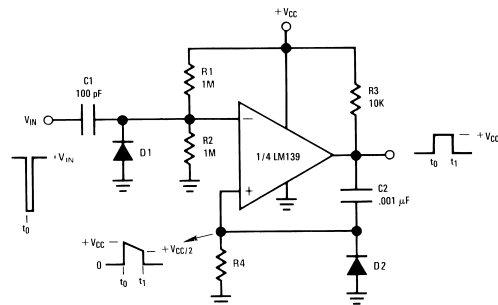


FIGURE 23. One Shot Multivibrator

AN007385-24

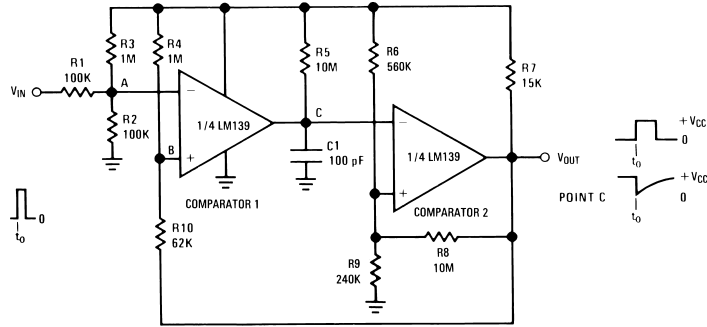
The one shot multivibrator shown in Figure 24 has several characteristics which make it superior to that shown in Figure 23. First, the pulse width is independent of the magnitude of the power supply voltage because the charging voltage and the intercept voltage are a fixed percentage of $+V_{CC}$. In addition this one-shot is capable of 99% duty cycle and exhibits input trigger lock-out to insure that the circuit will not re-trigger before the output pulse has been completed. The trigger level is the voltage required at the input to raise the voltage at point A higher than the voltage at point B, and is set by the resistive divider R_4 and R_{10} and the network R_1 , R_2 and R_3 . When the multivibrator has been triggered, the output of comparator 2 is high causing the reference voltage at the non-inverting input of comparator 1 to go to $+V_{CC}$. This prevents any additional input pulses from disturbing the circuit until the output pulse has been completed.

The value of the timing capacitor, C_1 , must be kept small enough to allow comparator 1 to completely discharge C_1 before the feedback signal from comparator 2 (through R_{10}) switches comparator 1 OFF and allows C_1 to start an exponential charge. Proper circuit action depends on rapidly discharging C_1 to a value set by R_6 and R_9 at which time comparator 2 latches comparator 1 OFF. Prior to the establishment of this OFF state, C_1 will have been completely discharged by comparator 1 in the ON state. The time delay, which sets the output pulse width, results from C_1 recharging to the reference voltage set by R_6 and R_9 . When the voltage across C_1 charges beyond this reference, the output pulse returns to ground and the input is again reset to accept a trigger.

BISTABLE MULTIVIBRATOR

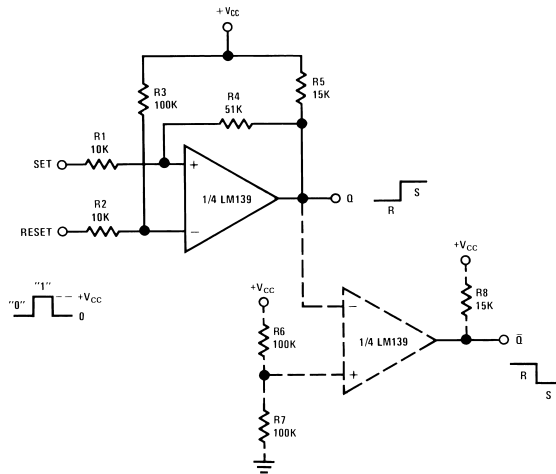
Figure 25 is the circuit of one comparator of the LM139 used as a bistable multivibrator. A reference voltage is provided at the inverting input by a voltage divider comprised of R_2 and R_3 . A pulse applied to the SET terminal will switch the output high. Resistor divider network R_1 , R_4 , and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse now applied to the RESET input will

pull the output low. If both Q and \bar{Q} outputs are needed, another comparator can be added as shown dashed in Figure 25.



AN007385-25

FIGURE 24. Multivibrator with Input Lock-Out



AN007385-26

FIGURE 25. Bistable Multivibrator

Figure 26 shows the output saturation voltage of the LM139 comparator versus the amount of current being passed to ground. The end point of 1 mV at zero current along with an R_{SAT} of 60Ω shows why the LM139 so easily adapts itself to

oscillator and digital switching circuits by allowing the DC output voltage to go practically to ground while in the ON state.

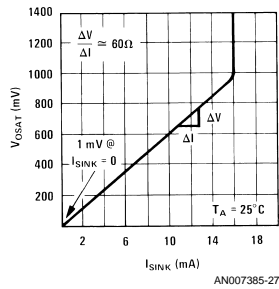


FIGURE 26. Typical Output Saturation Characteristics

TIME DELAY GENERATOR

The final circuit to be presented "Digital and Switching Circuits" is a time delay generator (or sequence generator) as shown in Figure 27.

This timer will provide output signals at prescribed time intervals from a time reference t_0 and will automatically reset when the input signal returns to ground. For circuit evaluation, first consider the quiescent state ($V_{IN} = 0$) where the output of comparator 4 is ON which keeps the voltage across C_1 at zero volts. This keeps the outputs of comparators 1, 2 and 3 in their ON state ($V_{OUT} = GND$). When an input signal is applied, comparator 4 turns OFF allowing C_1 to charge at an exponential rate through R_1 . As this voltage rises past the present trip points V_A , V_B , and V_C of each of these comparators will switch to the high state ($V_{OUT} = +V_{CC}$). A small amount of hysteresis has been provided to insure fast switching for the case where the R_C time constant has been chosen large to give long delay times. It is not necessary that all comparator outputs be low in the quiescent state. Several or all may be reversed as desired simply by reversing the inverting and non-inverting input connections. Hysteresis again is optional.

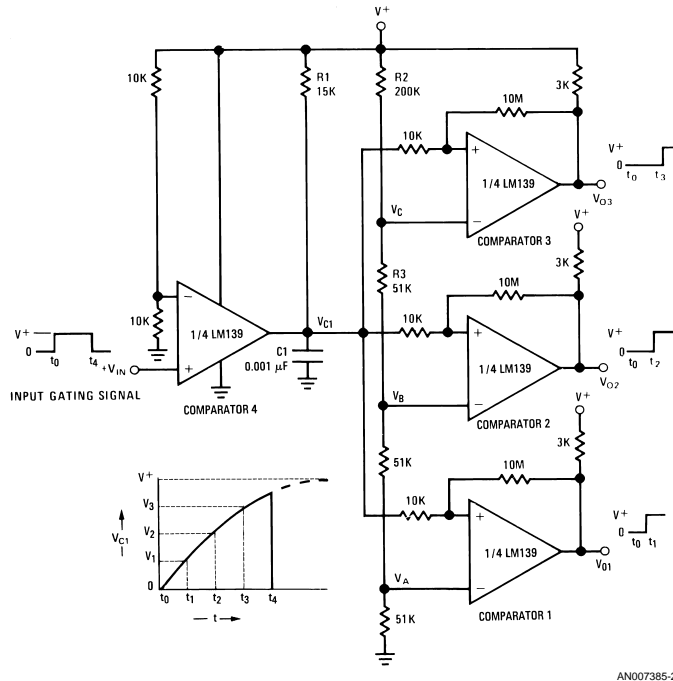
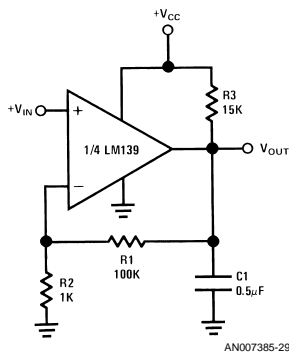


FIGURE 27. Time Delay Generator

LOW FREQUENCY OPERATIONAL AMPLIFIERS

The LM139 comparator can be used as an operational amplifier in DC and very low frequency AC applications (≤ 100 Hz). An interesting combination is to use one of the comparators as an op amp to provide a DC reference voltage for the other three comparators in the same package. Another useful application of an LM139 has the interesting feature that the input common mode voltage range includes

ground even though the amplifier is biased from a single supply and ground. These op amps are also low power drain devices and will not drive large load currents unless current is boosted with an external NPN transistor. The largest application limitation comes from a relatively slow slew rate which restricts the power bandwidth and the output voltage response time.



$$A_v = 1 + \frac{R_1}{R_2} = 101$$

FIGURE 28. Non-Inverting Amplifier

The LM139, like other comparators, is not internally frequency compensated and does not have internal provisions for compensation by external components. Therefore, compensation must be applied at either the inputs or output of the device. *Figure 28* shows an output compensation scheme which utilizes the output collector pull-up resistor working with a single compensation capacitor to form a dominant pole. The feedback network, R_1 and R_2 sets the closed loop gain at $1 + R_1/R_2$ or 101 (40 dB). *Figure 29* shows the output swing limitations versus frequency. The output current capability of this amplifier is limited by the relatively large pull-up resistor (15 kΩ) so the output is shown boosted with an external NPN transistor in *Figure 30*. The frequency response is greatly extended by the use of the new compensation scheme also shown in *Figure 30*. The DC level shift due to the V_{BE} of Q_1 allows the output voltage to swing from ground to approximately one volt less than $+V_{CC}$. A voltage offset adjustment can be added as shown in *Figure 31*.

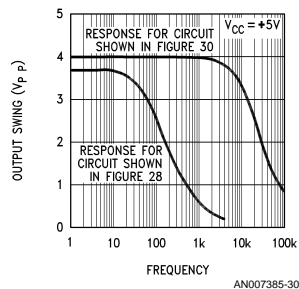


FIGURE 29. Large Signal Frequency Response

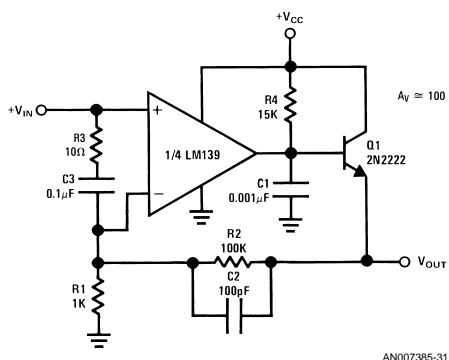
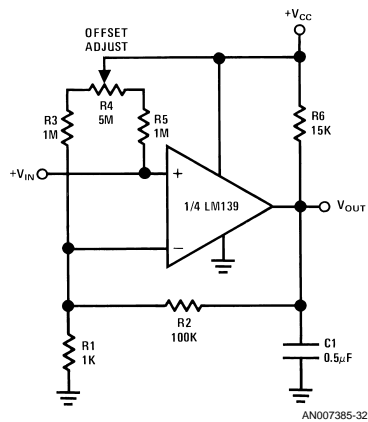


FIGURE 30. Improved Operational Amplifier



$A_v \cong 100$

FIGURE 31. Input Offset Null Adjustment

DUAL SUPPLY OPERATION

The applications presented here have been shown biased typically between $+V_{CC}$ and ground for simplicity. The LM139, however, works equally well from dual (plus and minus) supplies commonly used with most industry standard op amps and comparators, with some applications actually requiring fewer parts than the single supply equivalent.

The zero crossing detector shown in Figure 10 can be implemented with fewer parts as shown in Figure 32. Hysteresis has been added to insure fast transitions if used with slowly moving input signals. It may be omitted if not needed, bringing the total parts count down to one pull-up resistor.

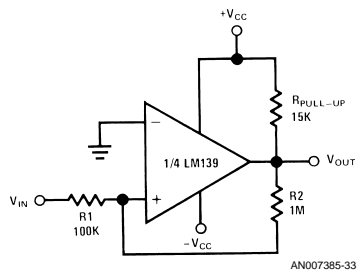


FIGURE 32. Zero Crossing Detector Using Dual Supplies

The MOS clock driver shown in Figure 16 uses dual supplies to properly drive the MM0025 clock driver.

The square wave generator shown in Figure 13 can be used with dual supplies giving an output that swings symmetrically

above and below ground (see Figure 33). Operation is identical to the single supply oscillator with only change being in the lower trip point.

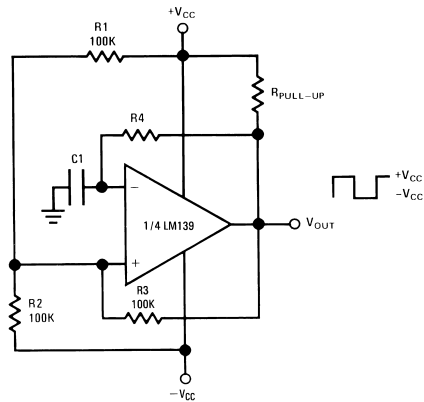


FIGURE 33. Squarewave Generator Using Dual Supplies

Figure 34 shows an LM139 connected as an op amp using dual supplies. Biasing is actually simpler if full output swing at low gain settings is required by biasing the inverting input from ground rather than from a resistive divider to some voltage between $+V_{CC}$ and ground.

All the applications shown will work equally well biased with dual supplies. If the total voltage across the device is increased from that shown, the output pull-up resistor should be increased to prevent the output transistor from being pulled out of saturation by drawing excessive current, thereby preventing the output low state from going all the way to $-V_{CC}$.

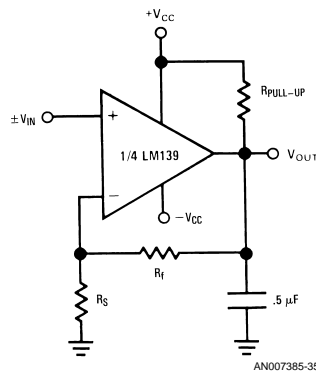


FIGURE 34. Non-Inverting Amplifier Using Dual Supplies

MISCELLANEOUS APPLICATIONS

The following is a collection of various applications intended primarily to further show the wide versatility that the LM139 quad comparator has to offer. No new modes of operation are presented here so all of the previous formulas and circuit descriptions will hold true. It is hoped that all of the circuits presented in this application note will suggest to the user a few of the many areas in which the LM139 can be utilized.

REMOTE TEMPERATURE SENSOR/ALARM

The circuit shown in *Figure 35* shows a temperature over-range limit sensor. The 2N930 is a National process 07 silicon NPN transistor connected to produce a voltage reference equal to a multiple of its base emitter voltage along with temperature coefficient equal to a multiple of 2.2 mV/°C.

That multiple is determined by the ratio of R_1 to R_2 . The theory of operation is as follows: with transistor Q_1 biased up, its base to emitter voltage will appear across resistor R_1 . Assuming a reasonably high beta ($\beta \geq 100$) the base current can be neglected so that the current that flows through resistor R_1 must also be flowing through R_2 . The voltage drop across resistor R_2 will be given by:

$$I_{R1} = I_{R2}$$

and

$$V_{R1} = V_{be} = I_{R1} R_1$$

so

$$V_{R2} = I_{R2} R_2 = I_{R1} R_2 = V_{be} \frac{R_2}{R_1} \quad (31)$$

As stated previously this base-emitter voltage is strongly temperature dependent, minus 2.2 mV/°C for a silicon transistor. This temperature coefficient is also multiplied by the resistor ratio R_1/R_2 .

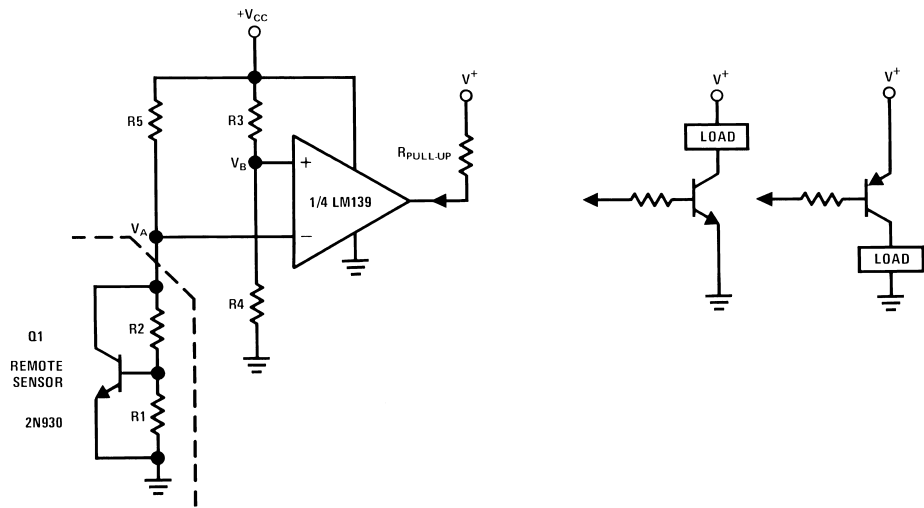
This provides a highly linear, variable temperature coefficient reference which is ideal for use as a temperature sensor over a temperature range of approximately -65°C to +150°C. When this temperature sensor is connected as shown in *Figure 35* it can be used to indicate an alarm condition of either too high or too low a temperature excursion. Resistors R_3

and R_4 set the trip point reference voltage, V_B , with switching occurring when $V_A = V_B$. Resistor R_5 is used to bias up Q_1 at some low value of current simply to keep quiescent power dissipation to a minimum. An I_Q near 10 μ A is acceptable.

Using one LM139, four separate sense points are available. The outputs of the four comparators can be used to indicate four separate alarm conditions or the outputs can be OR'ed together to indicate an alarm condition at any one of the sensors. For the circuit shown the output will go HIGH when the temperature of the sensor goes above the preset level. This could easily be inverted by simply reversing the input leads. For operation over a narrow temperature range, the resistor ratio R_2/R_1 should be large to make the alarm more sensitive to temperature variations. To vary the trip points a potentiometer can be substituted for R_3 and R_4 . By the addition of a single feedback resistor to the non-inverting input to provide a slight amount of hysteresis, the sensor could function as a thermostat. For driving loads greater than 15 mA, an output current booster transistor could be used.

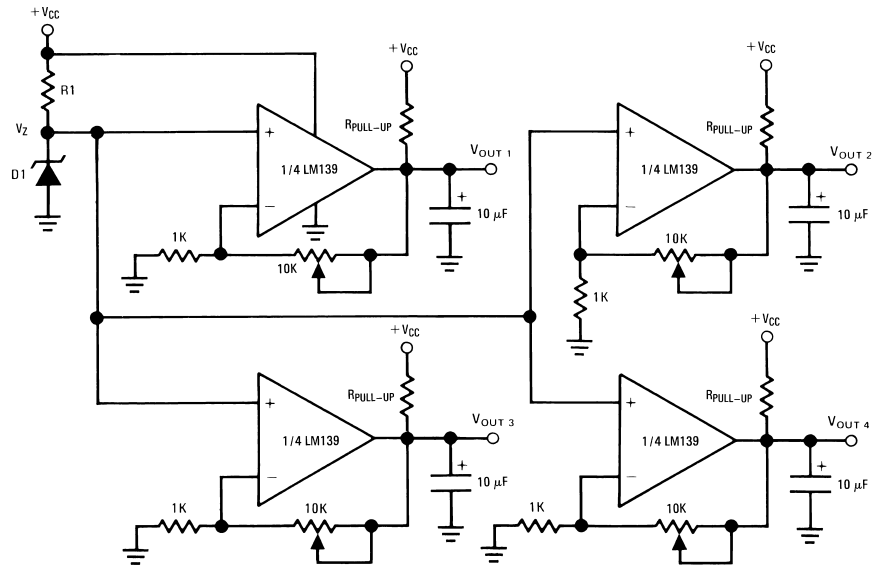
FOUR INDEPENDENTLY VARIABLE, TEMPERATURE COMPENSATED, REFERENCE SUPPLIES

The circuit shown in *Figure 36* provides four independently variable voltages that could be used for low current supplies for powering additional equipment or for generating the reference voltages needed in some of the previous comparator applications. If the proper Zener diode is chosen, these four voltages will have a near zero temperature coefficient. For industry standard Zeners, this will be somewhere between 5.0 and 5.4V at a Zener current of approximately 10 mA. An alternative solution is offered to reduce this 50 mW quiescent power drain. Experimental data has shown that any of National's process 21 transistors which have been selected for low reverse beta ($\beta_R < .25$) can be used quite satisfactorily as a zero T.C. Zener. When connected as shown in *Figure 37*, the T.C. of the base-emitter Zener voltage is exactly cancelled by the T.C. of the forward biased base-collector junction if biased at 1.5 mA. The diode can be properly biased from any supply by adjusting R_5 to set I_Q equal to 1.5 mA. The outputs of any of the reference supplies can be current boosted by using the circuit shown in *Figure 30*.



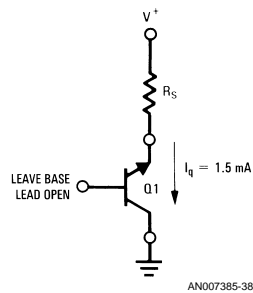
AN007385-36

FIGURE 35. Temperature Alarm



AN007385-37

FIGURE 36. Four Variable Reference Supplies



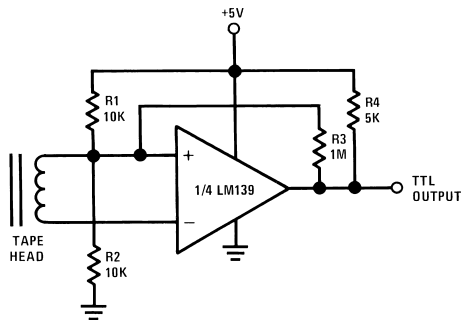
AN007385-38

Q1 = National Process 21 Selected for Low Reverse β

FIGURE 37. Zero T.C. Zener

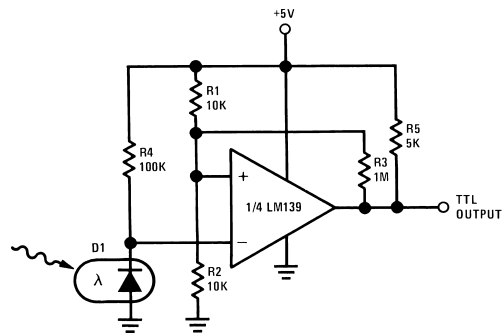
DIGITAL TAPE READER

Two circuits are presented here—a tape reader for both magnetic tape and punched paper tape. The circuit shown in *Figure 38*, the magnetic tape reader, is the same as *Figure 12* with a few resistor values changed. With a 5V supply, to make the output TTL compatible, and a 1 M Ω feedback resistor, ± 5 mV of hysteresis is provided to insure fast switching and higher noise immunity. Using one LM139, four tape channels can be read simultaneously.



AN007385-39

FIGURE 38. Magnetic Tape Reader with TTL Output



AN007385-40

FIGURE 39. Paper Tape Reader With TTL Output

The paper tape reader shown in *Figure 39* is essentially the same circuit as *Figure 38* with the only change being in the type of transducer used. A photo-diode is now used to sense the presence or absence of light passing through holes in the tape. Again a 1 M Ω feedback resistor gives ± 5 mV of hysteresis to insure rapid switching and noise immunity.

PULSE WIDTH MODULATOR

Figure 40 shows the circuit for a simple pulse width modulator circuit. It is essentially the same as that shown in *Figure 13* with the addition of an input control voltage. With the input control voltage equal to $+V_{CC}/2$, operation is basically the same as that described previously. If the input control voltage is moved above or below $+V_{CC}/2$, however, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. These trip points can be found if the circuit is simplified as in *Figure 41*. Equations 13 through 20 are still applicable if the effect of R_C is added, with equations 17 through 20 being altered for condition where $V_C \neq +V_{CC}/2$.

Pulse width sensitivity to input voltage variations will be increased by reducing the value of R_C from 10 k Ω and alternately, sensitivity will be reduced by increasing the value of R_C . The values of R_1 and C_1 can be varied to produce any desired center frequency from less than one hertz to the maximum frequency of the LM139 which will be limited by $+V_{CC}$ and the output slew rate.

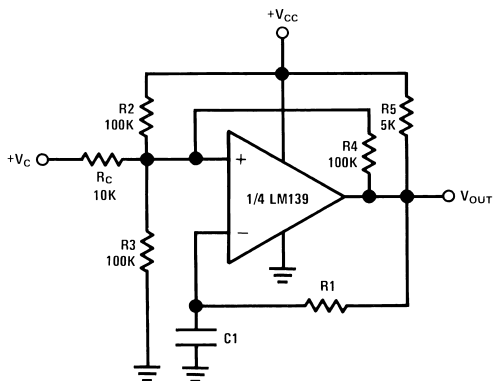
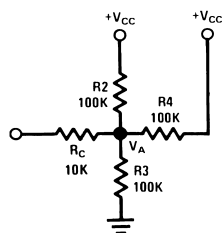


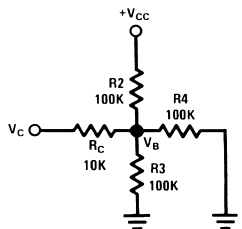
FIGURE 40. Pulse Width Modulator

AN007385-41



AN007385-81

V_A = UPPER TRIP POINT



AN007385-82

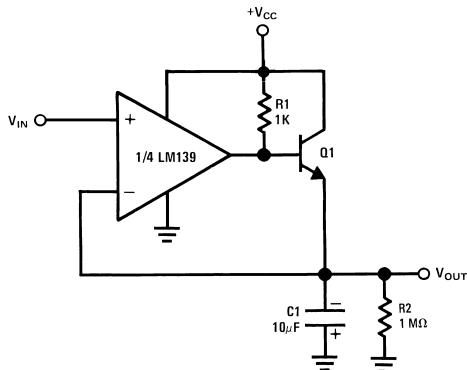
V_B = LOWER TRIP POINT

FIGURE 41. Simplified Circuit For Calculating Trip Points of Figure 40

POSITIVE AND NEGATIVE PEAK DETECTORS

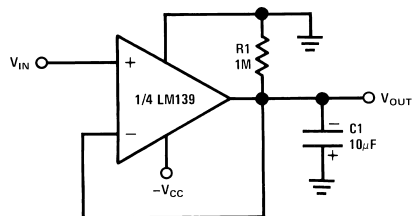
Figures 42, 43 show the schematics for simple positive or negative peak detectors. Basically the LM139 is operated closed loop as a unity gain follower with a large holding capacitor from the output to ground. For the positive peak detector a low impedance current source is needed so an additional transistor is added to the output. When the output of the comparator goes high, current is passed through Q_1 to

charge up C_1 . The only discharge path will be the $1\text{ M}\Omega$ resistor shunting C_1 and any load that is connected to V_{OUT} . The decay time can be altered simply by changing the $1\text{ M}\Omega$ resistor higher or lower as desired. The output should be used through a high impedance follower to avoid loading the output of the peak detector.



AN007385-43

FIGURE 42. Positive Peak Detector



AN007385-44

FIGURE 43. Negative Peak Detector

For the negative peak detector, a low impedance current sink is required and the output transistor of the LM139 works quite well for this. Again the only discharge path will be the $1\text{ M}\Omega$ resistor and any load impedance used. Decay time is changed by varying the $1\text{ M}\Omega$ resistor.

CONCLUSION

The LM139 is an extremely versatile comparator package offering reasonably high speed while operating at power levels in the low mW region. By offering four independent comparators in one package, many logic and other functions can now be performed at substantial savings in circuit complexity, parts count, overall physical dimensions, and power consumption.

For limited temperature range application, the LM239 or LM339 may be used in place of the LM139.

It is hoped that this application note will provide the user with a guide for using the LM139 and also offer some new application ideas.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

www.national.com