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CSR uEnergy®™

CSR1012 Hardware Review Template

Design Document

Issue 1

Document History

Revision	Date	History
1	25 FEB 14	Original publication of this document

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Contents

Tables, Figures and Equations

1. Introduction

This memo, prepared by CSR, contains a hardware design review for CSR1012 QFN.

The CSR1012 when used with SDK 2.3 onwards can now be operated up to 4.3V. When operating at the higher voltages there are some changes required to the power supply layout. See notes later in this document.

Note

Review text that is highlighted in yellow indicates that CSR has some concerns with this area of the design. **For all areas shown in Bold, we recommend the customer review the design.** An NG in the verdict column indicates that the information is not provided in the schematics. An '**X**' in the Verdict column indicates that CSR recommends a design change.

2. Schematic

2.1. Pin Out

Pin Name	Pin Number	Verdict
RF	7	
XTAL_32K_OUT	2	
XTAL_32K_IN	3	
XTAL_16MHz_OUT	9	
XTAL_16MHz_IN	10	
I2C_SDA /SF_DOUT	29	
I2C_SCL/SF_CLK	28	
PIO[11]	25	
PIO[10]	24	
PIO[9]	23	
PIO[8] / DEBUG_MISO	22	
PIIO[7] / DEBUG_MOSI	20	
PIO[6] / DEBUG_CS#	19	
PIO[5] / DEBUG_CLK	18	
PIO[4] / SF_CS#	17	
PIO[3] / SF_DIN	16	
PIO[2]	27	
PIO[1] UART_RX	15	
PIO[0] / UART_TX	14	
AIO[2]	11	
AIO[1]	12	
AIO[0]	13	
SPI_PIO#	26	
WAKE	4	
VDD_BAT	1	
VDD_BAT_SMPS	32	
SMPS_LX	31	
VDD_CORE	5	
VDD_CORE	30	

Pin Name	Pin Number	Verdict
VDD_PADS	21	
VDD_REG_IN	6	
VDD_XTAL (VDD_AUX)	8	
VSS	Exposed pad	

Table 2.1: Lead Name to Use on Schematic

2.2. CSR1012 Hardware Design

2.2.1. Operational Temperature Range

Check	Limits	Verdict	Observations
Temperature range	-30 ~ +85°C	-	-

Table 2.2: Operational Temperature Range

2.2.2. Power Rails

Check	Limits	Verdict	Observation
VDD_BAT	1.8 to 4.3 V		
VDD_BAT_SMPS	1.8 to 4.3 V		
SMPS_LX / VDD_REG_IN	0.65 to 1.35 V		SMPS_LX connects to VDD_REG_IN via a filter. **Note:** That SMPS_LX (pin 31) is SMPS output before smoothing and so is not a smooth 1.35 V but VDD_REG_IN (pin 6) is.
VDD_PADS	1.2 to 4.3 V		

Table 2.3: Power Rail Limits

2.2.3. Filtering Required on Power Rails

Check	Verdict	Observations
SMPS_LX needs an inductor of 4.7uH		The inductor is connected with VDD_REG_IN (pin 6).
VDD_BAT and VDD_BAT_SMPS require one common capacitor of 47nF capacitor		VDD_BAT is generally connected with VDD_SMPS and the power rail requires the decoupling capacitor.
33pF capacitor on VDD_BAT		33pF close to VDD_BAT pin.
Ferrite bead on between VDD_BAT port and VDD_BAT_SMPS		Keep ferrite bead and 33 pF capacitor close to VDD_BAT port.
2.2uF capacitor on VDD_BAT_SMPS 4.3V – Change 2.2uF to 4.7uF		2.2uF close to VDD_BAT_SMPS port.

Check	Verdict	Observations
Capacitor		For 4.3V operation - 4.7uF close to VDD_BAT_SMPS port.
2.2µF and 470nF capacitors on VDD_REG_IN For 4.3V – Change 2.2uF to 4.7uF Capacitor and add another 2.2uF capacitor		2.2uF close to Inductor and 470nF close to VDD_REG_IN pin 6. For 4.3V operation - 4.7uF close to Inductor and add another 2.2uF capacitor in parallel with 470nF close to VDD_REG_IN pin 6.
470nF and 150nF capacitors on VDD_CORE		CSR recommends that 470nF close to pin 5 and 150nF close to pin 30.
47nF capacitor on VDD_PADS		Decoupling for pads ring.
470nF on VDD_XTAL (VDD_AUX)		To provide decoupling of reference clock circuit.
1uF capacitor on PIO2 for the external EEPROM or Flash		To provide bulk capacitance for the Memory device.

Table 2.4: Power Rail Filtering

Note:

A recommended ferrite bead is listed in Table 2.13.

Figure 2.1 shows the supply rail filtering arrangements for CSR1012 (3.6Vmax).

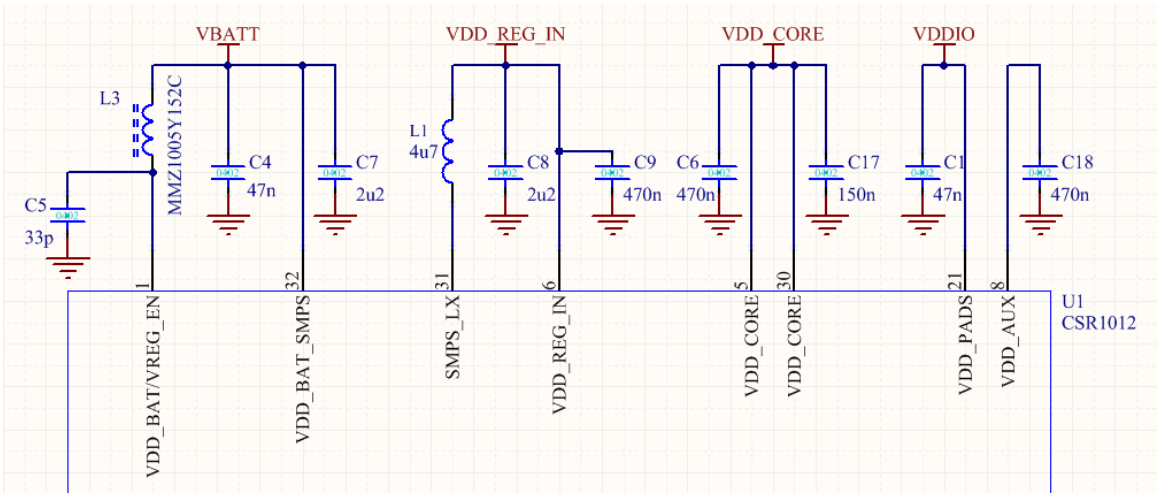

Figure 2.1: Filtering Capacitor Connected on Different Supply Rails (3.6V max)

Figure 2.2 shows the supply rail filtering arrangements for CSR1012 (4.3Vmax).

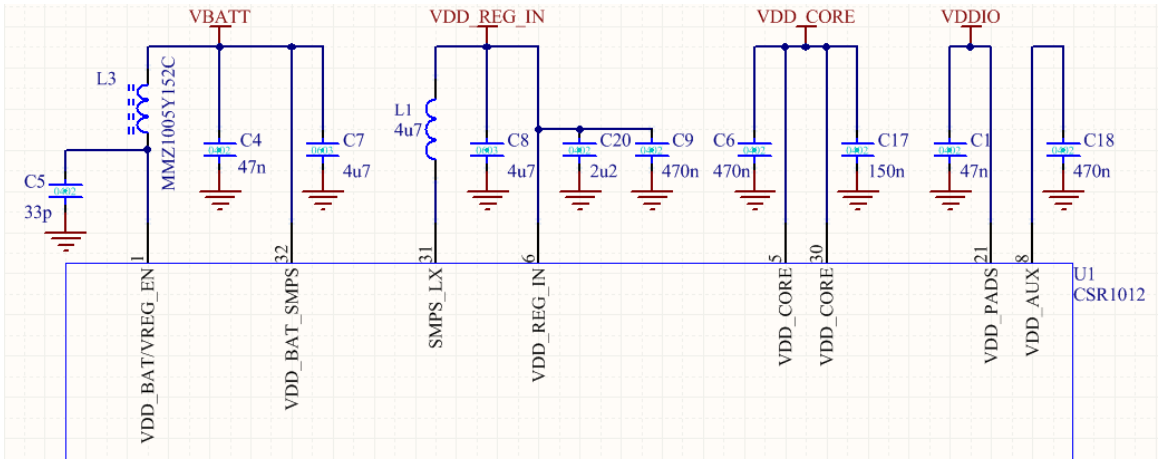

Figure 2.2: Filtering Capacitor Connected on Different Supply Rails (4.3Vmax)

Note:

The layout grounding around pin32 and pin1 is critical to stopping the switching noise in the region of 100 MHz getting into pin 1. It may need a second 33 pF capacitor in parallel with the 2.2uF (4.3V, 4.7uF) on pin 32 as well as the 33 pF close to pin1.

2.2.4. RF Matching

Check	Verdict	Observations
RF port is single-ended 50 Ω, thus no matching network is needed. (a DC block capacitor is not required)		For a simple RF filter a 0.5pF can be connected from close to pin 7 to ground and the RF filter omitted. This is good enough to pass ETSI and FCC.

Table 2.5: RF Matching

Figure 2.3 shows RF connection to ANT.

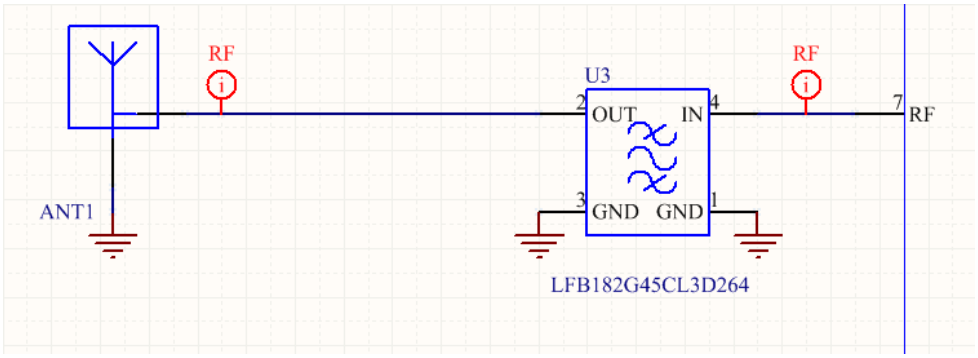

Figure 2.3: RF Port ~ ANT Connection

2.2.5. Clock Circuit

Reference (Main) Clock		
Crystal frequency must be 16 MHz		
Initial frequency tolerance (without trimming) must be less than ±25 ppm*		
The values of XTAL tank capacitors are in the ratio 2:1 (recommended 15 pF: 8.2 pF). Have the smaller capacitor on XTAL_IN.		
Sleep Clock		
Input frequency must be 32.768 kHz for the timing.		
Frequency tolerance must be less than ±250 ppm		
The values of XTAL tank capacitors are in the ratio 1:1 (recommended 10 pF: 10 pF).		

Table 2.6: Clock Circuit

Note:

CSR1012 contains on-chip XTAL trimming capacitors to fine-tune the crystal resonant frequency. All units should be calibrated in production. The Cap values are determined on a per design basis. The ±25 ppm accuracy requirement is after all compensation for any reproducible variation of crystal behaviour with temperature. To use no trimming on the production line use a 10ppm XTAL and 1% capacitors.

Figure 2.4 shows recommended Crystal applications.

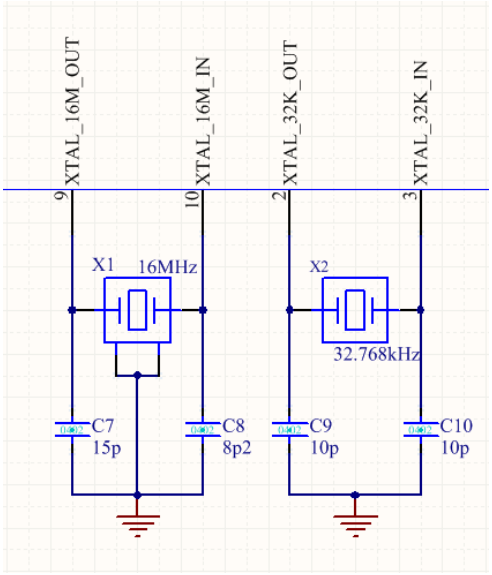

Figure 2.4: Recommended Crystal Circuit

CSR1012 can support external 32.768KHz clock input. In this application, Please note **32.768KHz MUST BE AVAILABLE** when CSR1012 is on. Figure 2.5 shows recommended external 32.768KHz clock input circuit.

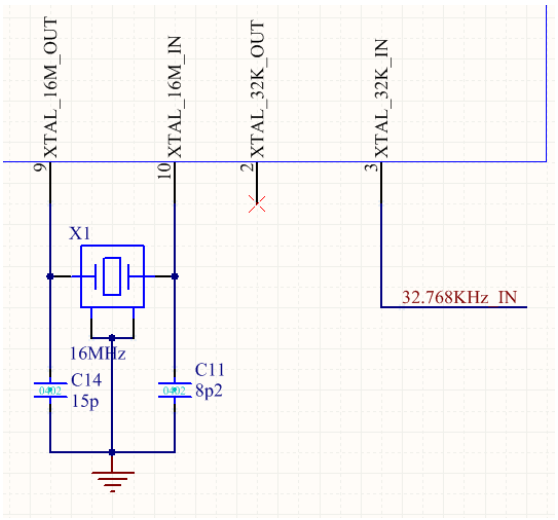

Figure 2.5: External 32.768KHz Clock Input Circuit

Check	Limit	Verdict	Observations
XTAL_32K_IN	DC Level: 1.2V~4.3V		
XTAL_32K_OUT			Leave XTAL_32K_OUT floating.

Table 2.7: External 32.768KHz Clock Input

2.2.6. WAKE

Check	Verdict	Observations
To wake up from hibernate or dormant mode, toggle the WAKE pin. If hibernate or dormant mode is not used, connect the WAKE pin to ground with a jumper.		

Table 8: WAKE pin Configuration

2.2.7. GPIO

Check	Verdict	Observations
Ensure that the interface voltage of PIO[11:0] is the same as VDD_PADS		
Ensure that the maximum input voltage of AIO[2:0] is 1.3 V		

Table 9: GPIO

2.2.8. Debug SPI

Check	Verdict	Observations
Take SPI_PIO#_SEL high to enable the SPI debug interface		
Insert a 47kohm pull-down on SPI_PIO#_SEL if PIO is selected		Please don't leave the port open even in PIO mode.
Ensure that the interface voltage of debug SPI is the same as VDD_PADS		
Assign SPI_CLK to PIO[5]		
Assign SPI_CSB to PIO[6]		
Assign SPI_MOSI to PIO[7]		
Assign SPI_MISO to PIO[8]		

Table 10: Debug SPI

Notes:

(1) CSR strongly recommends that Debug SPIs be tracked out to enable real world debugging.

(2) In addition, CSR recommends that SPI_PIO# have a flexibility to be connected with GND or VBAT so that the PIOs can be used and Debug SPIs can be used by pulling the line high.

2.2.9. EEPROM

Check	Verdict	Observations
I2C_SCL is for SCL		No pull-up resistor required.
I2C_SDA is for SDA		No pull-up resistor required.
PIO[2] is for VDD of the EEPROM		
Pulled-down WP pin to enable normal memory operation (valid read and write)		

Table 2.11: EEPROM

Figure 2.6 shows the recommended EEPROM Configuration.

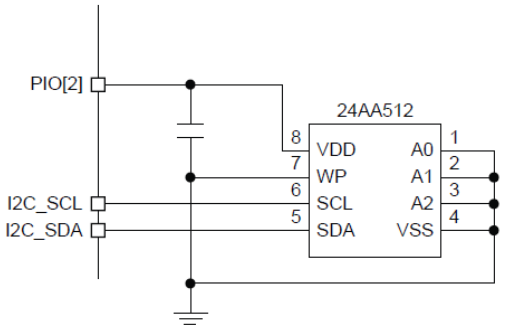

Figure 2.6: Example of an I2C Interface EEPROM Connection

2.2.10. SPI Master Memory Interface

Check	Verdict	Observations
PIO[2] is for Flash_VDD		
PIO[3] is for SF_DIN Note: Connect SF_DIN of CSR1012 to DIN of Serial FLASH		
PIO[4] is for SF_CS# Note: On an unprogammed PCB this line will be high		
I2C_SCL is for SF_CLK		
I2C_SDA is for SF_DOUT Note: Connect SF_DOUT of CSR1012 to DOUT of Serial FLASH		

Table 2.12: SPI Master Interface

Note:

If an application using CSR1012 QFN is designed to boot from SPI serial flash, it is possible for the firmware to map the I2C interface to alternative PIOs.

2.3. Component

Check	Verdict	Observations
RF Filter		Murata: LFB182G45CL3D264
External Switching Inductor		Murata: LQM2HPN4R7MGCL
16 MHz Crystal		Epson Toyocom: TSX3225
32 kHz Crystal		Epson Toyocom: MC-146 32768Hz
SPI Flash		ADESTO: AT25F512 (supports this flash only)
EEPROM		ATMEL: AT24C512C*
Ferrite bead		TDK: MMZ1005Y152C

Table 2.13: Components List

Note:

* A special price from ATMEL to go with CSR1012 is:

- Custom part number AT24C512C-SSHMEU-T
- See the Memories document in the uEnergy area of CSR support for other supported EEPROM's

3. Layout

3.1. Points for Layout

Item	Observations	Verdict
Board Structure	The PCB layout can be a simple double sided PCB (multi-layer PCB is also suitable)	
Ground Plane	Requires a solid ground plane. Put a lot of ground vias in the free ground area as well as a minimum of 9 via's the exposed ground pad in CSR1012.	
RF	Use a 50 Ω RF line. The RF line must completely be isolated and protected by the ground planes. No other signal lines are allowed to cross over the RF line or to run along with the RF line. Add ground stitching between RF track and the 16MHz XTAL to stop 16MHz spurs in RF output.	
32 kHz and 16 MHz Crystal	These need to have short connections directly from the crystal to the IC and its capacitors need to be close to the pins and connected to a solid ground that is directly connected to the ground paddle of the CSR1012. The second layer underneath the crystal must be ground plane. No other signal lines are allowed to cross over the crystal lines.	
SMPS and Power Lines	The switcher needs to be routed with a thick track from the LX pin to the inductor and then from the inductor with a thick track to the VDD_REG_IN pin usually on the second tracing layer. Keep the inductor close to the LX pin For 3.6V max voltage operation the two decoupling capacitors on VDD_REG_IN need to be placed one C8 (2.2uF) next to the inductor and the other C9 (470nF) next to the VDD_REG_IN pin with a good solid ground that is directly connected to the ground paddle of the CSR1012. C7(2.2uF) and C8(2.2uF) should share the same ground and that ground should be isolated from the top layer ground with a solid ground via connection to ground on Ground (Bottom) layer. VDD_BAT is connected to the internal references so it should be filtered with a C5 (33 pF) cap close the pin. VDD_BAT_SMPS is connected to the internals of the switcher so is C7	

Item	Observations	Verdict
	(2.2uF) decoupling capacitor should be connected close to the pin and have its own via back to the central ground paddle. Consider return current loop when designing the SMPS routing. The return current typically flows from the decoupling GNDs at the SMPS output to both the SMPS GND (VSS) and the decoupling GNDs at SMPS input. The tracking must be as short as possible. Generally power lines need thick tracks.	
	For 4.3V operation, C7 and C8 change from 2.2uF to 4.7uF(need to check the package and footprint) and add C20 (2.2uF) in parallel with C9 (470nF) and close to VDD_ VREG_IN.	
Decoupling Capacitors	All supply tracks should run through the decoupling capacitor before connecting to the chip pin where possible. Connect specific decoupling capacitors directly to relevant pins and keep tracks as short as possible. Use a thick line as much as possible. All decoupling capacitors need their own through vias to bottom layer (ground plane).	
Common Vias	Common vias are not used for decoupling capacitors (apart from the decoupling for SMPS).	

Table 3.1: Points for Layout

Figure 3.1 shows recommended layout with two-layer PCB (3.6V Max).

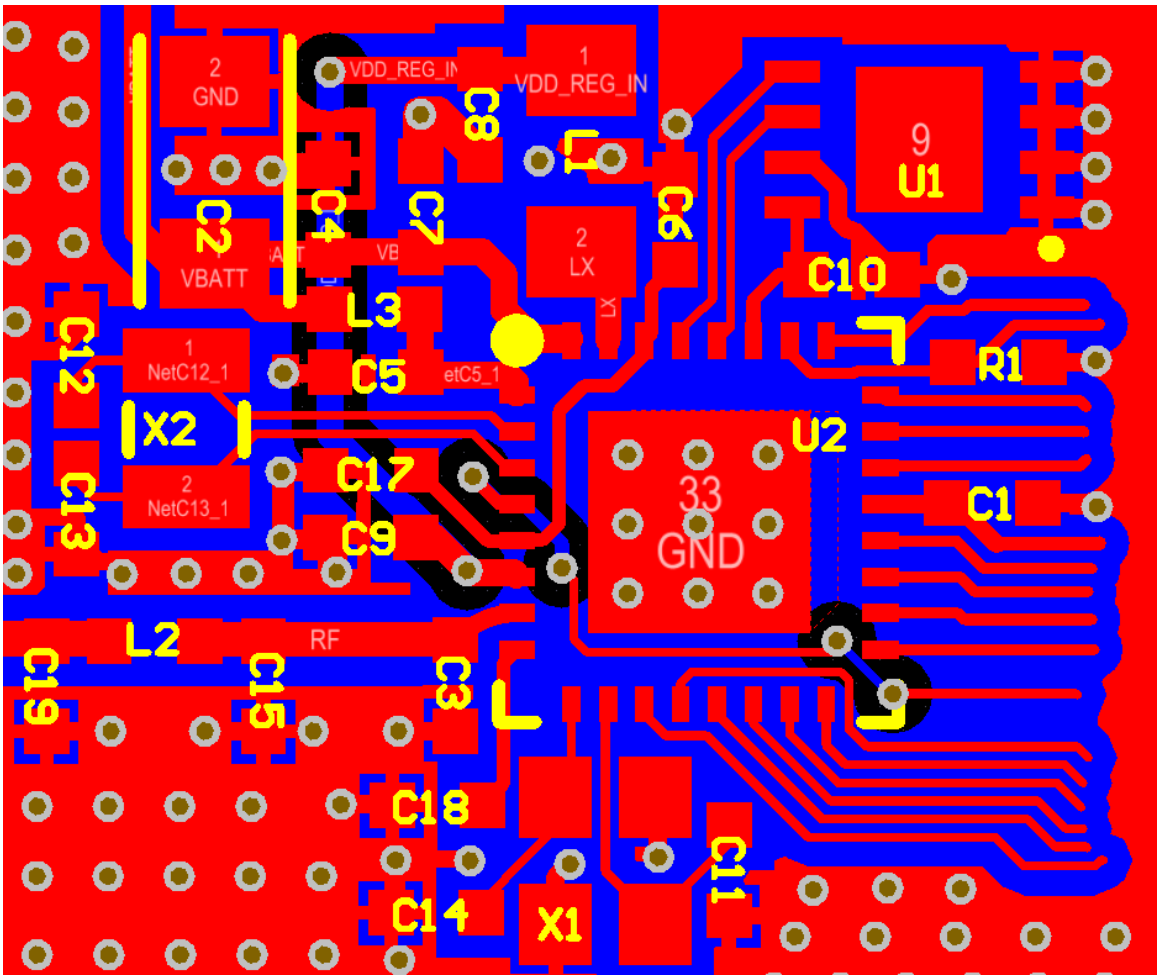

Figure 3.1: Recommended Layout with Two-Layer PCB (3.6V max.)

Figure 3.2 shows recommended layout with two-layer PCB (4.3V max).

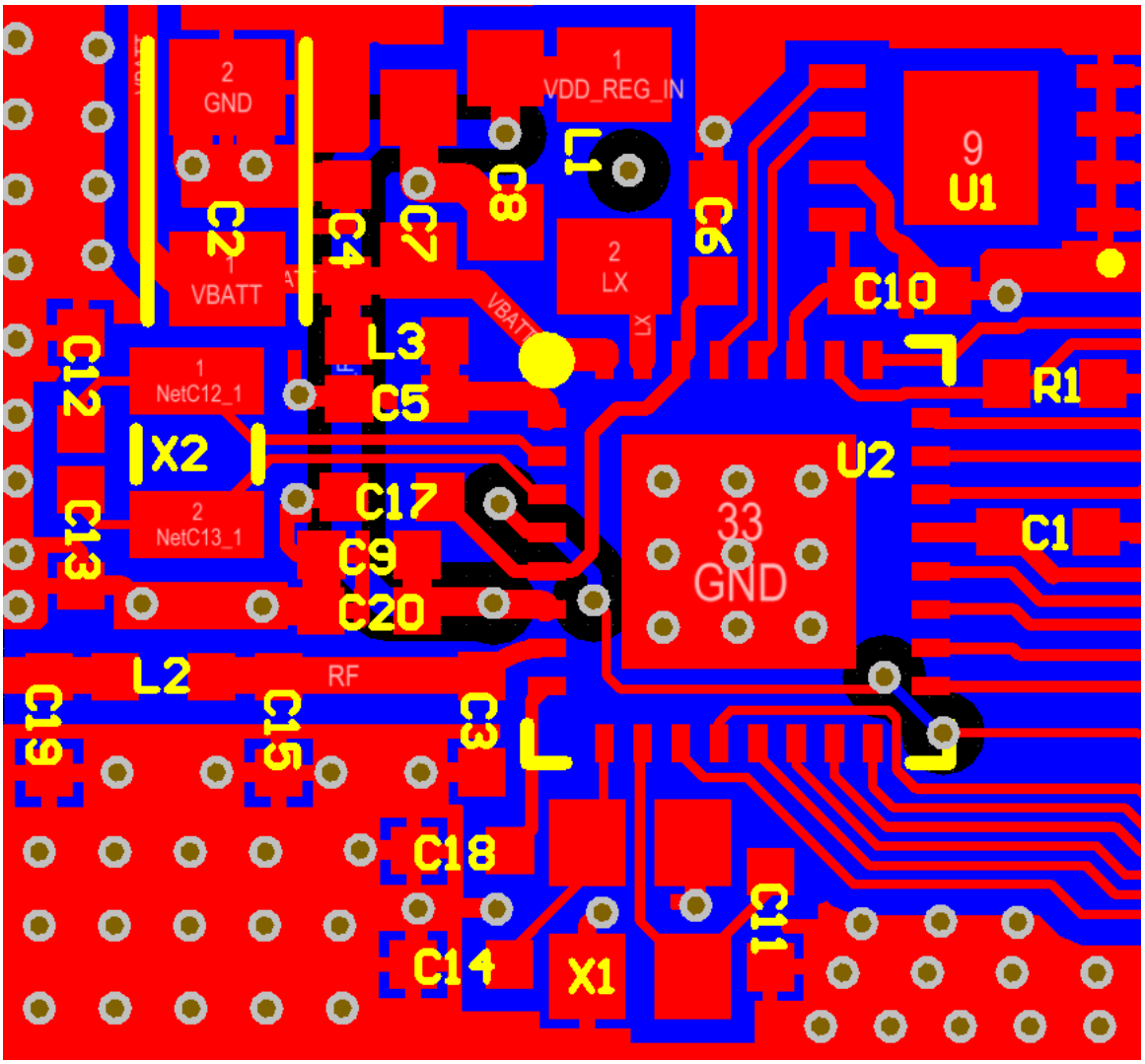

Figure 3.2: Recommended Layout with Two-Layer PCB (4.3V max.)

Note:

C7 and C8 change from 2.2uF (0402) to 4.7uF (0603) and add C20 (2.2uF) in parallel with C9 (470nF) and close to VDD_ VREG_IN port.

4. Project Details

Project / Code	
Module [or] COB	
PCB Revision	
End Customer	
End Application	
Remarks	

Table 4.1: Project Details

Document Reference

Document	Reference
CSR1012 QFN Data Sheet	CS-238833-DS
BTLE training part 3 sept 2011	www.csrsupport.com

Terms and Definitions

AIO	Analogue Input/Output
BPF	Band Pass Filter
CLK	Clock
CSR	Cambridge Silicon Radio
DC	Direct Current
e.g.	exempli gratia, for example
EEPROM	Electrically Erasable Programmable Read Only Memory
FAE	Field Application Engineer
GND	Ground
GPIO	General Purpose Input Output
I/O	Input/Output
I2C	Inter-Integrated Circuit Interface
IC	Integrated Circuit
MISO	Master In Slave Out
MOSI	Master Out Slave In
PCB	Printed Circuit Board
PIO	Parallel Input/Output

AIO	Analogue Input/Output
QFN	Quad Flat Non-Lead Package
RF	Radio Frequency
ROM	Read-Only Memory
RX	Receiver
SCL	Serial Clock Line
SDA	Serial Data (line)
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter
XTAL	Crystal