

CSR CSR101x hardware design guidelines



This Session



- Hardware design
 - Hardware design guidelines
 - Bringing up the new board
- Production line test
- Bluetooth qualification process



Hardware design guidelines

CSR101x Reference schematic







The selection of the power supply components is critical to getting optimal efficiency out of the switch mode power supply and in maximising battery life.



CSR1010 (4V3) SMPS Layout Routing

- C7 and C8 need an individual ground via separate from other grounds on top-layer (component side)
- C19 and C9 near VDD_REG_IN



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SPI_PIO#_SEL



- Insert a 47kΩ pull-down resistor on SPI_PIO#_SEL if PIO is selected. Please don't leave the port open even in PIO mode
- Add the VCC on SPI_PIO#_SEL to enable debug SPI mode on PIO[5..8]



Crystal circuit

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The values of 16MHz XTAL tank capacitors are in the ratio **2:1** (recommended 15pF:6.8pF). Have the **smaller** capacitor **on XTAL_IN**





CSR101x simple RF filter



A simple RF filter (a 0.5pF) is good enough to pass FCC, ETSI and TELEC



		CSR1011 Demo-Board		DUT1		DUT2		DUT3	
		0R	0R+0.5pF	0R	0R+0.5pF	0R	0R+0.5pF	0R	0R+0.5pF
TX Spurious	2nd Harmonic	-40.95	-47.03	-38.68	-43.46	-37.06	-50.19	-39.45	-48.26
Emissions (dBm)	3nd Harmonic	-45.41	-49.33	-55.94	-51.34	-50.81	-54.64	-51.6	-55.49

CSR101x ground



- Need to add the ground pin in the schematic and assign to CSR101x central ground pad in the layout
- CSR1010 and CSR1012 require at least 9 vias on the central ground pad
- CSR1011 requires at least 25 vias on the central ground pad
- Failure to do so can cause significant RF performance degradation









- The CSR101x does not have an internal pull-up or pull-down resistor on the WAKE pin therefore an external resistor should be used
- Hardware detects WAKE level change only
- WAKE pin mode is configurable with the Power Management API



EEPROM or SPI Flash circuit





Figure a: Example of an I2C Interface EEPROM Connection



Figure b: Example of an SPI Interface Flash Connection

Default PIO[3] is SPI Flash_DIN Default PIO[4] is SPI Flash _CS

Hardware Review



CSR Support:

R	Review Templates	Rename this section \cdot Move this section		
	CSR1012 HW review template	CSR1012 Hardware design review template Last updated: 26 Feb 2014, 02:50	Download 727.9 KB	Move this document Remove
	CSR1000/CSR1010 HW review template	CSR1000/CSR1010 Hardware design review template Last updated: 26 Feb 2014, 03:00	Download 682.9 KB	Move this document Remove
	CSR1001 HW review template	CSR1001 HW design review template Last updated: 24 Sep 2012, 17:00	Download 791.1 KB	Move this document Remove

- There is a review template for each component
- Regularly updated to add additional test cases
- Comprehensive step-by-step schematic and layout guidelines
- Recommended reading before embarking on a new schematic/layout design
- When CSR provide design reviews, they are usually in the form of a completed review template



- *CSR Support in the uEnergy section under Hardware.
- *Access to CSR Support is based on development kit registration and account verification.
- The Hardware Review Template is used internally by CSR to verify that components and layouts have been implemented according to CSR's recommendations.





Bringing up a new board



Bringing up a new board

Checking the power domain

- 1. VBAT :4.4V~1.8V
- 2. VDD_REG_IN: 1.35V~0.8V
- 3. VDD_CORE:1.2V~0.65V
- 4. PIO2: Based on PADS





If VDD_CORE and PIO2 don't show the correct voltage, check that the 32.768KHz clock is running



Check the Crystal Frequency



Check 16MHz and 32.768KHz clocks





Check SPI_PIO#_SEL state and pull high to enable debug SPI mode on PIO[5-8]





Production line test

CSR µEnergy boards

• Development Boards

CSR1011

DB-CSR1011-10139-1A DK-CSR1011-10138-1A (kit)

- USB-SPI Interface Board
 - Included with the development kits
 - Also available separately
 - Part number: DK-CSR1000-10086-1A



DB-CSR1010-10137-1A DK-CSR1010-10136-1A (kit)







CSR µEnergy Starter Development kit



DK-CSR1010-10169-1A

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Gang Programmer

- Supports up to 16 devices simultaneously
- Supports Flash devices using TestFlash DLL
- Supports EEPROM configuration using TestE2 DLL
- Increases throughput for production





Multi-way USB using USB hub



Tools support up to 16 instances of CNS10020V2A Interface Board



Low cost programmer board



Development Board

- Part Number: DK-USB-SPI-10225-1A
- Price: USD \$15
- Description: USB to Debug SPI
- Availability
 - Q1 2015
 - Via all CSR authorized distributors



Low cost programmer board



LED Power 26



- Board size: 35mm x 28mm
- Debug SPI header (connector type: 7-way 0.1" pitch header)
- Mounting holes 3.3mm hole with 22mm centre
- LEDs for SPI activity, Power and Error status indication
- USB Mini
- Board H13516V1

Debug SPI Header 300 CLK CON2 **10SI** USB Mini 1150 SPI SPI LEDs SPI and Error status indicator

ERR

Mounting hole 3.3mm

Mounting hole 3.3mm

CSR µEnergy Test Tool



- Choose the correct "PTest firmware"
- CsKeys affect the RF testing result

uEnergyTest Connection Settings		
SPI Transport:		Tester Interface Mode
Ptest Firmware:		Enable 🔽
C:\Program Files (x86)\CSR\uEnergy Too	ols 2.3.0\ptest_CSR101x.xbv Brow	vse Tester Interface
Configuration Settings Source C Ptest Firmware Defaults C Chip Non-Volatile Memory	Chip NVM Type © EEPROM © SPI Flash	Port: COM1 Baud Rate (kbps): 115200
CS Source File	Brows	Protocol:
	OK Cancel	

Note: CSR μ Energy PTest firmware is released as part of the CSR μ Energy Tools, and is downloaded to RAM on the CSR101x ICs to enable RF and other hardware test modes

CSR µEnergy Test Application Tool



- Application for testing of the board
- Various test functions available
 - RF functions
 - PIO Get/Set
 - AIO Get/Set
 - LED Set
 - UART Loopback
- "Reconnect" will show connection dialog then stop and reset chip after connection parameters selected
- "Cold Reset" will re-load same firmware and configuration as before without showing connection dialog

📓 uEnergyTest					
Test Mode CW TRANSMIT CRYSTAL TRIM SET RADIO STOP PACKET TRANSMIT RECEIVE PIO SET PIO SET AIO SET AIO SET LED SET	Test Arguments Channel (0-39) Freq. Override (MHz) 0	Close Execute Cold Reset			
Percent Test Results Save to file Browse for file Display : Standard PER .Vlogfile.txt Opening USB SPI (1). Transport active CSR100x (Hardware ID 0x402B) ptest firmware loaded Build ID = 176 (0x80) Build Info = rob_SDK_1_3_ptest_1111161527_gcc 2011-11-16 CS Version ID = 60 (0x3C)					

Crystal trim



 Trimming the crystal is an important part of the configuration of CSR101x design. A board with incorrect crystal trim value may suffer from poor RF performance (range, carrier frequency drift, sensitivity) that will affect the overall operation of the device



CLOAD1 and CLOAD2 in combination with CTRIM and any parasitic capacitance provide the load capacitance required by the crystal



- Direct Test Mode is used to control the Device Under Test (DUT) and provides a report back to the Tester
- Direct Test Mode shall be set up using one of two alternate methods:
 - 1. over HCI or
 - 2. through a 2-wire UART interface



Direct test mode



- The unit under test needs the CSR Direct test mode firmware to be loaded into it or for the same API calls to be built into the customer application
- To use a direct test, UART TX and RX test points are required on the PCB



An example Direct Test Mode application project is available as an example app within the SDK

CSR Tester Interface



 Debug SPI could be also used for RF testing – for designs that lack spare PIOs or test points for UART interface





Qualification for Bluetooth 4.1



- Bluetooth 4.1 improves usability for consumers, empowers innovation for product developers and extends the technology's foundation as an essential link for the Internet of Things
- The qualification process remains the same for all Bluetooth specifications
- Core Specification versions 2.0 +EDR, 2.1+EDR, 3.0+HS and 4.0 are still available for use and qualification

Qualification for Bluetooth 4.1



• SIG RF LE Test Cases

Test Case/Parameter	Temperature	Power Supply
TRM-LE/CA/01/C (Output power at NOC)	Nominal	Nominal
TRM-LE/CA/02/C (Output power at EOC)	Max/Min	Max/Min
TRM-LE/CA/03/C (In-band emissions at NOC)	Nominal	Nominal
TRM-LE/CA/04/C (In-band emissions at EOC)	Max/Min	Max/Min
TRM-LE/CA/05/C (Modulation characteristics)	Nominal	Nominal
TRM-LE/CA/06/C (Carrier frequency offset and drift at NOC)	Nominal	Nominal
TRM-LE/CA/07/C (Carrier frequency offset and drift at EOC)	Max/Min	Max/Min
RCV-LE/.CA/01/C (receiver sensitivity at NOC)	Nominal	Nominal
RCV-LE/.CA/02/C (receiver sensitivity at EOC)	Max/Min	Max/Min
RCV-LE/CA/0A/C (C/I- and selectivity performance)	Nominal	Nominal
RCV-LE/CA/04/C (Blocking performance)	Nominal	Nominal
RCV-LE/CA/05/C (Intermodulation performance)	Nominal	Nominal
RCV-LE/CA/06/C (Maximum input signal level)	Nominal	Nominal
RCV-LE/CA/07/C (PER Report Integrity)	Nominal	Nominal

NOC = Normal Operating Condition EOC = Extreme Operating Condition

Note: Test cases in red require complex or expensive resources and are often omitted for pre-production line testing



New listing process from February 2014

- Discontinuing the QDID fee
- A new listing fee either USD \$8000 or USD \$4000 depending on membership level
- Issuing a Declaration ID as your proof of purchase
 - The Declaration ID is a unique identification number assigned to a listing and used as a reference for the member's Declaration of Compliance (DoC)
- Simple Listing Process
 - 1. Create Qualification Project (new designs)
 - 2. Pay listing fee
 - 3. Reference a qualified design (QDID)
 - 4. List associated product(s)

The streamlined qualification and listing process



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Push every boundary.®