DATA SHEET

User Guide

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CONTENTS

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1 INTRODUCTION

The 74HC/HCT/HCU family is a comprehensive range of high-speed CMOS (HCMOS) integrated circuits. Whilst retaining all the advantages of CMOS technology - wide operating voltage range, very low power consumption, high input noise immunity and wide operating temperature range - these circuits have the high-speed and drive capabilities of low-power Schottky TTL (LSTTL). An extensive product range (most TTL functions and some devices from the successful HE4000B series: analog multiplexers, long time-constant multivibrators, phase-locked loops) and the aforementioned performance open new avenues in system design.

For comparison, the key performance parameters of HCMOS are shown with those of other technologies in Table 1. The propagation delay of metal-gate CMOS ruled out CMOS for many applications until the arrival of our HE4000B series. Now, our 3 μm gate HCMOS technology has a speed comparable to LSTTL while retaining the important CMOS qualities, see Fig.1.

Table 2 compares the operating characteristics of the 74HC and 74HCT IC types with those of LSTTL in more detail. 74HC and 74HCT devices are ideal for use in new equipment designs and, as alternatives to TTL devices, in existing designs. The 74HCT circuits which are direct replacements for LSTTL circuits also enhance performance in many respects.

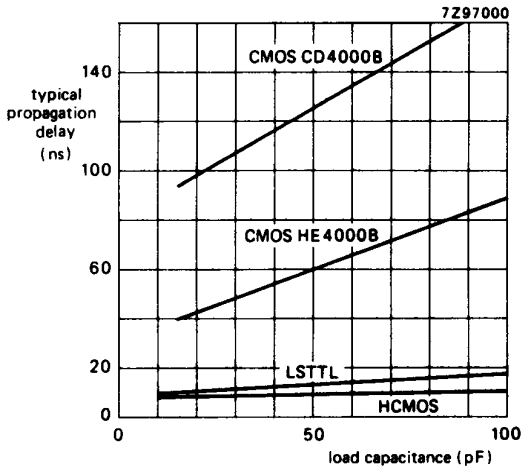

Fig.1 Propagation delay as a function of load capacitance; V_{CC} = 5 V, T_{amb} = 25 °C.

Table 1 Comparison of CMOS and TTL technologies; supply voltage V_{CC} = 5 V; ambient temperature T_{amb} = 25 °C; load capacitance C_L = 15 pF

parameters \ technology		HCMOS	metal gate CMOS		standard TTL	low-power Schottky TTL	Schottky TTL	advanced low-power Schottky TTL	advanced Schottky TTL	Fairchild advanced Schottky TTL
family		74HC	4000 CD	4000 HE	74	74LS	74S	74ALS	74AS	74F
Power dissipation, typ. (mW)										
Gate	static	0.0000025	0.001		10	2	19	1.2	8.5	5.5
	dynamic @100 kHz	0.075	0.1		10	2	19	1.2	8.5	5.5
Counter	static	0.000005	0.001		300	100	500	60	–	190
	dynamic @100 kHz	0.125	0.120		300	100	500	60	–	190
Propagation delay (ns)										
Gate	typical	8	94	40	10	9.5	3	4	1.5	3
	maximum	14	190	80	20	15	5	7	2.5	4
Delay/power product (pJ)										
Gate	at 100 kHz	0.52	9	4	100	19	57	4.8	13	16.5
Maximum clock frequency (MHz)										
	typical	55	4	12	25	33	100	60	160	125
D-type flip-flop										
	minimum	30	2	6	15	25	75	40	–	100
Counter	typical	45	2	6	32	32	70	45	–	125
	minimum	25	1	3	25	25	40	–	–	100
Output drive (mA)										
	standard outputs	4	0.51	0.8	16	8	20	8	20	20
	bus outputs	6	1.6		48	24	64	24	48	64
Fan-out (LS-loads)										
	standard outputs	10	1	2	40	20	50	20	50	50
	bus outputs	15	4		120	60	160	60	120	160

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Table 2 Comparison of HCMOS and LSTTL circuits (V_{CC} = 5 V unless stated otherwise; C_L = 50 pF)

characteristic	**74HCXXX (note 1) 74HCTXXX**	**74LSXXX**
Max. quiescent power dissipation over temp. range at V_{CCmax}		
per gate (mW)	0.027	6
per flip-flop (mW)	0.11	22
per 4-stage counter (mW)	0.44	175
per transceiver/buffer (mW)	0.055	60
Max. dynamic power dissipation (C_L = 50 pF)		
at f_i (MHz)	0.1 1 10	0.1 to 1 10
per gate (mW)	0.25 2.25 22	6 22
per flip-flop (mW)	0.35 2.5 24	22 27
per 4-stage counter (mW)	0.70 3 27	175 200
per buffer/transceiver (mW)	0.30 2.5 24	60 90
Operating supply voltage (V)	2 to 6 (HC) 4.5 to 5.5 (HCT)	4.75 to 5.25
Operating temperature range (°C)	–40 to +85 –40 to +125	0 to +70
Max. noise margin (V_{NMH}/V_{NML} V; I_{OHCMOS} = 20 μA; I_{OLSTTL} = 4 mA)	1.4/1.4 (HC) 2.9/0.7 (HCT)	0.7/0.4
Input switching voltage stability over temp. range	±60 mV	±200 mV
Min. output drive current at $T_{amb\ max}$ and V_{CCmin} (mA)		
source current (V_{OH} = 2.7 V; note 2)		
standard logic	–8	–0.4
bus logic	–12	–2.6
sink current		
standard logic (V_{OL} = 0.4 V)	4	4
standard logic (V_{OL} = 0.5 V)	6	8
bus logic (V_{OL} = 0.4 V)	8	12
bus logic (V_{OL} = 0.5 V)	9	24
Typ. output transition time (ns) (C_L = 15 pF)		
standard logic		
t_{TLH}	6	15
t_{THL}	6	6
bus logic		
t_{TLH}	4	15
t_{THL}	4	6
Typ. propagation delay (ns) (C_L = 15 pF; note 3)		
gate t_{PHL}/t_{PLH}	8/8	8/11
flip-flop t_{PLH}	14	15
t_{PHL}	14	22
Typ. clock rate of a flip-flop; note 5 (MHz)	50	33

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characteristic	74HCXXX (note 1) 74HCTXXX	74LSXXX
Max. input current (μA)		
I_{IL}	–1	–400 to –800
I_{IH}	1	40
3-state output leakage current (± μA)	5	20
Reliability (%/1000 h at 60% confidence level)	0.0005	0.008 (note 4)

Notes

1. Data valid for HCMOS between –40 °C and +85 °C.
2. V_{OH} for a few LSTTL bus outputs is specified as 2.4 V.
3. Refer to data sheets for the effect of capacitive loading.
4. RADC report.
5. Measured with a 50% duty factor for HCMOS. For LSTTL, per industry convention, the maximum clock frequency is specified with no constraints on rise and fall times, pulse width or duty factor.

2 CONSTRUCTION

Our HCMOS family is a result of a continuing development programme to enhance the proven polysilicon-gate CMOS process. Figure 2 shows the construction of a basic inverter from the HE4000B series and its HCMOS successor.

The polysilicon gate of a HCMOS transistor is deposited over a thin gate oxide before the source and drain diffusions are defined. Source and drain regions are formed using ion implantation, with the polysilicon gates acting as masks for the implantation. The source and drain are automatically aligned to the gate, minimizing gate-to-source and gate-to-drain capacitances. In addition, the junction capacitances, which are proportional to the junction area, are reduced because of the shallower diffusions. Figure 3(c) shows the parasitic capacitances in a CMOS inverter.

In a metal-gate CMOS transistor, the source and drain are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. This is why a metal-gate CMOS transistor has a higher overlap capacitance than an HCMOS transistor. Furthermore, the deeper diffusions of metal-gate CMOS make the junction capacitance larger.

In a silicon-gate MOS transistor, there are three interconnect layers (diffusion, polysilicon and metal) instead of the two layers (diffusion and metal) in a metal-gate MOS transistor. This makes a silicon-gate MOS transistor more compact. The shorter gate length means higher drive capability, which in turn increases the speed at which a silicon-gate MOS transistor can charge or discharge junction capacitance. The drain current of a saturated MOS transistor which determines the speed of the transistor is:

$$I_{DS} = \frac{-\beta}{2} \times \frac{\text{gate width}}{\text{gate length}} \times (\text{gate voltage} - \text{threshold voltage})^2$$

where β is the current gain factor which is proportional to the thickness of the oxide layer.

The threshold voltage is typically 0.7 V for HCMOS.

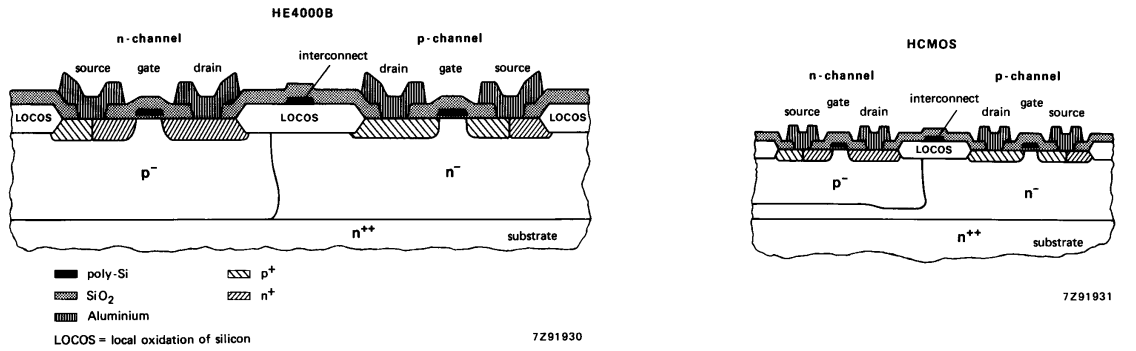


Fig.2 Basic inverter (left) in HE4000B CMOS, 6 μm gate, and (right) in HCMOS, 3 μm gate.

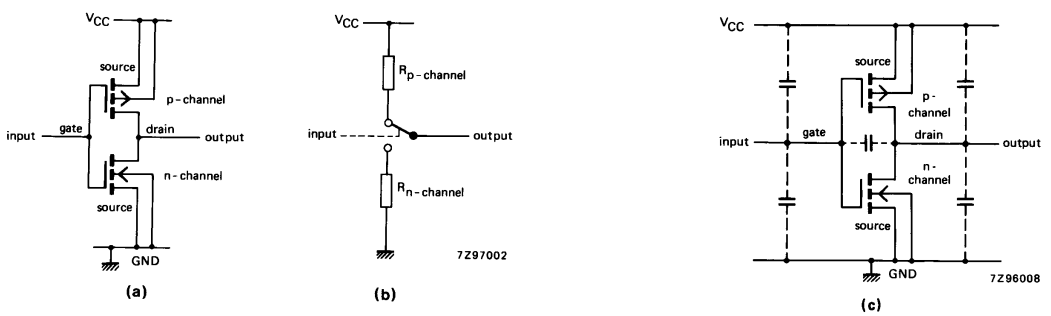


Fig.3 (a) Basic CMOS inverter; (b) electrical equivalent; (c) parasitic capacitances in a CMOS inverter.

3 AC CHARACTERISTICS

3.1 Test conditions

The propagation delays and transition times specified in the HCMOS data sheets are guaranteed when the circuits are tested according to the conditions stated in the chapter 'Family Characteristics', section 'Family Specifications'. For some circuits such as counters and flip-flops, the test conditions are defined further by the a.c. set-up requirements specified in the data sheet.

Values given in the data sheets are for the whole operating temperature range (–40 to +125 °C) and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for 74HC devices, and 4.5 V for 74HCT devices. This is a much tougher specification than that commonly used for LSTTL, where the characteristics are usually only specified at 25 °C and for a 5 V supply. Furthermore, the published a.c. characteristics of HCMOS are guaranteed for a capacitive test load of 50 pF, a more realistic load than the 15 pF specified for LSTTL and one that loads the device as the output switches. The published values for HCMOS are therefore representative of those measured in actual systems.

3.2 Comparing the speed of HCMOS and LSTTL

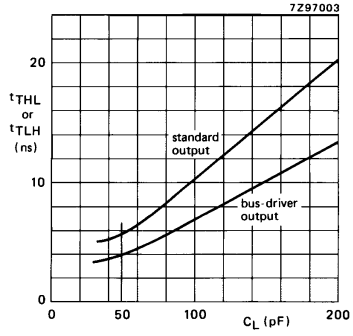
A feature of a HCMOS circuit is its speed - in general, comparable to that of its LSTTL equivalent. Owing to the different (more informative) way of specifying data for HCMOS devices, it will be useful to indicate how to compare the published data for HCMOS and LSTTL.

For example, in an LSTTL specification, the use of a 15 pF load instead of a 50 pF one means the maximum propagation delays and enable times published for the LSTTL device will be up to 2.5 ns (typ. 1.3 ns) shorter than those for the HCMOS equivalent. In addition, measuring at the nominal LSTTL supply voltage of 5 V instead of 4.5 V (HCMOS) reduces propagation delays and enable times by a further 10%. So, a 30 ns propagation delay for a HCMOS device is equivalent to a (30 – 2.5) 0.9 = 25 ns delay for an LSTTL device measured at 4.5 V and with a 15 pF load.

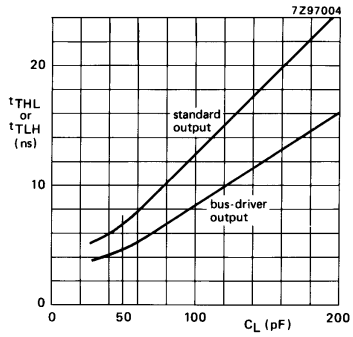
Disable times are measured under different test conditions too - for HCMOS with a 50 pF, 1 kΩ load, for LSTTL with a 5 pF, 2 kΩ load or for a 45 pF, 667 Ω load. To compare a HCMOS disable time with that for a LSTTL device with a 5 pF load, subtract 4 ns from the published HCMOS disable time and multiply by 0.9. To compare a value for a 45 pF load, subtract 2 ns and multiply by 0.9. For example, a 30 ns HCMOS disable time is equivalent to (30 – 4) 0.9 = 23 ns for a 5 pF load and (30 - 2) 0.9 = 25 ns for a 45 pF load.

Set-up hold and removal times are not affected by output load, only by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the HCMOS value by 0.9.

(a) V_{CC} = 6 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 2 V

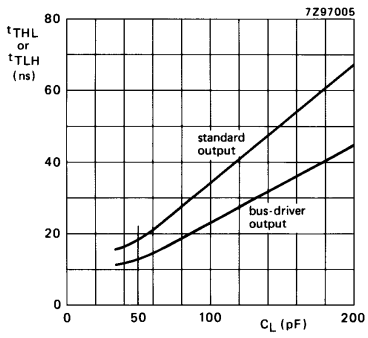


Fig.4 Typical output transition times as a function of load capacitance; T_{amb} = 25 °C; for 74HCT circuits the data at V_{CC} = 4.5 V only is valid.

Operating frequency is also unaffected by output load, but is affected by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the value for HCMOS at 4.5 V by 1.1.

In general, these guidelines apply both to 74HC and to 74HCT devices. For 74HCT devices however, the propagation delay is the time for the output to reach 1.4 V (compared with 50%V_{CC} for 74HC devices), so HIGH-to-LOW output transition times are slightly more dependent on load and the LOW-to-HIGH transition times are slightly less dependent on load than the 74HC versions.

3.3 Propagation delays and transition times

The symmetrical push-pull output structure of both 74HC and 74HCT devices gives symmetrical rise/fall times and provides for a well-balanced system design. Table 3 shows the maximum output transition times for all standard and bus-driver HCMOS outputs.

The influence of capacitive loading on output transitions is shown in Fig.4; A good approximation of the output transition times can be calculated using the data of Table 4.

Table 3 Maximum output transition times (C_L = 50 pF)

		maximum output transition time (ns)		
	V_{CC} (V)	T_{amb} = 25 °C	T_{amb} = 85 °C	T_{amb} = 125 °C
standard	2	75	95	110
output	4.5[1]	15	19	22
	6	13	16	19
bus-driver	2	60	75	90
output	4.5[1]	12	15	18
	6	10	13	15

Note

1. 74HC and 74HCT devices; all other data for 74HC devices only.

Table 4 Typical output transition times for load capacitances greater than the standard 50 pF load, see Fig.4

V_{CC}	t_{THL} or t_{TLH}	
	standard output	bus-driver output
2.0 V	18.5 ns + 0.32 ns/pF	12.5 ns + 0.22 ns/pF
4.5 V	6.6 ns + 0.12 ns/pF	4.5 ns + 0.077 ns/pF
6.0 V	5.6 ns + 0.10 ns/pF	3.8 ns + 0.065 ns/pF

Note

1. values in pF are the load capacitance minus 50 pF.

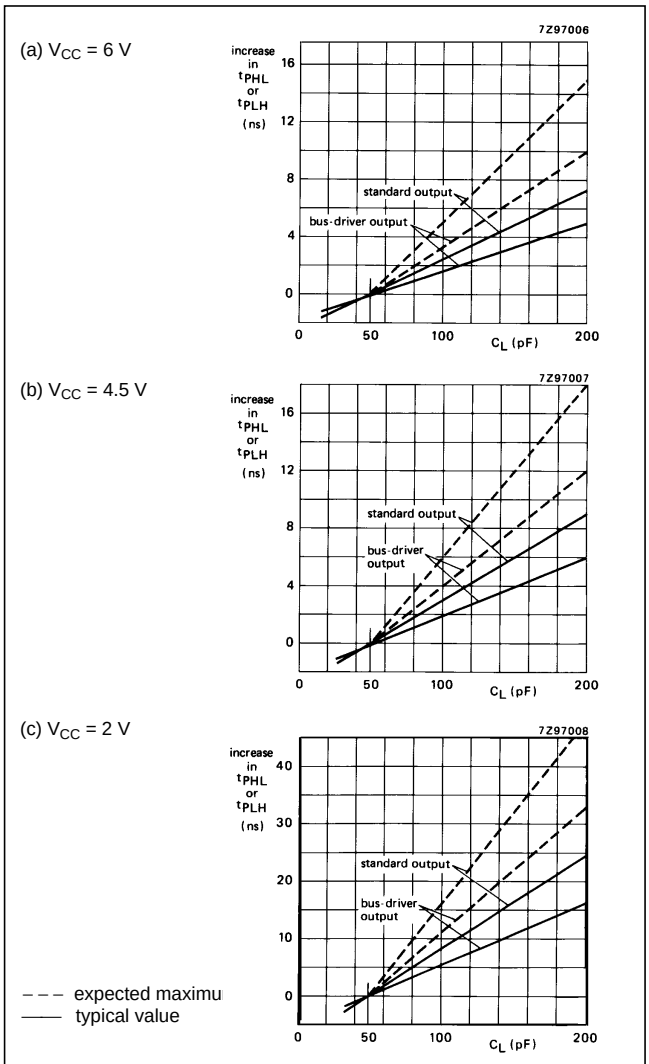


Fig.5 Increase in propagation delay for 74HC devices as a function of load capacitance; T_{amb} = 25 °C.

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A parameter specified for TTL devices is the output short-circuit current HIGH (I_{OS}). Originally intended to reassure the TTL user that the device would withstand accidental grounding, this parameter has become a measure of the ability of the circuit to charge the line capacitance and is used to calculate propagation delays. In CMOS devices however, there is no need to specify I_{OS} because the purely capacitive loads allow extrapolation of the a.c. parameters over the whole loading range. Figure 5 (for 74HC devices) and Fig.6 (for 74HCT devices) show the increase in propagation delay for loads greater than 50 pF. The additional delay can be calculated from the output saturation current (short-circuit current). Referring to the output characteristics (Figs 33 to 36), the propagation delay is the time taken for the output voltage to reach 50% of V_{CC} for 74HC devices, or 1.4 V for 74HCT devices. Since a saturated output transistor acts as a current source, the additional delay is $\Delta CV/I$, where ΔC is the load capacitance minus 50 pF, V is the voltage swing at the output to the switching level of the next circuit, and I is the average source current of the saturated output.

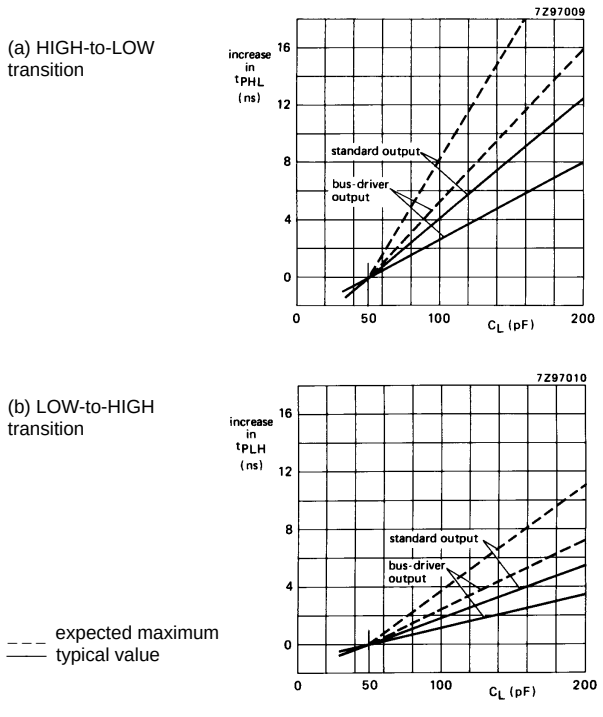

Fig.6 Increase in propagation delay for 74HCT devices as a function of load capacitance; the different values for t_{PHL} and t_{PLH} are due to the asymmetrical reference level of 1.3 V at the outputs; T_{amb} = 25 °C; V_{CC} = 4.5 V.

3.3.1 *SUPPLY VOLTAGE DEPENDENCE OF PROPAGATION DELAY*

The dynamic performance of a CMOS device depends on its drain characteristics. These are related to the switching thresholds and the gate-to-source voltage V_{GS} which is equal to the supply voltage V_{CC}. A reduction in V_{CC} adversely affects the drain characteristics, increasing the propagation delays.

Over the supply voltage range of 74HCT devices, 4.5 V to 5.5 V, the effects of different propagation delays on performance are minimal. Over the supply voltage range of 74HC circuits, 2 to 6 V, the effects on performance are significant, see Figs 7 and 8.

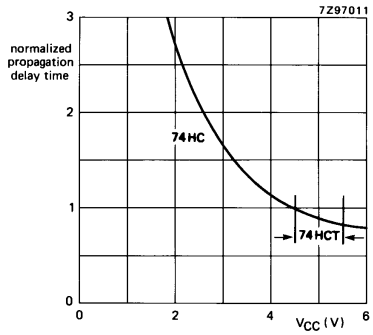

Fig.7 Propagation delay as a function of supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

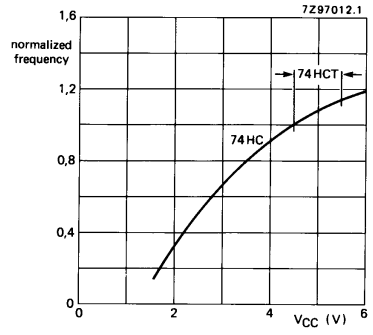

Fig.8 Operating frequency as a function of supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

3.3.2 *TEMPERATURE DEPENDENCE OF PROPAGATION DELAY*

In TTL circuits, β (current gain), internal resistances and forward-voltage drops are all temperature-dependent. In HCMOS circuits, essentially only the carrier mobility, which affects the propagation delay, is temperature dependent. In general, propagation delay increases by about 0.3% per °C above 25 °C.

Between 25 °C and 125 °C,

$t_P = t_P' (1.003)^{T_{amb}-25}$

where:
t_P' is the propagation delay at 25 °C,
T_{amb} is the ambient temperature in °C.

Between −40 °C and +25 °C,

$t_P = t_P'(0{,}997)^{25-T_{amb}}$

Figure 9 shows the temperature dependence of a characteristic such as propagation delay.

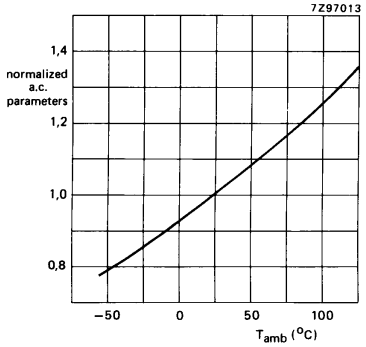

Fig.9 Typical influence of temperature on AC parameters; V_{CC} = 5 V.

3.4 Derating system for AC characteristics

Because HCMOS devices are a coherent family, manufactured under strictly-controlled conditions, it is possible to have a common set of derating coefficients for temperature and supply voltage that is valid for all AC characteristics of all devices. Table 5 shows the derating coefficients which are derived from the published values of the AC characteristics at 25 °C for V_{CC} = 4.5 V, denoted by x in the Table. The coefficients have been established after extensive high-temperature testing at many supply voltages. A temperature coefficient of −0.4%/°C was established after comparing the test results with worst-case calculations. The voltage derating given in Table 5 is conservative compared with that shown in Fig.7 for propagation delay. For operating frequencies (Fig.8), the reciprocal of the derating coefficients shown should be used.

Table 5 Derating coefficients for the AC characteristics of HCMOS devices

supply voltage	ambient temperature		
	25 °C	85 °C	125 °C
2 V	5 (5x)	6.25 (5y)	7.5 (5z)
4.5 V[1]	1 (x)	1.25 (y = 1.25x)	1.5 (z = 1.5x)
6 V	0.85 (0.85x)	1.0625 (0.85y)	1.275 (0.85z)

Note

1. 74HC and 74HCT devices; all other data for 74HC devices only.

All coefficients are derived from the value of the AC characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

3.5 Clock pulse requirements

All HCMOS flip-flops and counters contain master-slaves with level-sensitive clock inputs. When the voltage at the clock input reaches the voltage threshold of the device, data in the master (input) section is transferred to the slave (output) section. The threshold for 74HC devices is typically 50% of V_{CC} and that for 74HCT devices is 28% of V_{CC} (1.4 V at V_{CC} = 5 V). The thresholds are virtually independent of temperature.

The use of voltage thresholds for clocking is an improvement over a.c. coupled clock inputs, but it does not make the devices totally insensitive to clock-edge rates. When clocking occurs, the internal gates and output circuits of the device dump current to ground, producing a noise transient that is equal to the algebraic sum of the internal and external ground plane noise. When a number of loaded outputs change simultaneously, the device ground reference (and therefore the clock reference) can rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at or near to its threshold during a noise transient, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the published maximum (500 ns at V_{CC} = 4.5 V).

In the HCMOS family, all the J-K flip-flops have a Schmitt-trigger circuit at the clock input, which eliminates the need to specify a maximum rise/fall time. The flip-flops 74HC/HCT73, 74, 107, 109 and 112 have special

Schmitt-trigger circuits for increased tolerance to slow rise/fall times and ground noise.

The published maximum input clock frequency ratings for clocked devices are for a 50% duty factor input clock. At these rated frequencies, the outputs will swing between V_{CC} and GND, assuming no DC load on the outputs. This is a very conservative and reliable method of rating the clock-input-frequency limits for HCMOS devices which are always at least as good as those for LSTLL even though they may appear to be inferior. This is because the maximum operating frequency of a TTL device is published, not for a 50% duty factor clock, but for a minimum clock pulse width.

3.6 System (parallel) clocking

In synchronously-clocked systems, spreads in the clock threshold levels of devices can cause logic errors if slow clock edges are used. For example, if data in one circuit changes before the clock threshold of the next sequential circuit is reached, a logic error will occur, see Fig.10.

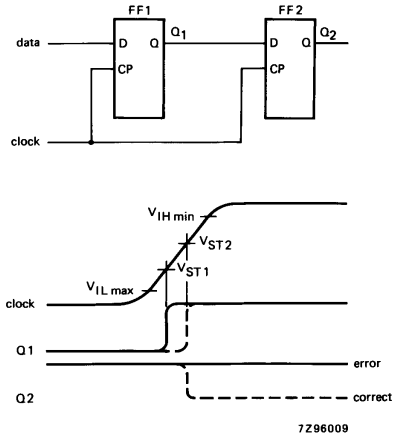

Fig.10 In synchronously-clocked systems, changing the data in one device before the clock switching threshold of the next has been reached can cause logic errors. V_{ST1} is the clock threshold of device 1; V_{ST2} is the clock threshold of device 2.

To prevent this type of logic error, the maximum rise or fall time of the clock pulse should be less than twice the propagation delay of the flip-flop.

For a HCMOS device, the rise/fall time must be limited to 1000, 500 or 400 ns for V_{CC} = 2 V, 4.5 V and 6 V respectively. If these times are exceeded, noise on the input or power supply rails may cause the outputs to oscillate during transitions, causing logic errors and excessive power dissipation.

3.7 Clock pulse considerations as functions of maximum frequency

The minimum input frequency is measured with a clock that has a 50% duty factor. For a stand-alone flip-flop, the following direct relationship exists between the minimum required width of the clock pulse $t_{w\,LOW}$ or $t_{w\,HIGH}$ (whichever is the longest) and the measured maximum frequency:

$$f_{max} = 1/2t_w$$

If two or more flip-flops are synchronously clocked in parallel, other timing conditions may cause a lower maximum frequency than that which can be calculated from the pulse width measurements. An example is shown in Fig.11.

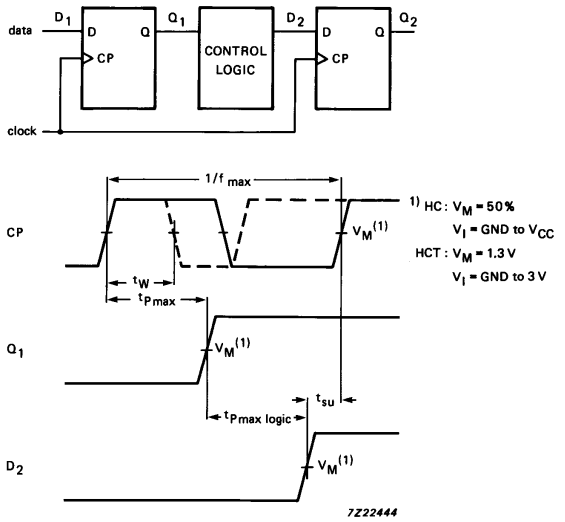

Fig.11 Timing conditions for parallel clocking.

The maximum frequency is now determined by:

$$f_{max} = \frac{1}{t_{P\,max}(\text{CP to } Q_1) + t_{P\,max}(\text{control logic}) + t_{su}(D_2 \text{ to CP})}$$

The measured minimum width (t_w) of the clock pulse as shown in Fig.11 would suggest a higher obtainable frequency in this example. This parallel clocking scheme is often encountered in counter circuits (e.g. ′160′ or ′190′ series).

If the internal delays and set-up times exceed the minimum required duration for the clock pulse, the maximum frequency will be entirely determined by these internal delays and set-up times.

Cascading HCMOS counters in a parallel clocking scheme may also result in lower maximum frequencies than those given for stand-alone ICs. This is because the frequency will then be determined by the propagation delay of a count output, for example the delay of the intermediate logic and the set-up time between the clock enable and the count input of the succeeding counter IC.

3.8 Minimum AC characteristics

Minimum propagation delays are not specified in the data sheets. However, an increasing number of HCMOS users are asking for minimum propagation delay values so that they can make conclusive data handling calculations. Since our test programs don't include lower limits for propagation delays, it's impossible for us to guarantee these values for the entire HCMOS family. However, propagation delays for the whole HCMOS family have been constantly monitored by our Quality Department over the past three years. The very small deviations from the typical values that were observed between May 1985 and February 1988 are shown, together with their three sigma values, in Fig.12. The indicated mean value $\bar{x}$ is within a few percent of the published typical values. Users can derive their own minimum expected values from this figure and the typical propagation delays published in the data sheets.

A conservative estimate of minimum propagation delay is one third of the typical value. For set-up and hold times, the guard-band which should be applied to obtain max./min. limits is 5 ns for typical values between the limits of –5 ns and +5 ns. For typical values beyond –5 ns and +5 ns, the distribution shown in Fig.12 applies.

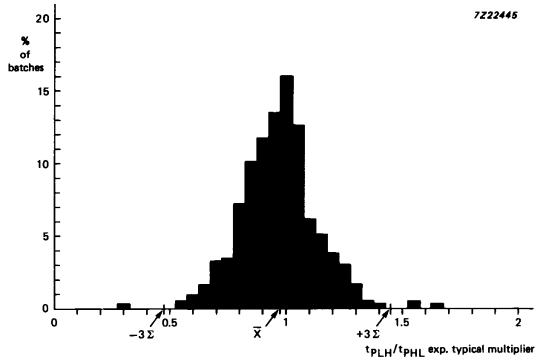

Fig.12 Batch-to-batch variation of propagation delay (t_{PLH}/t_{PHL}).

Table 6 gives the derating coefficients for calculating the minimum propagation delays of HCMOS devices at various supply voltages and temperatures.

Table 6 Derating coefficient for the expected minimum propagation delay of HCMOS devices

supply voltage	ambient temperature	
	25 °C	–40 °C
2 V	2 (2x)	1.67 (2y)
4.5 V[1]	1 (x)	0.83 (y = 0.83 x)
6 V	0.8 (0.8x)	0.66 (0.8y)

Notes

1. 74HC and 74HCT devices; all other data for 74HC devices only.
2. The minimum value is reached at the lowest possible temperature.

All coefficients are derived from the value of the AC characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

4 POWER DISSIPATION

4.1 Static

When a HCMOS device is not switching, the p-channel and n-channel transistors don't conduct at the same time,

so leakage current flows between V_{CC} and GND. Because this leakage current is typically a few nA, HCMOS power dissipation is extremely low.

Static power dissipation can be calculated for both 74HC and 74HCT devices from the maximum quiescent current specified in the data sheets, see Table 7.

Table 7 Maximum quiescent current of HCMOS devices at V_{CCmax} (1) ($V_I = V_{CC}$ or GND; $I_O = 0$)

device complexity	quiescent current typical at 25 °C	maximum 25 °C	maximum 85 °C	current 125 °C
SSI	2 nA	2 μA	20 μA	40 μA
FF	4 nA	4 μA	40 μA	80 μA
MSI	8 nA	8 μA	80 μA	160 μA
LSI	50 nA	50 μA	500 μA	1000 μA

Note

1. 6 V for 74 HC; 5.5 V for 74 HCT.

4.2 Dynamic

When a device is clocked, power is dissipated charging and discharging on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. However, this transient energy loss is typically only 10% of that due to parasitic capacitance.
The total dynamic power dissipation per device (P_D) is:

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \quad (1)$$

where:

- C_{PD} is the power dissipation capacitance per package
- f_i is the input frequency
- f_o is the output frequency
- C_L is the total external load capacitance per output.

The second term of equation (1) implies summing the product of the effective output load capacitance and frequency for each output. However, a good approximation of the total dynamic power dissipation of an HCMOS system can be obtained by summing the published C_{PD} values and load capacitance for the HCMOS devices used and, assuming an average frequency, using equation (1).

For one-shot circuits, gates configured as oscillators, phase-locked loops and devices used in a linear mode, additional dissipation is caused by static supply currents (I_{CC}) whose values are given in the device data sheets.

4.3 Power dissipation capacitance

C_{PD} is specified in the device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Fig.13. The worst-case operating conditions for C_{PD} are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. Table 8 gives the pin status for HCMOS devices during a C_{PD} test. Devices which can be separated into independent sections are measured per section, the others are measured per device.

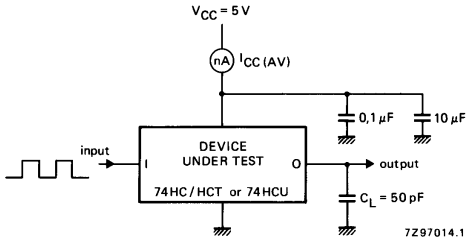

Fig.13 Test set-up for determining C_{PD}. The input pulse is a square wave between V_{CC} and GND; $t_r = t_f \leq 6$ ns; $T_{amb} = 25$ °C. All switching outputs are loaded with 50 pF (including test jig capacitance). Unused inputs are connected to V_{CC} or GND.

The recommended test frequency for determining C_{PD} is 1 MHz, but this is best increased to 10 MHz when I_{CC} is low and the device quiescent current influences $I_{CC(AV)}$. Loading the switched outputs gives a more realistic value of C_{PD}, because it prevents transient 'through-currents' in the output stages. Furthermore, automatic testers often introduce about 30 pF to 40 pF on each device pin.

The values of C_{PD} in the data sheet have been calculated using:

$$C_{PD} = \frac{I_{dyn(device)}}{V_{CC} f_i}$$

where:
$I_{dyn(device)} = I_{CC(AV)} - I_{dyn(load)}$
and
$I_{dyn(load)} = \Sigma(C_L V_{CC} f_o)$

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Table 8 Pin conditions for C_{PD} tests.

74HC/ HCT	equiv. load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
02	50	C	P	L	O	D	D	G	D	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
03	0	P	H	B	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
U04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
08	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
10	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
11	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
14	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
20	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
21	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
27	50	P	L	D	D	D	O	G	O	D	D	D	C	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
30	50	P	H	H	H	H	H	G	C	O	O	H	H	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
32	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
42	100	C	C	O	O	O	O	O	G	O	O	O	L	L	L	P	V	–	–	–	–	–	–	–	–	–	–	–	–
58	50	P	D	D	D	D	O	G	O	L	L	L	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
73	50	P	H	H	V	D	D	D	O	O	D	G	C	C	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
74	50	H	Q	P	H	C	C	G	O	O	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
75	50	C	Q	D	D	V	D	D	O	O	O	O	G	P	O	O	C	–	–	–	–	–	–	–	–	–	–	–	–
85	50	L	H	P	H	O	C	O	G	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
86	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
93	47	Q	L	L	D	V	D	D	C	C	G	C	C	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
107	50	H	C	C	H	O	O	G	D	D	D	D	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
109	50	H	H	L	P	H	C	C	G	O	O	D	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
112	50	P	H	H	H	C	C	O	G	O	D	D	D	D	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
123	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
125	50	L	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
126	50	H	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
132	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
133	50	P	H	H	H	H	H	H	G	C	H	H	H	H	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–

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74HC/ HCT	equiv. load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
137	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
138	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
139	100	L	P	L	C	C	O	O	G	O	O	O	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
147	50	H	H	H	H	H	O	O	G	C	H	P	H	H	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
151	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
153	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
154	100	C	C	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V	–	–	–	–
157	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
158	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
160	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
161	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
162	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
163	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
164	200	Q	H	C	C	C	C	G	P	H	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
165	50	H	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
166	25	Q	D	D	D	D	L	P	G	H	D	D	D	C	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
173	25	L	L	C	O	O	O	P	G	L	L	D	D	D	Q	L	V	–	–	–	–	–	–	–	–	–	–	–	–
174	25	H	C	Q	D	O	D	O	G	P	O	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–
175	50	H	C	C	Q	D	O	O	G	P	O	O	D	D	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
181	300	P	H	H	L	L	H	H	L	C	C	C	G	C	B	C	C	C	L	H	L	H	L	H	V	–	–	–	–
182	150	H	L	H	L	H	L	O	G	C	O	C	C	P	H	L	V	–	–	–	–	–	–	–	–	–	–	–	–
190	55	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
191	53	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
192	55	D	C	C	H	P	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
193	50	D	C	C	H	P	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
194	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

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195	125	H	H	L	D	D	D	D	G	H	P	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
221	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
237	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
238	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
240	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	C	D	–	–	V	–	–	–	–	–	–	–	–
241	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	C	D	–	–	V	–	–	–	–	–	–	–	–
242	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
243	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
244	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–	–	–
245	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–
251	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
253B	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
257	50	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
258	50	P	L	H	C	D	D	O	G	O	D	D	O	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
259	25	L	L	L	C	O	O	O	G	O	O	O	O	Q	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–
273	25	H	C	Q	D	O	O	D	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–
280	100	L	L	O	L	C	C	G	P	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
283	250	C	H	L	C	P	H	L	G	C	C	H	L	C	L	H	V	–	–	–	–	–	–	–	–	–	–	–	–
297	12	H	H	H	P	Q	L	C	G	D	D	O	O	D	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–
299	250	H	L	L	C	C	C	C	C	H	G	Q	P	C	C	C	C	C	D	L	V	–	–	–	–	–	–	–	–
354	100	D	D	D	D	D	D	L	H	L	G	L	L	L	P	L	L	H	C	C	V	–	–	–	–	–	–	–	–
356	50	D	D	D	D	D	D	D	Q	P	G	L	L	L	L	L	L	H	C	C	V	–	–	–	–	–	–	–	–
365	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
366	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
367	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
368	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
373	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
374	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
377	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
390	50	P	L	C	Q	C	C	C	G	O	O	O	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
393	47	P	L	C	C	C	C	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–

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74HC/ HCT	equiv. load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
423	100	L	P	H	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
533	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
534	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
563	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
564	25	L	Q	D	D	D	D	D	D	D	G	P	O	D	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
573	25	L	P	D	D	D	D	D	D	D	G	H	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
574	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
583	200	H	H	H	L	H	C	C	G	C	C	C	L	P	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–
594	225	C	C	C	C	C	C	C	G	C	H	P	P	H	Q	C	V	–	–	–	–	–	–	–	–	–	–	–	–
595	225	C	C	C	C	C	C	C	G	C	H	P	P	P	Q	C	V	–	–	–	–	–	–	–	–	–	–	–	–
597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
640	25	H	P	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
643	50	H	P	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
646	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
648	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
652	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
670	200	L	L	L	L	P	C	C	G	C	C	L	H	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
688	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–
4002	50	C	P	L	L	L	O	G	O	D	D	D	D	O	V	–	–	–	–	–	–	–							
4015	100	P	C	O	O	O	D	D	G	D	O	C	C	C	L	Q	V	–	–	–	–	–	–						
4016	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–							
4017	55	C	C	C	C	C	C	C	G	C	C	C	C	L	P	L	V	–	–	–	–	–	–						
4020	29	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–						
4024	48	P	L	C	C	C	C	G	O	C	O	C	C	O	V	–	–	–	–	–	–	–							
4040	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–						
4046A	50	O	C	L	O	H	O	O	G	L	O	O	O	O	P	O	V	–	–	–	–	–	–						
4049	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–						
4050	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–						

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74HC/ HCT	equiv. load (pF)	pin numbers 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
4051	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–						
4052	0	O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	–	–	–	–	–	–						
4053	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–						
4059	17	P	D	H	L	L	L	L	L	L	L	H	G	H	H	L	L	L	L	L	L	L	L	C	V	–	–		
4060[1]	106	C	C	C	C	C	C	C	G	C	C	P	L	C	C	C	V	–	–	–	–	–	–						
4066	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–							
4067	0	O	O	O	O	O	O	O	O	O	P	L	G	L	L	L	O	O	O	O	O	O	O	O	V	–	–		
4075	75	P	L	D	D	D	O	G	L	C	O	D	D	D	V	–	–	–	–	–	–	–							
4094	250	H	Q	P	C	C	C	C	G	C	C	C	C	C	C	H	V	–	–	–	–	–	–						
4316	0	O	O	O	O	P	D	L	G	G	O	O	O	O	D	D	V	–	–	–	–	–	–						
4351	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–				
4352	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–				
4353	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–				
4510	55	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–							
4511	200	L	L	H	H	L	L	P	G	C	C	O	O	C	O	C	V	–	–	–	–	–	–						
4514	100	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–		
4515	100	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–		
4516	50	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–						
4518	45	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–						
4520	47	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–						
4538	100	G	R	H	P	H	C	C	G	O	O	D	D	L	O	G	V	–	–	–	–	–	–						
4543	50	H	L	L	H	L	P	L	G	C	C	C	C	O	O	O	V	–	–	–	–	–	–						
5555	–	not applicable																											
6323A	7	C	O	O	G	O	O	P	V	–	–	–	–	–	–	–	–	–	–										
7014	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
7030	7	G	G	C	P	Q	Q	Q	Q	Q	Q	Q	Q	Q	G	L	C	C	C	C	C	C	C	C	C	C	P	H	V
7046A	50	O	C	L	O	H	O	O	G	L	O	O	O	O	P	O	V	–	–	–	–	–	–						
7080	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	C	V	–	–	–	–	–	–			
7132	–	not applicable																											
7245	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–			
7266	50	P	L	C	O	D	D	G	D	D	O	O	D	D	V	–	–	–	–	–	–	–							
7403	200	L	C	P	Q	Q	Q	Q	G	H	C	C	C	C	C	P	V	–	–	–	–	–	–						

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74HC/ HCT	equiv. load (pF)	pin numbers 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
7404	225	L	C	P	Q	Q	Q	Q	G	H	C	C	C	C	C	P	V	–	–	–	–	–	–						
7540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–				
7541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–				
7597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–					
7731	25	C	P	Q	L	D	D	O	G	O	D	D	D	D	D	O	V	–	–	–	–	–	–						
9014	50	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	V	–	–	–	–				
9015	50	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	V	–	–	–	–				
9046	–	not applicable																											
9114	0	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	B	V	–	–	–	–				
9115	0	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	V	–	–	–	–				
40102	5	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–						
40103	3	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–						
40104	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–						
40105	200	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	C	P	V	–	–	–	–	–	–						

Note

1. load word;

0:	0	0	0	0
1:	1	1	1	1
2:	X	X	X	X
3:	X	X	X	X

Key

V	=	V_{CC} (+5V)
G	=	ground
H	=	logic 1 (V_{CC}) - inputs at V_{CC} for HC types; 3.5 V for HCT types
L	=	logic 0 (ground)
D	=	don’t care - either H or L but not switching
C	=	a 50 pF load to ground is allowed
O	=	an open pin; 50 pF to ground is allowed
P	=	input pulse (see illustration)
Q	=	half frequency pulse (see illustration)
R	=	1 kΩ pull-up resistor to an additional 5 V supply other than the V_{CC} supply
B	=	both R and C.

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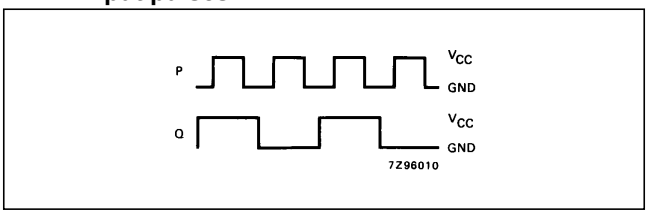
4.4 Input pulses



4.5 Conditions for C_{PD} tests

Gates. All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency. C_{PD} is specified per-gate.

Decoders. One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to V_{CC} or GND, whichever enables operation. C_{PD} is specified per-independent-decoder.

Multiplexers. One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With three-state multiplexers, C_{PD} is specified per output function for enabled outputs.

Bilateral switches. The switch inputs and outputs are open-circuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW. C_{PD} is specified per switch.

Three-state buffers and transceivers. C_{PD} is specified per buffer with the outputs enabled. Measurement is as for simple gates.

Latches. The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. Three-state latches are measured with their outputs enabled. C_{PD} is specified per-latch.

Flip-flops. Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at V_{CC} or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters. A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the device.

Arithmetic circuits. Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers. C_{PD} is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs.

If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits. In some cases, when the device I_{CC} is significant, C_{PD} is not specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a square wave. The timing resistor is tied to a separate supply (equal to V_{CC}) to eliminate its power contribution.

4.6 Additional power dissipation in 74HCT devices

When the inputs of a 74HCT device are driven by a TTL device at the specified minimum HIGH output level of V_{OH} = 2.4 V, the input stage p-channel transistor does not completely switch off and there is an additional quiescent supply current (ΔI_{CC}). This current has been considerably reduced by proprietary development of 74HCT input stages, see ′74HCT inputs′.

The value of ΔI_{CC} specified in the data sheets is per input and at the worst-case input voltage of V_{CC} – 2.1 V for V_{CC} between 4.5 and 5.5 V. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum V_{CC} and minimum V_{OH}), see Table 9.

The additional power dissipation P is:

$$P = V_{CC} \times \Delta I_{CC} \times \text{duty factor HIGH} \times \text{unit load coefficient}$$

The unit load coefficient for an input is a factor by which the value of ΔI_{CC} given in the data sheet has to be multiplied. A unit load coefficient is published for each 74HCT device. It is a function of the size of the input p-channel transistor.

Table 9 Worst-case additional quiescent supply current (ΔI_{CC}) for 74HCT devices

	T_{amb} (°C)				UNIT	TEST CONDITIONS		
	74HCT							
	+25		−40 to +85	−40 to +125		V_{CC} (V)	V_I	OTHER
	typ.	max.	max.	max.				
ΔI_{CC} per input pin for a unit load coefficient of 1(1)	100	360	450	490	µA	4.5 to 5.5	V_{CC} − 2.1 V	other inputs at V_{CC} or GND I_O = 0

Note

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

4.7 Power dissipation due to slow input rise/fall times

When an output stage switches, there is a brief period when both output transistors conduct. The resulting 'through-current' is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time.

As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current.

When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at $V_I = 0.5\ V_{CC}$ for 74HC devices, and $V_I = 28\%V_{CC}$ for 74HCT devices, the maximum current being determined by the geometry of the input transistors. The through-current is proportional to V_{CC}^n where n is about 2.2. The supply current for a typical HCMOS input is shown as a function of input voltage transient in Fig.14.

When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation, see Schmitt-trigger data sheets. In the case of RC oscillators, or oscillators constructed with Schmitt triggers this contribution to the power dissipation is frequency-dependent.

4.8 Comparison with LSTTL power dissipation

The dynamic power dissipation of a HCMOS device is frequency-dependent; above 1 MHz, that of an LSTTL device is too. Below 1 MHz, the dynamic component of power dissipation of an LSTTL device is negligible compared to the static component. Figure 15 shows the average power dissipation of four HCMOS devices and their LSTTL equivalents. Because all functions in a multi-functional LSTTL device are biased when power is applied, for comparison, the dissipation of whole HCMOS devices besides individual functions are given.

In Fig.15 it can be seen that:

- for SSI gate types, the HCMOS power dissipation is less than LSTTL power dissipation below about 1 MHz
- for more complex types such as a 74HC/HCT138 3-to-8 line decoder HCMOS power dissipation is less than LSTTL power dissipation up to 10 MHz.

In typical microcomputer systems, the operating frequency or the data/address signal rates will usually vary, whereas Fig.15 is for continuous operation at a constant frequency. Average operating frequencies are usually far below the peak frequencies, particularly in the 100 kHz region where the power dissipation of HCMOS is several orders of magnitude less than that of LSTTL.

For further information, see chapter 'Power dissipation'.

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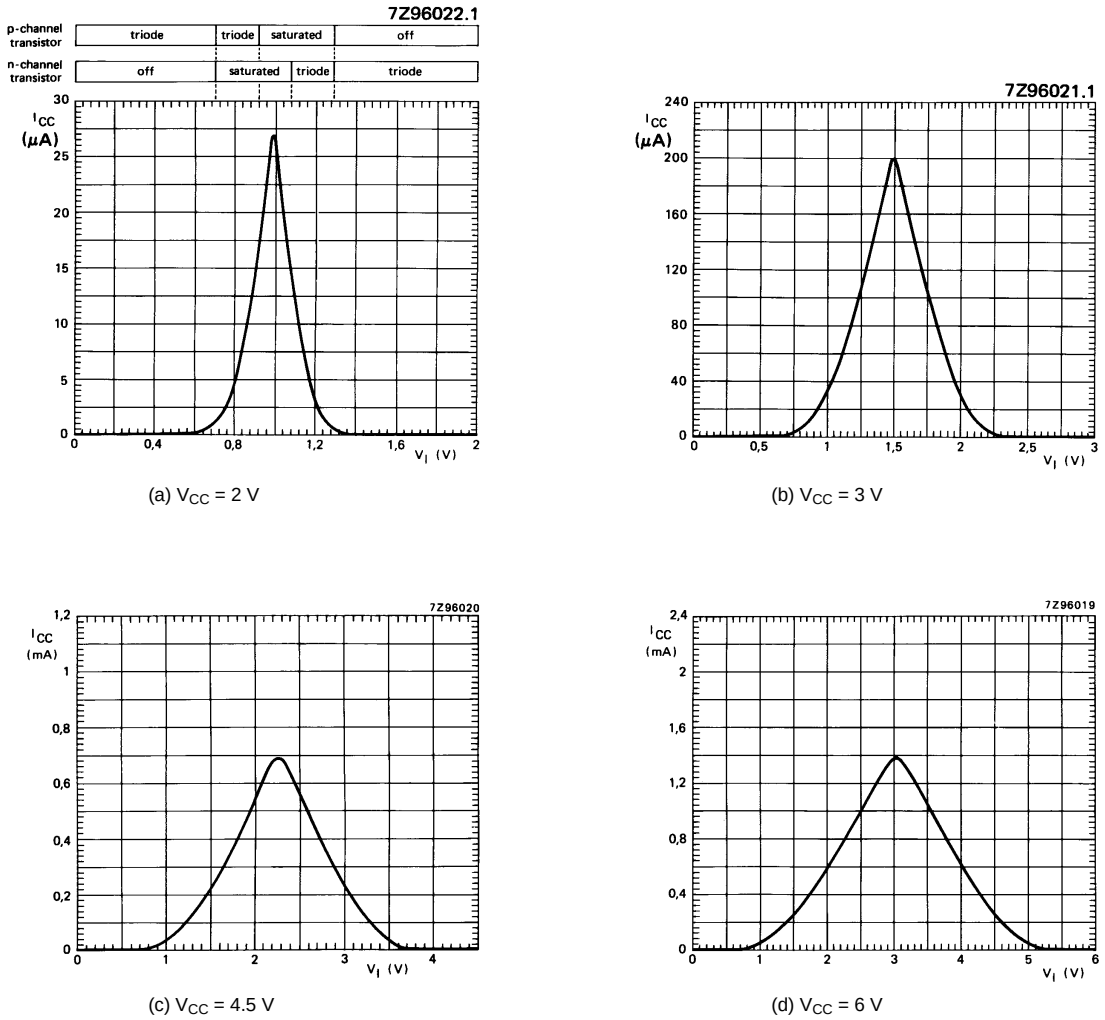


(a) V_{CC} = 2 V

(b) V_{CC} = 3 V

(c) V_{CC} = 4.5 V

(d) V_{CC} = 6 V

Fig.14 Typical DC supply current as a function of input voltage for 74HC circuits; normalized curves for a unit load coefficient of 1. The I_{CC} for a specific 74HC circuit can be calculated by multiplying the values of I_{CC} shown by the unit load coefficient for the 74HCT type given in the data sheet.

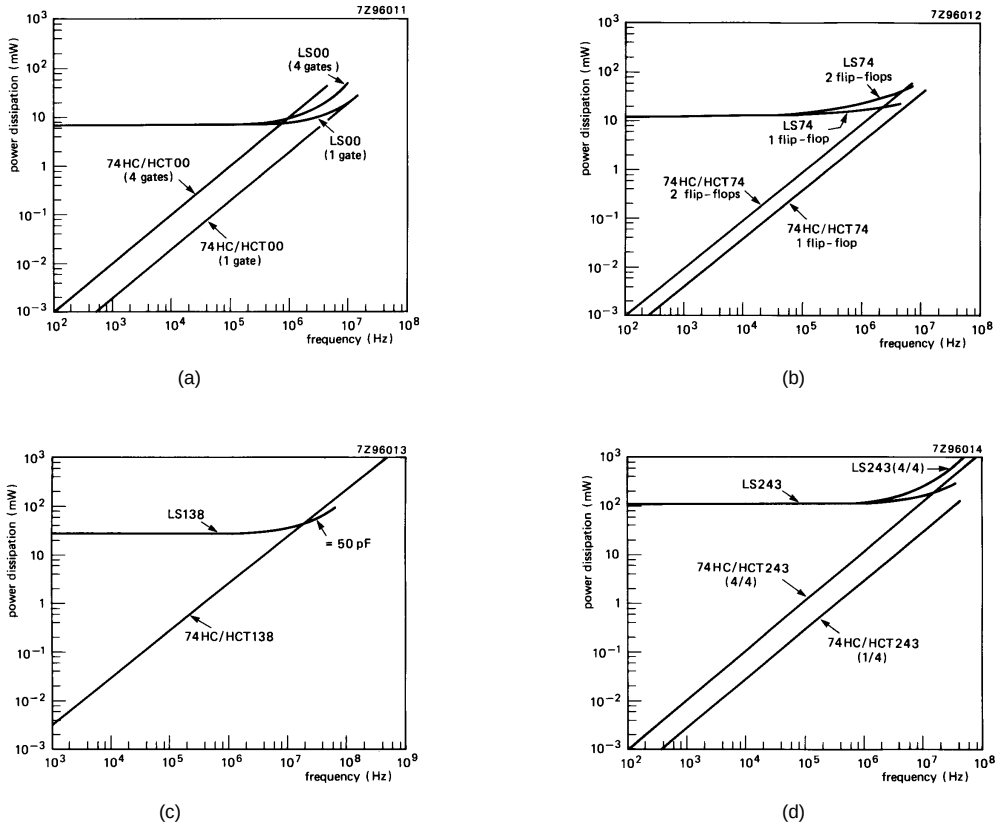


Fig.15 Typical power dissipation as a function of operating frequency for a variety of LSTTL and HCMOS circuits; (a) quad 2-input NAND gate, (b) dual D-type flip-flop, (c) 3-to-8 line decoder/demultiplexer; inverting, (d) quad 3-state bus transceiver.

5 SUPPLY VOLTAGE

5.1 Range

The supply voltage range of 74HC devices is 2 V to 6 V (Fig.16). This ensures continued use of HCMOS with future generations of memory and microcomputer requiring supply voltages of less than 5 V, simplifies the regulation requirements of power supplies, facilitates battery operation and allows lithium battery back-up. When 74HC devices are used in linear applications, for example when they are used as RC oscillators, a supply of at least 3 V is recommended to ensure sufficient margin for operation in the linear region.

74HCT devices are pin-compatible with LSTTL circuits and are intended as power-saving replacements for them. The 74HCT devices will operate from the traditional 5 V LSTTL supply, but the voltage range is extended to ±10% for both LSTTL temperature ranges (–40 to +85 °C and –40 to +125 °C). This allows extended temperature range LSTTL devices to be replaced by 74HCT devices.

The absolute maximum supply or ground current per pin is ±50 mA for devices with standard output drive, and ±70 mA for devices with bus driver outputs. These currents are only drawn when the outputs of a device are heavily loaded. The average dynamic current at very high frequencies can be calculated using C_{PD}.

The maximum rated supply voltage of HCMOS devices is 7 V and any voltage above this may destroy the device, even though the on-chip parasitic diode break-down voltage is at least 20 V and the threshold voltage of parasitic thick-field oxide transistors is 15 V.

The V_{CC} and GND potentials must never be reversed as this can cause excessive currents to flow through the input protection diodes.

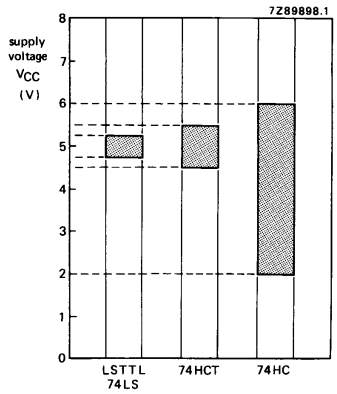


Fig.16 Supply voltage ranges for LSTTL and HCMOS circuits. The supply voltage range for 74HCT circuits retain the LSTTL nominal supply of 5 V, but the range has been extended from ±5% to ±10% for both the standard and the extended temperature range. 74HC circuits operate with a supply voltage as low as 2 V.

5.2 Battery back-up

A battery back-up for a 74HC system is extremely simple. Figure 17 shows an example. The minimum battery voltage required is only 2 V plus one diode drop.

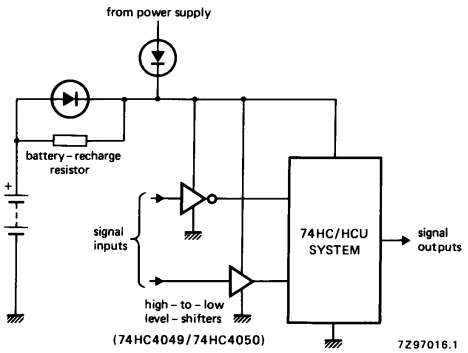


Fig.17 An HCMOS system with battery back-up.

In the example, HIGH-to-LOW level shifters (74HC4049 or 74HC4050) prevent positive input currents into the system due to input signals greater than one diode drop above V_{CC}. If the circuit is such that input voltages can exceed V_{CC}, external resistors should be included to limit the input current to 15 mA for one input (7.5 mA per input for two inputs, 5 mA per input for three inputs, etc.). External resistors may also be necessary in the output circuits to limit the current to 20 mA if the output can be pulled above V_{CC} or below GND. These current limits are set by the parasitic V_{CC}/GND diodes present in all outputs, including three-state outputs.

For further information, see chapter ‘Battery back-up’.

5.3 Power supply regulation and decoupling

The wide power supply range of 2 V to 6 V may suggest that voltage regulation is unnecessary. However, a changing supply voltage will affect system speed, noise immunity and power consumption. Noise immunity, and even the operation of the circuit, can be affected by spikes on the supply lines, so matched decoupling is always necessary in dynamic systems.

Both 74HC and 74HCT devices have the same power supply regulation and decoupling requirements. The best method of minimizing spikes on the supply lines is simple enough — use a good power supply, provide good ground bussing and low AC impedances from the V_{CC} and GND pins of each device. The minimum decoupling capacitance depends on the voltage spikes that can be tolerated, which in general should be limited to 400 mV. A local voltage regulator on a printed circuit board can be decoupled using an electrolytic capacitor of 10 to 50 μF. Localized decoupling of devices can be provided by 22 nF per every two to five packages and a 1 μF tantalum capacitor for every ten packages. The V_{CC} line of bus driver circuits and level-sensitive devices can be decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

For further information, see chapter ‘Power supply decoupling’.

6 INPUT/OUTPUT PROTECTION

The gate input of a MOS transistor acts as a capacitor (<1 pF) with very low leakage current (<1 pA). Without protection, such an input could be electrostatically charged to a high voltage that would breakdown the dielectric and permanently damage the device.

The integration process of the HCMOS family allows polysilicon resistors to be formed at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. These resistors also ensure that the input impedance of an HCMOS device is typically 100 Ω under all biasing conditions, even when

V_{CC} is short-circuited to GND — an improvement over direct input diode clamps during power-up.

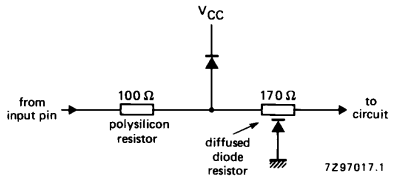


Fig.18 Standard input protection of 74HC/HCT/HCU inputs against electrostatic discharge.

The standard input protection comprises a series polysilicon resistor and two stages of diode clamping (Fig.18). The typical forward voltage of the diodes is 0.9 V at 2 mA and the reverse breakdown voltage is 20 V. In some applications such as oscillators, the diodes conduct during normal operation, in which case the input current should be limited. The maximum positive input current $+I_{IK}$ per input is 20 mA. For devices with a standard output, the total positive input current is 50 mA; for devices with a bus-driver output, the total input current is 70 mA. The maximum negative input current $-I_{IK}$ per pin is:

14 mA for one input
9 mA for two inputs
6 mA for three inputs
5 mA for four inputs
4 mA for five inputs
3 mA for six to eight inputs.

High-to-low level shifters 74HC4049 and 74HC4050 have a single-sided input protection network (Fig.19) which protects against electrostatic input voltages. The diode D1 is the parasitic drain-to-GND diode of the thick field oxide protection device.

All input pins can withstand discharge voltages up to 2.5 kV (typ.) when tested according to MIL-STD-883B, method 3015, see Fig.20. The output configurations of standard, bus driver, three-state, open drain and I/O ports can withstand >3.5 kV (typ.) because of the large diodes formed by the drain surfaces of the output transistors.

Figure 21 shows the voltage pulse for the discharge test. The rise time t_r prescribed by MIL-STD-883B is ≤15 ns, but in practice it is helpful to adjust the test set-up to give a rise time of 13 ± 2 ns to avoid correlation problems.

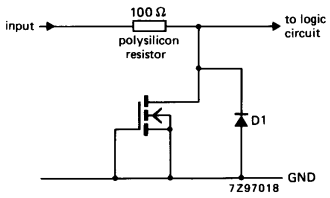
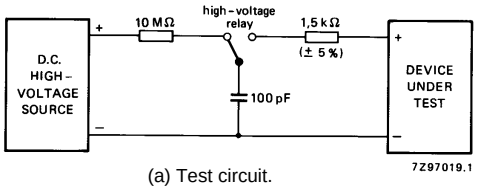


Fig.19 Input protection of 74HC4049 and 74HC4050.

Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed (see chapter ‘Handling precautions’).



(a) Test circuit.

mode	device under test	
	+	−
1	input	GND
2	GND	input
3	input	V_{CC}
4	V_{CC}	input
5	output	GND
6	GND	output
7	output	V_{CC}
8	V_{CC}	output
9	input	output
10	output	input
11	V_{CC}	GND
12	GND	V_{CC}

Note

1. all other pins should be left open circuit

(b) Test modes

Fig.20 Electrostatic discharge test.

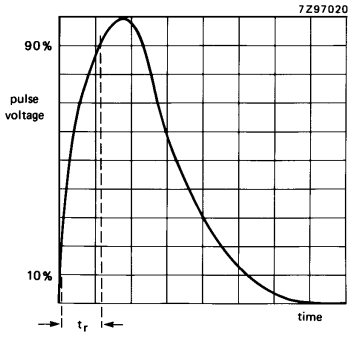


Fig.21 Test voltage for electrostatic discharge test.

7 INPUT CIRCUITS

7.1 74HC inputs

The 74HC input circuit (Fig.22) includes the resistor/diode network for electrostatic discharge protection and clamps input voltages greater than V_{CC} or less than GND. The circuit is intended for AC working and cannot handle heavy DC currents for long periods; the maximum input diode current is 20 mA.

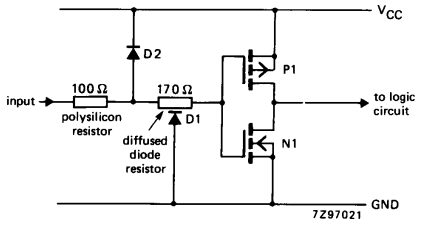


Fig.22 74HC input circuit.

The 74HC input circuit has no active input current; the only current flowing is through the reversed-biased diodes D1 and D2, typically a few nA reaching a maximum when $V_I = V_{CC}$ or GND.

The MOS transistors P1 (p-channel) and N1 (n-channel) have the same conductance when switched on, giving a typical switching threshold of 50% V_{CC}, see Fig.23. This threshold is almost independent of temperature, a ±60 mV variation of the switching point from –40 to +125 °C being typical. The temperature dependence of V_{IL} is –0.6 mV/°C, that of V_{IH} is +0.6 mV/°C. The only other factors that affect the switching threshold are the spreads of β and V_T of P1 and N1 between devices.

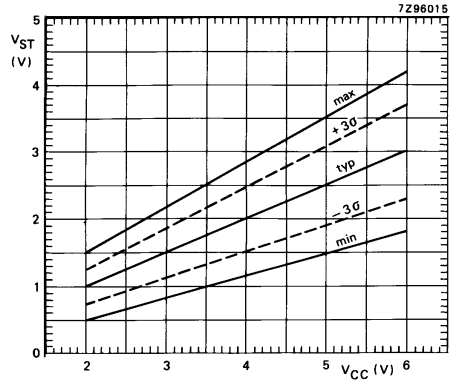


Fig.23 74HC input switching level as a function of supply voltage.

There is no current path from V_{CC} to GND when the input is lower than V_{TN}, or higher than $V_{CC}–V_{TP}$. However, when the input voltage is in the linear region, a static current path from V_{CC} or GND flows in the input stage (Fig.14). This current is negligible under normal operating conditions when the input rise time $t_r \leq 15$ ns, but the power dissipation should be taken into account for devices operating in the linear region. Owing to the voltage gain of the input stage, there is no static flow-through current in the second and subsequent stages. Small currents do flow in these stages during operation when both n-channel and p-channel transistors conduct for brief periods and their effect is included in the C_{PD} value in the data sheets.

7.2 74HCT inputs

The 74HCT input stage is similar to that of a 74HC device. It has the same characteristics for LSTTL levels as a 74HC input has for CMOS levels, so there is no trade-off in speed or power dissipation. The switching threshold is lower, 1.4 V at V_{CC} = 5 V. In addition, the 74HCT input circuit, shown in Fig.24, has an enlarged n-channel transistor (N1) and a level-shift diode (D3) has been added. The natural drain voltage of the p-channel transistor (P1) is approximately V_{CC} – 0.6 V, but when the input voltage is LOW, an auxiliary pull-up transistor (P2) raises this to V_{CC}, cutting off p-channel transistor P3 completely. The input stage is well matched to the load presented by the second stage so that symmetrical propagation delays are obtained.

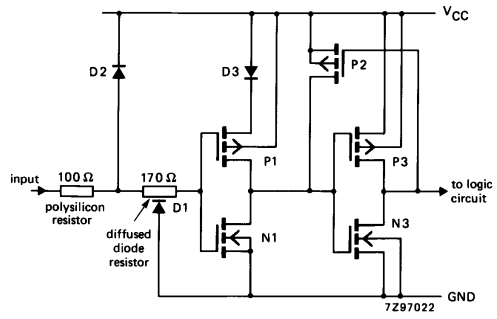


Fig.24 74HCT input circuit.

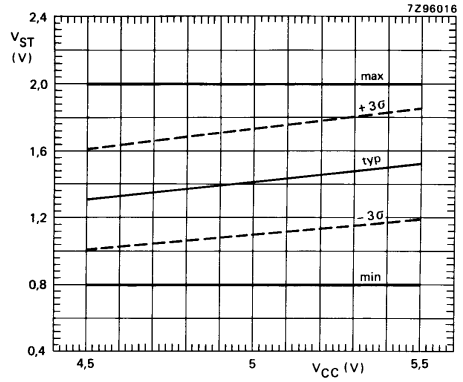


Fig.25 74HCT input switching level as a function of supply voltage.

Figure 25 shows the switching level as a function of supply voltage.

A TTL HIGH level can be as low as 2.4 V. An input of this order to a HCMOS device would not cut off P1 completely, and additional supply current would flow through the input stage. A level-shift diode D3 and the influence of the back-gate (substrate) connection to P1 minimizes power dissipation caused by this through-current and gives an input switching level compatible with LSTTL. Figure 26 shows the input stage through-current with and without the diode circuit. The peak in the curve occurs at the input switching threshold.

The input stage through-current is virtually zero for a typical TTL HIGH level input of 3.5 V. Thus, this unique 74HCT input structure gives true CMOS low power-consumption when driven by TTL. Typical and maximum through-currents ΔI_{CC} per input are given in the data sheets.

In a system where 74HCT devices are only driven by LSTTL devices, $V_{OH\,min}$ can be 2.7 V except for some bus drivers. With V_{OH} = 2.7 V, ΔI_{CC} is half the published value.

7.3 Maximum input rise/fall times

All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, Schmitt-triggers are recommended if rise/fall times are likely to exceed 500 ns at V_{CC} = 4.5 V.

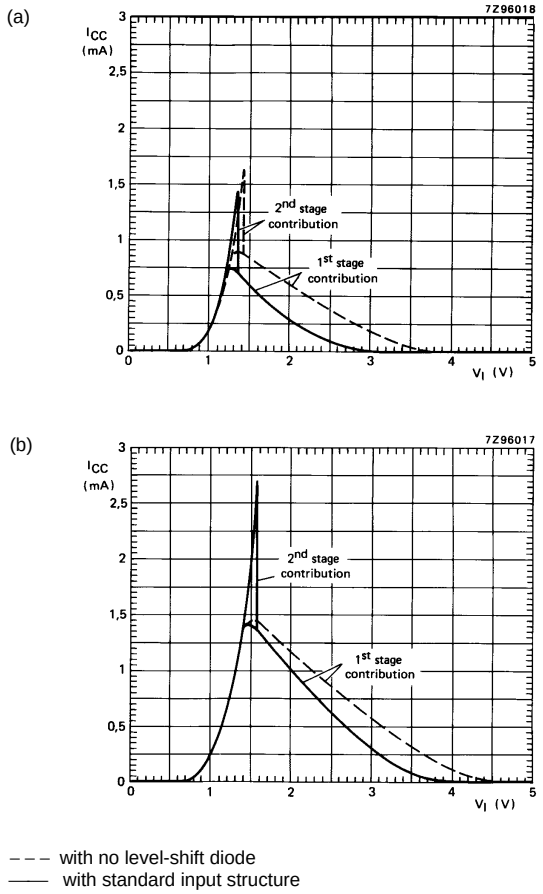


Fig.26 Additional quiescent supply current ΔI_{CC} (typ.) per input pin of a 74HCT device as a function of supply voltage (unit load coefficient is 1); (a) V_{CC} = 4.5 V, (b) V_{CC} = 5.5 V.

The flip-flops 74HC/HCT73, 74, 107, 109 and 112 incorporate Schmitt-trigger input circuits and the 74HC/HCT14 and 132 are dedicated Schmitt triggers with specified input levels.

For further information, see chapter ‘Schmitt trigger applications’.

7.4 Termination of unused inputs

To prevent any possibility of linear operation of the input circuitry of an LSTTL device, it is good practice to terminate all unused LSTTL inputs to V_{CC} via a 1.2 kΩ resistor. Inputs should not be connected directly to GND or V_{CC}, and they should not be left floating.

Unlike LSTTL inputs, the impedance of 74HC and 74HCT inputs is very high and unused inputs must be terminated to prevent the input circuitry floating into the linear mode of operation which would increase the power dissipation and could cause oscillation. Unused 74HC and 74HCT inputs should be connected to V_{CC} or GND, either directly (a distinct advantage over LSTTL), or via resistors of between 1 kΩ and 1 MΩ. Since the resistors used to terminate the inputs of LSTTL devices are usually between 220 Ω and 1.2 kΩ, it is often possible to directly replace LSTTL circuits with their 74HCT counterparts.

Some of the bidirectional (transceiver) logic devices in the HCMOS family have common I/O pins. These pins cannot be connected directly to V_{CC} or GND. Instead, when defined as inputs, they should be connected via a 10 kΩ resistor to V_{CC} or GND.

7.5 Input current

Figure 27 shows the typical input leakage current of a HCMOS device as a function of ambient temperature for a V_{CC} of 6 V. Over the total operating temperature range, the input leakage current is well below the rating specified in the JEDEC standard (100 nA between –55 °C and +25 °C and 1μA at +85 °C and +125 °C. The reason for this difference between the measured performance and the rating is the high-speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the rating is end-of-line, allowing some leakage current shift due to the ingress of moisture or foreign material.

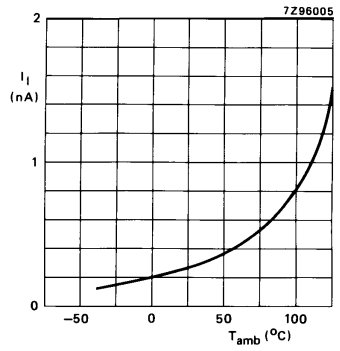


Fig.27 Typical HCMOS input leakage current I_I as a function of ambient temperature T_{amb}.

7.6 Input capacitance

Since CMOS inputs present essentially no load, fan-out is limited only by the input capacitance. This is specified as 3.5 pF (typ.) and comprises package, bonding pad/interconnecting track, input protection diode and transistor gate capacitances. Figs 28 and 29 show the typical input capacitances for powered 74HC and 74HCT devices. The initial decrease in capacitance as V_I rises from zero or falls from 5 V is due to increased reverse bias on the protection diodes. The peak is caused by internal Miller feedback capacitance when the inverter is in its linear mode. A conservative value for the maximum input capacitance is 10 pF (20 pF for I/O pins owing to the output drain capacitance). Input capacitance is measured with all other inputs tied to ground.

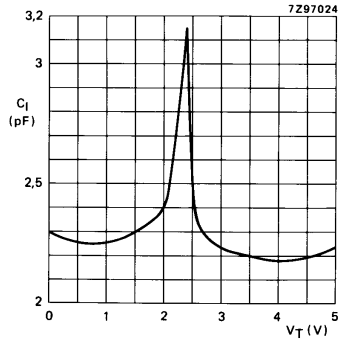


Fig.28 Typical input capacitance C_I of a 74HC device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

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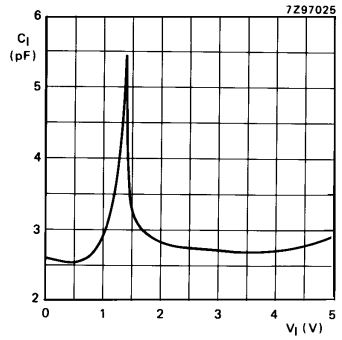

Fig.29 Typical input capacitance C_I of a 74HCT device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

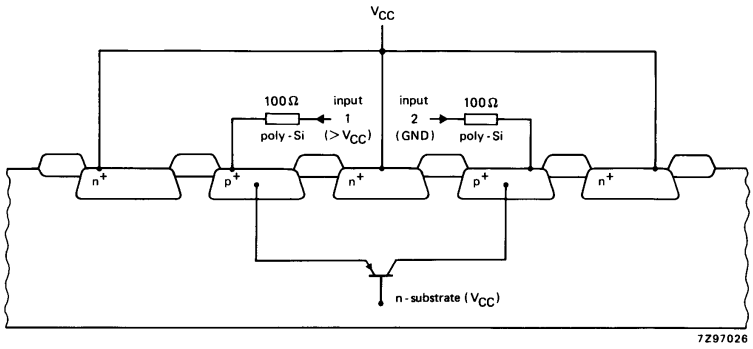

Fig.30 Cross-section of the input protection of an HCMOS device showing the parasitic pnp transistor between adjacent inputs.

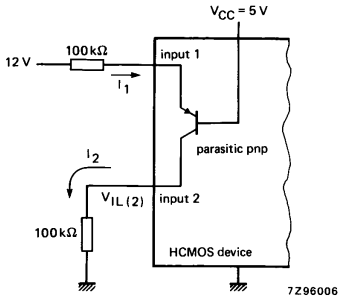

Fig.31 12 V-to-5 V logic-level conversion at HCMOS inputs using 100 kΩ series resistors.

7.7 Coupling of adjacent inputs

Parasitic bipolar pnp transistors can be present between adjacent inputs, e.g. between an input protection diode to V_{CC} and the same diode at the adjacent input, as shown in Fig.30. If the recommended operating input voltage is exceeded, perhaps by ringing of more than 0.7 V, current into the terminal (I_1) can cause a current I_2 in the parasitic transistor and in the adjacent input (Fig.31). Because I_2 in the adjacent input has to be drained by the source driving that input, the source resistance (R) must be low. If R is not low enough, the parasitic current can lift the source voltage and cause unwanted switching.

The ratio of the parasitic adjacent input current (I_2) to the forced input current (I_1) denoted α:

$$\alpha = \frac{I_2}{I_1}$$

α has been reduced to less than 0.05 (typically 0.001) in the HCMOS family by the use of deep guard rings and optimum bonding pad spacing.

A low α permits proper logic operation in the presence of transients and also allows HIGH-to-LOW voltage translation simply by adding series input resistors. For example, in Fig.31, 12 V system logic is converted to 5 V system logic by adding a 100 kΩ resistor in each input. Since the logic signals are delayed by 1-2 μs, this arrangement is suitable for rather slow 12 V control logic such as that in automotive applications. When the input diodes are used as clamps for logic level translation, the total input current should be limited to 20 mA.

7.8 Input voltage and forward diode input current

As a general rule, CMOS logic devices with input clamp diodes (Fig.18) should be operated between the power supply rails. Neglecting the input series polysilicon resistor shown in Fig.18, this means: $-0.5\ V \leq V_I \leq V_{CC} + 0.5\ V$.

This rule is JEDEC Std. No. 7A and is intended to prevent users damaging devices similar to HCMOS that do not have the polysilicon resistor. HCMOS devices however meet the tougher rating: $-1.5\ V \leq V_I \leq V_{CC} + 1.5\ V$. Furthermore, virtually all HCMOS devices can operate reliably up to the rating without logic errors.

The maximum permissible continuous current forced into an input or output of a HCMOS device is ±20 mA (JEDEC rating).

8 OUTPUT CIRCUITS

8.1 Output drive

There are three different output configurations in the HCMOS family:

- push-pull
- three-state
- open-drain n-channel transistor.

Each is available with a standard output or a bus driver output, the latter having 50% more drive capability. All 74HC and 74HCT outputs are buffered for consistent current drives and AC characteristics throughout the HCMOS family. Well-matched output n-channel and p-channel transistors give symmetrical output rise and fall times.

When comparing the output drive capabilities of HCMOS with those of LSTTL, note that LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This guarantees that a system will operate correctly with worst-case LOW and HIGH input signals and that noise immunity margins will be preserved. HCMOS capability is expressed as the source or sink current at a specified output voltage. Since HCMOS requires virtually no input current, the unit load concept is not applicable.

With a specified output drive of 4 mA (at $V_{OLmax} = 0.4$ V), the HCMOS capability exceeds 4000 ULs, and with a 20 μA (at $V_{OL} = 0.1$) specification the HCMOS capability is 20 ULs. A standard HCMOS output can drive ten LSTTL loads and maintain $V_{OL} \leq 0.4$ V over the full temperature range. A bus driver output can drive 15 LSTTL loads under the same conditions. Table 10 shows the output drive capabilities of some HCMOS devices expressed in LSTTL unit loads. The output current may be increased for higher output voltages. For example, extrapolating the 6 mA bus driver capability at $V_{OL} = 0.33$ V and $T_{amb} = 85$ °C to a V_{OL} of 0.5 V gives an output drive capability of 9 mA.

Output current derating as a function of temperature is shown in Fig.32 and is valid for all types of output. Output source and sink drives at $V_{CC} = 2$ V, 4.5 V and 6 V are given in Figs 33 to 36 which show the output current as a function of output voltage; these graphs indicate the typical output currents and the expected minimum output currents. They can serve as a design aid when calculating transmission line effects or when charging highly capacitive loads.

The expected minimum curves are not guaranteed; they are tested only at the values given in the data sheets.

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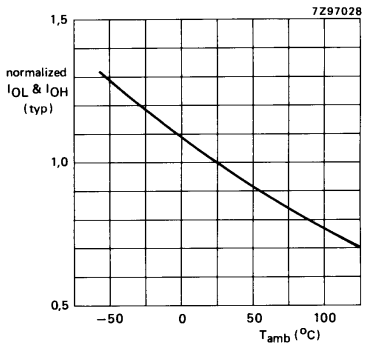

Fig.32 Derating curve for output drive currents I_{OL} and I_{OH}.

Table 10 Comparison of the output drive capabilities of LSTTL and HCMOS ($V_{OL} \leq 0.4$ V)

LS device	output	drive capacity	HCMOS equiv.	type	output	drive capacity
74LS00	4 mA	10 UL	74HC00	standard	4 mA	10 UL
74LS138	4 mA	10 UL	75HC138	standard	4 mA	10 UL
74LS245	12 mA	30 UL	74HC245	bus	6 mA	15 UL
74LS374	12 mA	30 UL	74HC374	bus	6 mA	15 UL

Note

1. UL = unit load.

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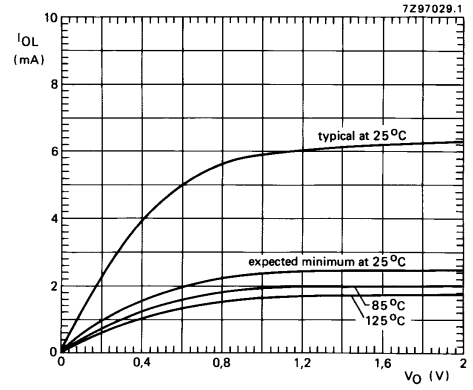
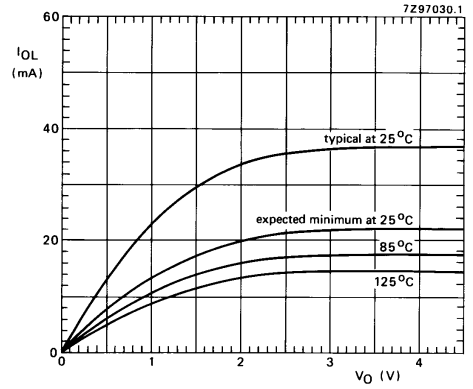
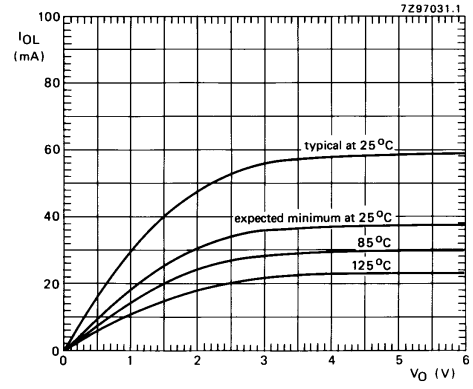


(a) V_{CC} = 2 V

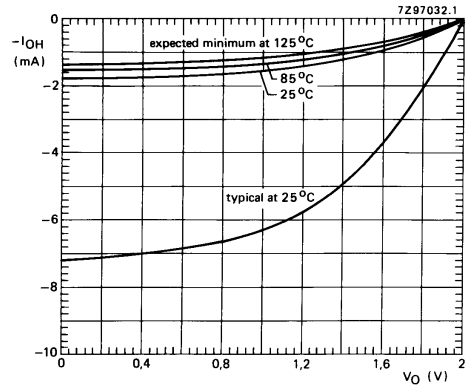


(b) V_{CC} = 4.5 V

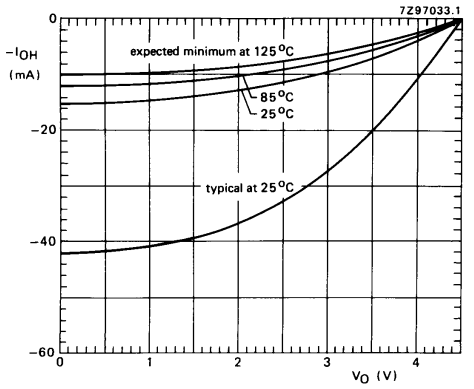


(c) V_{CC} = 6 V

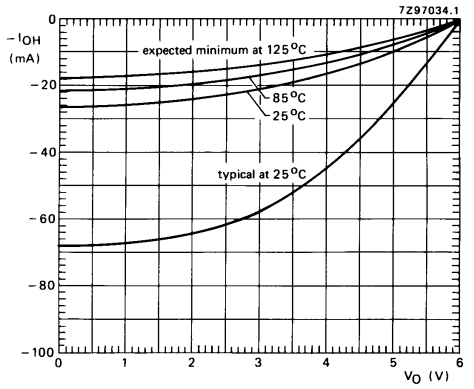
Fig.33 Standard output n-channel sink current.



(a) V_{CC} = 2 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 6 V

Fig.34 Standard output p-channel source current.

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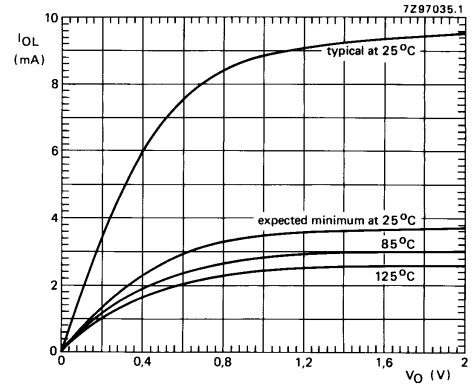
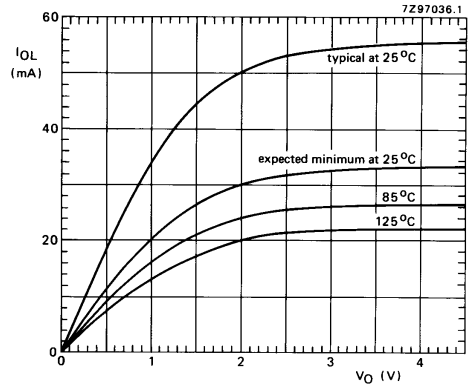
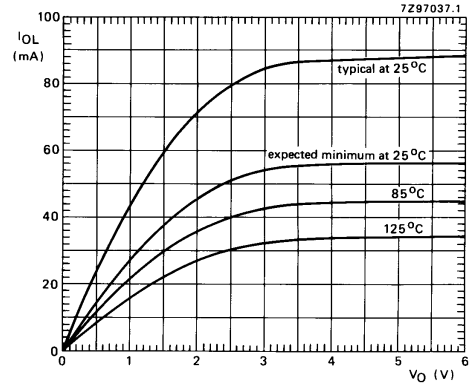


(a) V_{CC} = 2 V

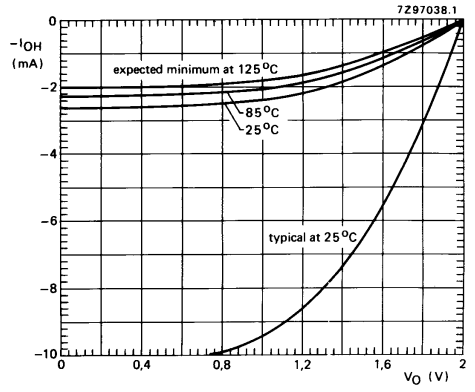


(b) V_{CC} = 4.5 V

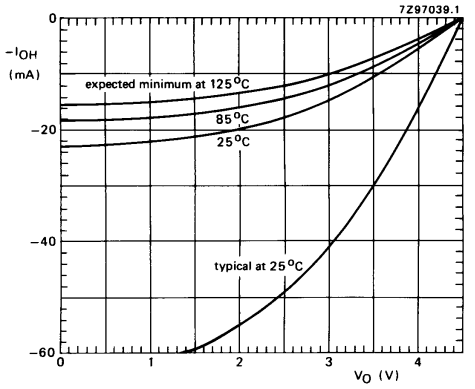


(c) V_{CC} = 6 V

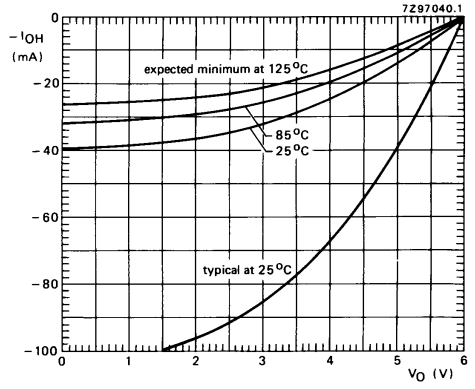
Fig.35 Bus-driver output n-channel sink current.



(a) V_{CC} = 2 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 6 V

Fig.36 Bus-driver output p-channel source current.

8.2 Push-pull outputs

A typical push-pull output stage is shown in Fig.37. The bipolar parasitic transistor-drain diodes (D1 and D2) limit the output voltage V_O of all HCMOS devices in the case of externally-forced voltages such that $-0.5\ V \leq V_O \leq V_{CC} + 0.5\ V$. For voltages outside this range, the diodes and parasitic bipolar elements start to conduct. Although the diode current rating is 20 mA DC, line ringing and power supply spikes in normal high-speed systems cause current-peaks that exceed this rating. Careful chip-layout and adequate aluminium traces ensure that the current peaks produced will not damage the diodes or degrade the internal circuitry.

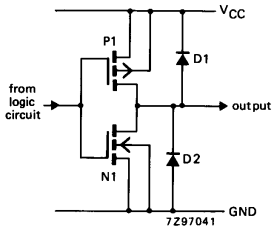


Fig.37 Basic CMOS output stage.

The maximum rated DC current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These ratings are dictated by the current capability of on-chip metal traces and long-term aluminium migration, but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

A shorted output will also cause the maximum DC current rating to be exceeded. However, one output may be shorted for up to 5 s without causing any direct damage to the IC.

The life of the IC will not be shortened if not more than **one** input or output at a time is forced to GND or V_{CC} during in-circuit logic testing (“back drive”) as long as the following rules are obeyed:

- maximum duration : 1 ms
- maximum duty factor : 10 %
- maximum V_{CC} : 6 V

Non-standard inputs or outputs may not be in-circuit tested. Examples of non-standard inputs/outputs are:

- timing pins (R_X, C_X) of monostables ‘123’, ‘221’, ‘423’ and ‘4538’
- the Y and Z pins of all compensated analog switches (‘4051’ series, ‘4351’ series, ‘4066’ and ‘4077’)
- pins for external timing components of PLLs ‘4046A’ and ‘7046A’
- the R_{TC} and C_{TC} pins of the ‘4060’.

The only exception to this rule is the non-standard output of the ‘4511’.

8.3 Three-state outputs

In the typical three-state output circuit shown in Fig.38, when EO is HIGH the output is enabled and transistors P4 and N4 act as a transmission gate connecting the gates of the output transistors. A LOW at EO puts the output in the high-impedance OFF-state and transistors P3 and N3 act as pull-up and pull-down transistors respectively. The logic symbol for a three-state output and its function table is shown in Fig.39.

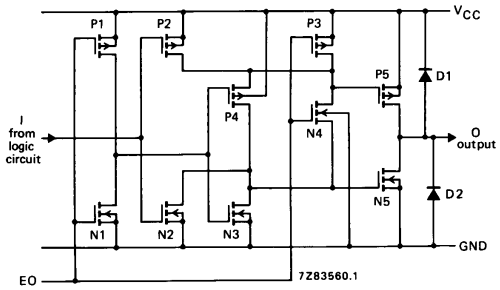
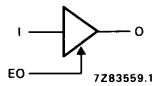


Fig.38 Typical three-state output circuit.



(a) logic symbol

inputs		outputs
I	EO	O
X	L	Z
L	H	L
H	H	H

Notes

1. H = HIGH voltage level
2. L = LOW voltage level
3. X = don't care
4. Z = high impedance OFF-state

(b) function table

Fig.39 Three-state output logic symbol and functions.

Three-state outputs are designed to be tied together but are not intended to be active simultaneously. To minimize noise and to protect outputs from excessive power dissipation, only one three-state output should be active at any time. In general, this requires that the output enable signals should not overlap. When decoders are used to enable three-state outputs, the decoder should be disabled while the address is being changed. This avoids overlapping output-enable signals caused by decoding spikes to which all decoder outputs are prone during address-changing.

When designing with three-state outputs, note that disable propagation delays are measured for an RC load when the output voltage has changed by 10% of the voltage swing. This 10% level is adequate to ensure that a device output has turned off. Although this method provides a standard reference for measuring disable times, it implies that the output is already off for 10% of the RC time. Because all disable times are measured with a load of 1 kΩ and 50 pF, subtract the 10% RC time (5 ns) from the values published in the data sheets to obtain the real internal disable propagation delay.

Diodes D1 and D2 are parasitic diodes associated with output transistors P5 and N5 respectively. Diode D1 clamps the output at one V_{BE} above V_{CC}, of importance in large systems where sections of the system may be powered-down (V_{CC} = 0 V), in which case the output diode current has to be limited to 20 mA.

All I/O ports and transceivers have a three-state output as shown in Fig.38. The I/O pin is defined as an input when the output is disabled, but this pin should be regarded as a real input and should not be left floating, because the input to an I/O port can cause V_{CC} current. If necessary, terminate the input with a 10 kΩ resistor, see 'Termination of unused inputs'.

8.4 Open-drain outputs

In TTL families, several functions are offered with open-collector outputs to enhance logic functions by using OR- tied logic. The advantage of OR-tied logic is the logic elements saved and hence the lower power dissipation. However, this is countered by power loss and reliance on RC time propagation delays. These disadvantages are not encountered in CMOS and similar applications can be made using devices with 3-state outputs, or simply with the power-saving logic devices. However, the 74HC/HCT03 (quad 2-input NAND gate) has an open-drain n-channel output, see Fig.40. The parasitic diode D1 is not present (there being no p-channel transistor); this allows the output voltage to be pulled above V_{CC} to V_{Omax} making both HIGH-to-LOW and LOW-to-HIGH level-shifting possible. For digital operation, a pull-up resistor is necessary to establish a logic HIGH level.

The open drain output is protected against electrostatic discharge.

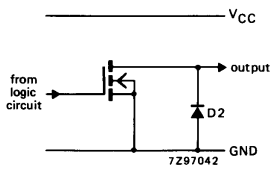


Fig.40 Open-drain output circuit.

8.5 Increased drive capability of gates

To increase output drive, the inputs and outputs of gates in the same package may be connected in parallel. It is advisable to restrict parallel connection to gates within one

package to avoid large transient supply currents due to different gate-switching times.

For further information, see chapter ‘Interfacing and protection of circuit board inputs’.

8.6 Output capacitance

For push-pull outputs, no output capacitance is specified because either the n-channel transistor or the p-channel transistor creates a low-impedance path to the supply rails.

Three-state outputs can be switched to the high impedance OFF-state, and because many of them can be connected to a bus line, the output capacitance is needed to calculate the total capacitive load. For bus-driven 3-state outputs in a DIL package, the output capacitance is 6 pF (typ.) and 20 pF (max.).

9 STATIC NOISE IMMUNITY

The static noise immunity can be divided into:

- the static noise margin LOW. This is the voltage difference between V_{ILmax} of the driven device and V_{OLmax} of the driver.
- the static noise margin HIGH. This is the difference between V_{OHmin} of the driver and V_{IHmin} of the driven device.

For 74HC devices, both the LOW level noise-margin and the HIGH-level noise margin is 28% of V_{CC}. This is a considerable improvement over LSTTL where the LOW-level noise margin is only 8% of V_{CC} and the HIGH level noise margin is just 14% of V_{CC}. The margins are even greater for HCMOS at higher supply voltages as shown in Fig.41. As 74HCT devices have the same switching levels as LSTTL, their noise margins are also the same.

The superior noise immunity of the 74HC input can be clearly seen from the voltage levels of the input-to-output transfer characteristics shown in Figs 42 and 43.

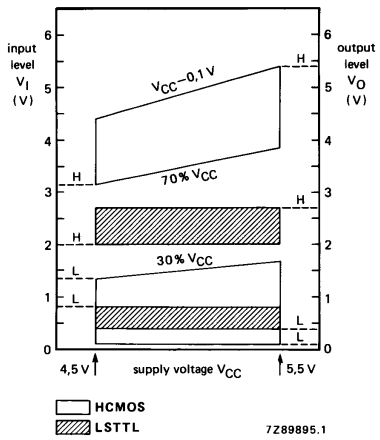


Fig.41 Worst-case input and output voltages over an operating supply range of 4.5 V to 5.5 V.

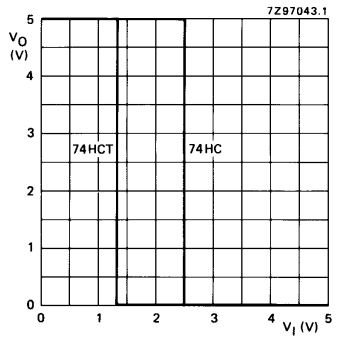


Fig.42 Typical input-to-output transfer characteristic for 74HC and 74HCT devices.

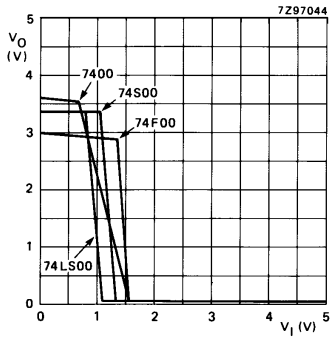


Fig.43 Input-to-output transfer characteristics for TTL devices.

Table 11 shows the input noise margin of HCMOS devices where like devices are interfaced. Output voltages are also given.

Table 11 Noise immunity and noise margin for HCMOS devices (V_{CC} = 4.5 V)

		74HC	74HCT	74HCU
$V_{IL\ max}$	(V)	1.35	0.8	0.9
V_{IHmin}	(V)	3.15	2	3.6
V_{OLmax}	(V)	0.1	0.1	0.5
V_{OHmin}	(V)	4.4	4.4	4
Noise margin low				
V_{NML}	(V)	1.25	0.7	0.4
Noise margin high				
V_{NMH}	(V)	1.25	2.4	0.4

Table 12 shows the input noise margin of 74HCT devices interfacing with LSTTL devices; the 74HCT or LSTTL output is fully-loaded, V_{CC} = 4.5 V and T_{amb} is 0 °C to +70 °C (the only convenient temperature range when using LSTTL characteristics).

Table 12 Noise immunity and noise margin for 74HCT and LSTTL device interfacing

		74HCT	LSTTL
$V_{IL\ max}$	(V)	0.8	0.8
V_{IHmin}	(V)	2	2
V_{OLmax}	(V)	0.33 (note 1) 0.1 (note 2)	0.4
V_{OHmin}	(V)	3.84 (note 1) 4.4 (note 2)	2.7
Noise margins (V):			
from 74HCT to LS		V_{NML} V_{NMH}	0.47 1.84
from LS to 74HCT		V_{NML} V_{NMH}	0.4 0.7
from LS to LS		V_{NML} V_{NMH}	0.4 0.7
from 74HCT to 74HCT		V_{NML} V_{NMH}	0.7 2.4

Notes

1. 4 mA load (i.e. 10 LSTTL inputs).
2. 20 μA load (i.e. 20 74HCT inputs).

Whenever a 74HCT output drives either an LSTTL or a 74HCT input, the noise margin is better than when an LSTTL device drives an LSTTL or 74HCT input. This improvement is larger for V_{NMH} owing to the superior output sourcing current of the rail-to-rail HCMOS output swing compared with the limited totem-pole pull-up output voltage of LSTTL.

10 DYNAMIC NOISE IMMUNITY

As for static noise immunity, dynamic noise immunity can be divided into two parts:

- a dynamic noise margin LOW
- a dynamic noise margin HIGH.

For 74HC devices, both margins are similar; for 74HCT devices, the dynamic noise margin LOW is the smaller of the two. To plot it, a pulse of known magnitude, V_p, is applied to the input of a device and its width, t_W, is increased until the device just begins to switch. The input level on which V_p is based is equal to the switching voltage minus the worst-case static noise margin LOW. The pulse width is measured at half pulse height, $V_p/2$. The rise and fall times, t_r and t_f are 0.6 ns.

V_p is then reduced in increments and t_W for each new value is ascertained.

The test is repeated for different supply voltages — for 74HC devices between 2 V and 6 V, and at 5 V for 74HCT devices. A range of output currents, I_O, are also used. Increasing the DC load reduces the dynamic noise immunity.

Figure 44 shows the amplitude of positive-going pulses that can be withstood in the LOW state for 74HC and 74HCT devices. The curves are worst-case ones with fully-loaded drivers, so a system using only 74HC or 74HCT devices will have 0.23 V more noise margin for all t_W.

For typical input switching thresholds of 1.4 V and 2.25 V for 74HCT (V_{CC} = 5 V) and 74HC (V_{CC} = 4.5 V) respectively, the noise margins will be 0.83 V [(1.4 − 0.8) + 0.23 V] larger for 74HCT and 1.13 V [(2.25 − 1.35) + 0.23 V] larger for 74HC devices.

The main causes of unwanted input pulses are spikes due to outputs switching, which dumps large currents on the GND lines, or reflections when long lines (longer than about 32 cm) are driven. For more information on the latter, see chapter ‘Replacing LSTTL and driving transmission lines’.

The best example of an unwanted pulse generator is an octal device with bus outputs of which seven are switching simultaneously and the eighth, most remote, output is LOW. Figure 45(a) shows the maximum pulse voltage measured on the unswitched output of a 74HC/HCT374 as a function of V_{CC}. Figures 45(b) and 45(c) show this maximum voltage and the pulse width as functions of the number of outputs that are switching. It should be emphasised that any pulses produced by switching outputs won’t cause other devices to respond even in worst-case conditions. This is because Fig.44 is based on a worst-case V_{OL} and the maximum expected pulse height of Fig.45 occurs for a best-case V_{OL}. So, even when a pulse of the maximum expected height shown in Fig.45 occurs, there is still a noise margin. This can be verified by plotting the pulse heights of Fig.45 on the curves of Figs 44(a) and 44(b).

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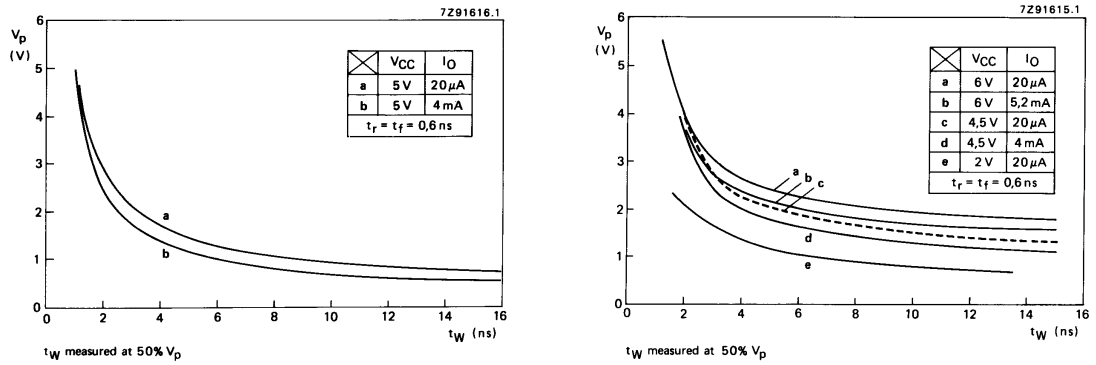

(a) (b)

Fig.44 Amplitude of the positive-going pulses that can be withstood in the LOW state (worst-case, fully-loaded driver) for (a) 74HCT devices and (b) 74HC devices.

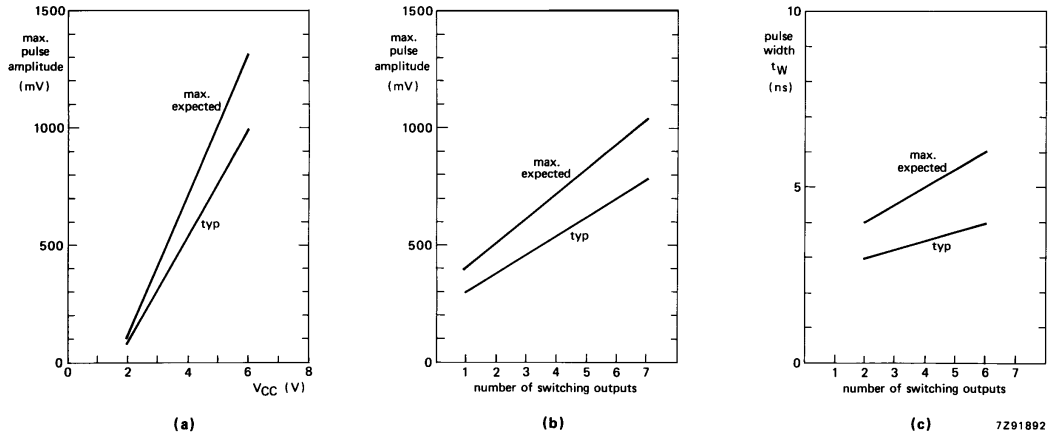

Fig.45 (a) Amplitude of the voltage pulse (on pin 2, the most remove) due to switching seven of the bus-driver outputs of a 74HC/HCT374 octal flip-flop; C_L = 150 pF, T_{amb} = 25 °C. (b) Amplitude of the voltage pulse (on pin 2) as a function of the number of outputs switched; V_{CC} = 5 V, C_L = 150 pF. (c) Pulse width as a function of the number of outputs switched; V_{CC} = 4.5 to 6 V, C_L = 150 pF. For V_{CC} = 2 V, the maximum expected pulse width is about 10 ns.

11 BUFFERED DEVICES

11.1 Definition

Often the terms ‘buffer devices’, ‘buffered inputs’ or ‘buffered outputs’ are used without qualification and originate from the very first unbuffered CMOS logic family consisting of one-stage logic elements, usually gates. In these devices, both input switching levels and output impedances were not constant, so neither were output rise/fall times or propagation delay times. The Jedec JC40.2 committee define a buffered device to be at least two active stages with the output independent of the input logic voltage level and independent of the number of inputs that are HIGH or LOW.

A buffer meeting this definition is the AND-function circuit of Fig.46. The gain between input and output is high enough to consider the output impedance to be independent of the logic level at the input, and the output impedance is not affected by the state of the logic inputs.

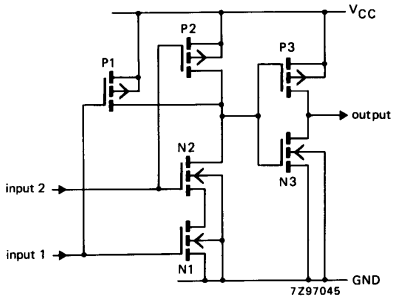

Fig.46 The minimum number of stages for a buffered device is two. This 2-stage example is an AND function.

All 74HC and 74HCT devices comprise at least two stages to minimize any pattern sensitivity of propagation delay time. Buffering also improves static noise immunity due to increased voltage gain, giving almost ideal transfer characteristics.

The designation 74HCU is used to denote single-stage devices. These have the same specification as 74HC devices but their input and output voltage parameters are relaxed. 74HCU devices don’t have the high gain of 74HC/HCT versions, which makes them more suitable for use in RC or crystal oscillators and other feedback circuits operating in the linear mode.

11.2 Output buffering

All 74HC and 74HCT devices have buffered outputs for optimum performance. To demonstrate the benefits of output buffering, consider what would happen without it. In the single-stage device shown in Fig.47, the output impedance depends on the DC input voltage. Consequently, the noise margins at the output become a function of the input voltage, even when V_I is a legal HIGH or LOW level.

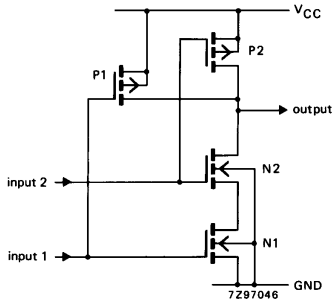

Fig.47 Unbuffered NAND gate.

The steady-state impedance of the circuit of Fig.47 is also affected by the state of the inputs. Given that P1 and P2 have identical performances (same size), there are two values of impedance for output HIGH; one when either input is LOW and P1 or P2 conducts, and another when both inputs are LOW and both P1 and P2 conduct. Therefore, without output buffering, the state of output conduction depends on the number of inputs that are HIGH or LOW.

11.3 Input buffering

An input is considered to be buffered when its switching threshold is unaffected by the logic states of other inputs. In the example of Fig.47 that has unbuffered inputs, the switching threshold of input 1 varies with a HIGH level at input 2, and vice versa. This is because the series impedance of transistors N1 and N2 determines the switching threshold of the device. The result can be seen in Fig.48 where curve $1 + 2$ occurs when the two inputs are tied together, and curve 1 or 2 is the switching threshold when the accompanying input is at V_{CC}.

For true input buffering, an input must have an inverter stage with sufficient gain to ensure that logic levels give independent on-chip levels. Some gates in the 74HC series (usually AND or OR gates) have unbuffered inputs,

however all devices meet the family logic level requirements. All 74HCT devices have buffered inputs.

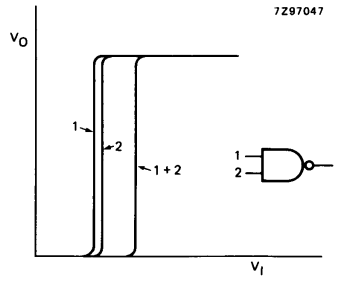

Fig.48 Example of different switching levels in unbuffered inputs.

12 PERFORMANCE OF OSCILLATORS

When HCMOS devices are used in RC, crystal or Schmitt trigger oscillators or in analog amplifiers:

- a supply voltage of at least 3 V is required. Below this value, the transconductance of crystal oscillators is too low to start oscillations. In analog circuits, insufficient output current is available to drive external components;
- slow input rise and fall times cause the input stage of a HCMOS device to draw current. This additional quiescent supply current ΔI_{CC} is given in the data sheets for 74HCT devices since these can be used as LSTTL replacements and may be driving a significant load. The total I_{CC} for 74HC devices can be calculated by multiplying the value of I_{CC} read from Fig.14 by the unit load coefficient given in the data sheet for the 74HCT device;
- in general, frequency stability won't be affected by supply voltage, so long as the permissible output currents of the devices are not exceeded.

For further information, see chapters 'Crystal oscillators' and 'Astable multivibrators'.

13 LATCH-UP FREE

Latch-up is the creation of a low-impedance path between the power supply rails caused by the triggering of parasitic bipolar structures (SCRs) by input, output or supply over-voltages. These overvoltages induce currents that can exceed maximum device ratings. When the low-impedance path remains after removal of the triggering voltage, the device is said to have latch-up.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to the maximum rating (±20 mA), and that V_{CC} should also be not more than twice V_{CCmax} (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC. In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5 s on, 15 s off) of 100 mA to 120 mA, or 1μs pulses of 300 mA with a duty factor of 0.001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5 s on, 15 s off) of 200 mA to 300 mA, or 1 μs pulses of 400 mA with a duty factor of 0.001. However, because there is an internal polysilicon 100 Ω resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high ($V_I = V_{CC} + 0.7\ V + 100I_I$) that it is unlikely that they could occur in practice, even in a 6 V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires breakdown. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

For further information, see chapter 'Standardizing latch-up immunity tests' in the Designers Guide, High-speed CMOS.

14 DROP-IN REPLACEMENTS FOR LSTTL

74HCT devices are power-saving, drop-in replacements for LSTTL devices. Because most systems are operated at frequencies far below the maximum possible, 74HCT devices can also be used to good effect in systems using ALS, AS, S, and FAST devices.

Fan-out should be considered when replacing a TTL device by a 74HCT device. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). Table 13 shows the fan-out of 74HCT to the different TTL families.

The fan-outs given in Table 13 are derived at a voltage drop of max. 0.4 V (V_{OL}). In the "74" TTL series, an extended V_{OL} figure is often seen, e.g. 8 mA at 0.5 V voltage drop for LSTTL. If this figure is used to determine the fan-out of the TTL device it can result in a higher fan-out than is possible with 74HCT. This can be resolved by replacing as many of the driven TTL parts as possible by 74HCT devices to reduce the sink current requirement

(the 74HCT input current is negligible). In addition, power dissipation is reduced significantly by using 74HCT.

Table 13 Fan-out of 74HCT to TTL circuits

74HCT	TTL	LS	ALS	FAST	S & AS
standard output	2	10	20	6	2
bus-driver output	3	15	30	10	3

15 BUS SYSTEMS

CMOS is being used to an increasing extent in microprocessor bus systems following the introduction of versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically-noisy environments, battery-standby requirements and sealed, gas-tight enclosures. HCMOS bus systems, e.g. the CMOS STD bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

For optimum results, use only 74HC devices in circuits which communicate directly with the bus. This allows a new bus termination to be introduced (see Fig.49(b)) which, unlike the conventional TTL bus termination, draws no heavy DC current and is more suited to HCMOS outputs.

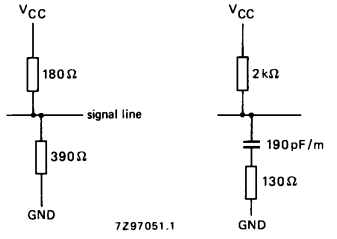

Fig.49 Bus terminations. (a) Conventional termination for TTL buses. (b) Proposed termination for CMOS STD bus equivalents.

The wider supply voltage range of HCMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes of differential voltages via an edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a 10 kΩ series resistor in the HCMOS logic line. This will limit current to ±20 mA for external voltages of up to ±200 V, however, for correct functioning, the DC input current should be kept below those values stated in ‘Input/output protection’. The recommended board edge input protection is shown in Fig.50.

In the circuit of Fig.50, if the input diode current exceeds the maximum input current, a HIGH-to-LOW level shifter should be used (e.g. 74HC4049 or 74HC4050).

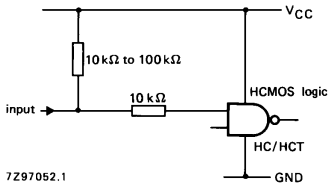

Fig.50 Example of the board edge input protection circuit.

For further information, see chapter ‘Interfacing and protection of circuit board inputs’.

Since HCMOS bus-drivers do not have built-in hysteresis, slowly-rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the flip-flop series 74HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt triggers 74HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section ‘Propagation delays and transition times’ of this User Guide.

16 PACKAGE PIN CAPACITANCE

In purely digital circuits, the input capacitance or three-state output capacitance is sufficient to determine the dynamic characteristics. However, when a HCMOS device is used in the linear region, it is necessary to take pin capacitance into account, e.g. to prevent crosstalk in analog switches or peaks in the frequency response of PLLs.

The use of SO packages with their low pin capacitances is recommended for HCMOS analog designs. Table 14 gives the pin-to-pin capacitances for the plastic DIL and SO packages used for HCMOS. Measurements were made using a dummy package with all unused pins connected to ground.

Table 14 Typical pin capacitances (pF) of SO and DIL packages

	SO-14 & SO-16	DIL-16	SO-20	DIL-20	SO-24	DIL-24
capacitance to ground of:						
corner pins	0.41	0.97				
all other pins	0.21	0.37				
any end two pins			0.65	1.12		
all other pins			0.25	0.40		
any end three pins					0.65	1.64
all other pins					0.33	0.65
capacitance between adjacent pins:						
including a corner pin	0.15	0.40				
all other pins	0.04	0.13				
any end three pins			0.28	0.49		
all other pins			0.14	0.22		
any end three pins					0.30	0.70
all other pins					0.12	0.28

17 POWER-ON RESET

The power-on reset (POR) circuit used to automatically set HCMOS ICs in a defined reset state after power-up is shown in Fig.51.

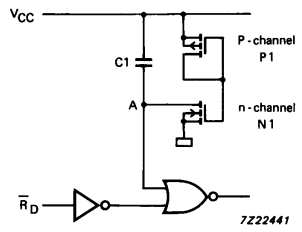

Fig.51 Power-on reset circuit.

When the IC is powered-up, node A follows the rise of V_{CC} through C1 and the circuit is reset. When the gate voltage of transistor N1 exceeds its threshold level (typically 0.7 V) because it is biased with V_{CC} via transistor P1, capacitor C1 discharges and pulls node A below the switching level of the NOR gate. The IC cannot be used during the POR release time which is the discharge time of C1 (typically 3 µs at V_{CC} = 4.5 V and 35 µs at V_{CC} = 2 V). The sensitivity of the POR circuit to supply voltage reduction is indicated in Table 15. The typical values of parameters t_W and V_L used in Table 15 are illustrated in Fig.52.

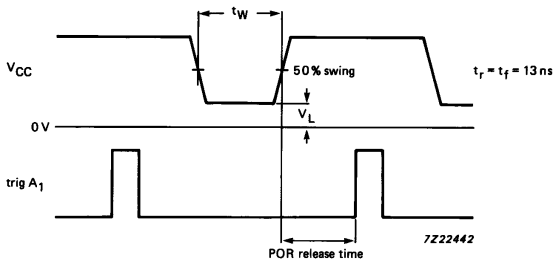

Fig.52 V_L as a function of the duration of a LOW pulse on the supply voltage.

Table 15 Sensitivity of HCMOS POR circuitry to V_{CC} reduction

	V_{CC} (V)		
t_W (µs)	2	4.5	6
	V_{Lmax} (V)	V_{Lmax} (V)	V_{Lmax} (V)
8	0.8	2.2	2.8
6	0.75	2.2	2.8
4	0.7	2.2	2.8
2	0.6	2.1	2.8
1	0.5	2.0	2.8
0.5	0.4	1.9	2.8
0.1	0.4	1.9	2.8
0.05	0.4	–	–
0.02	0.3	–	–
0.015	0.15	1.7	2.5

The time taken for a transition to propagate from $\overline{R}$ to Q is about the time taken for the reset action to take effect. Also of course, node A in Fig.51 must rise to a level above the switching level of the NOR gate. Because of this, the Q output of the IC may initially follow the V_{CC} ramp as indicated in Fig.53. If the V_{CC} ramp is fast (typically less than 100 ns), the amplitude of the Q output pulse can exceed $V_{CC}/2$ and have a duration of about 10 ns.

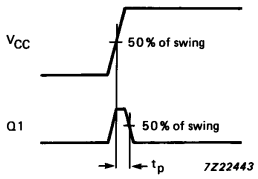

Fig.53 Initial output pulse during power-up.

Normally, the Q output pulse is negligible because the V_{CC} ramp is slow (typically more than 0.5 µs) due to the charging time of large-value smoothing and decoupling capacitors. With a slow V_{CC} ramp, the amplitude of the Q output pulse remains well below the switching level of the succeeding stage. In any event, it is most unlikely that a system will be triggered by the Q output pulse because it only occurs during power-up.