SAR (shift arithmetically right) SHR Value,#Bits 4 clks

Result: Value is shifted arithmetically right by Bits

- **Value (d-field) is the register to SAR**
- **Bits (s-field) is a register or a 5bit lateral whose value is the number of bits to SAR.**

Assume we have a value to start in a register called adc1
adc1=%01000000_00000000_00000000_00000000

SAR adc1,#10 (note the MSB is 0)
Result > adc1=%00000000_00010000_00000000_00000000
C flag=0 and the Z flag=0

Now we try the next one.(note the MSB is now 1)
adc1=%10000001_00000000_00000000_00000000

SAR adc1,#8
Result > adc1=%11111111_10000001_00000000_00000000
C flag=0 and the Z flag=0

One more to see the C flag being set.

adc1=%10000001_00000000_00000000_00000001

SAR adc1,#3
Result > adc1=%11110000_00100000_00000000_00000000
C flag=1 and the Z flag=0

Z flag set when resulting value =0	**IF WZ specified**
C flag set to original value of bit0	**IF WC specified**
The result is not written to Value if NR is specified.	

The MSB is extended along the way.
(preserves the sign in a signed value)

RTN

ROL (Rotate value left by no of Bits) ROL Value,(#)Bits 4 clks

Result: Value is rotated left by Bits

- **Value (d-field) is the register to ROL**
- **Bits (s-field) is a register or a 5bit lateral whose value is the number of bits to ROL**

Assume we have a value to start in a register called adc1
adc1=%11111111_00000000_00000000_00000000

We execute the following instruction

ROL adc1,#8
Result > adc1=%00000000_00000000_00000000_11111111
C flag=1 and the Z flag=0

Now we try the next one.
adc1=%00000000_00000000_10100000_00001010

ROL adc1,#8
Result > adc1=%00000000_1010000_00001010_00000000
C flag=0 and the Z flag=0

Z flag set when resulting value =0	**IF WZ specified**
C flag set to original value of bit31	**IF WC specified**
The result is not written to Value if NR is specified.	

(ROL and ROR are also referred to as Barrel Shifter instructions)

RTN

ROR (Rotate value right by no of Bits) ROR Value,(#)Bits 4 clks

Result: Value is rotated right by Bits

- **Value (d-field) is the register to ROR**
- **Bits (s-field) is a register or a 5bit lateral whose value is the number of bits to ROR**

Assume we have a value to start in a register called adc1
adc1=%11111111_00000000_00000000_00000000

We execute the following instruction

ROR adc1,#8
Result > adc1=%00000000_11111111_00000000_00000000
C flag=0 and the Z flag=0

Now we try the next one.
adc1=%00000000_00000000_00000000_00001010

ROR adc1,#8
Result > adc1=%00001010_00000000_00000000_00000000
C flag=0 and the Z flag=0

One more
adc1=%00000000_00000000_00000000_00001001
ROR adc1,#4
Result > adc1=%10010000_00000000_00000000
C flag=1 and the Z flag=0

Z flag set when resulting value =0	**IF WZ specified**
C flag set to original value of bit0	**IF WC specified**
The result is not written to Value if NR is specified.	

(ROL and ROR are also referred to as Barrel Shifter instructions)

RTN