

3 Section III – Quick Reference

3.1 SX Pin Assignments

RA2	1	18	RA1
RA3	2	17	RA0
RTCC	3	16	OSC1
/MCL	4	15	OSC2
V _{SS}	5	14	V _{DD}
RB0	6	13	RB7
RB1	7	12	RB6
RB2	8	11	RB5
RB3	9	10	RB4

SX 18
DIP/SOIC Package

RA2	1	11	RA1
RA3	2	12	RA0
RTCC	3	13	OSC1
/MCL	4	14	OSC2
V _{SS}	5	15	V _{DD}
V _{SS}	6	16	V _{DD}
RB0	7	17	RB7
RB1	8	18	RB6
RB2	9	19	RB5
RB3	10	20	RB4

SX 20
SSOP Package

RTCC	1	28	/MCL
V _{DD}	2	27	OSC1
	3	26	OSC2
V _{SS}	4	25	RC7
	5	24	RC6
RA0	6	23	RC5
RA1	7	22	RC4
RA2	8	21	RC3
RA3	9	20	RC2
RB0	10	19	RC1
RB1	11	18	RC0
RB2	12	17	RB7
RB3	13	16	RB6
RB4	14	15	RB5

SX 28
DIP/SOIC Package

V _{SS}	1	28	/MCL
RTCC	2	27	OSC1
V _{DD}	3	26	OSC2
V _{DD}	4	25	RC7
RA0	5	24	RC6
RA1	6	23	RC5
RA2	7	22	RC4
RA3	8	21	RC3
RB0	9	20	RC2
RB1	10	19	RC1
RB2	11	18	RC0
RB3	12	17	RB7
RB4	13	16	RB6
V _{SS}	14	15	RB5

SX 28
SSOP Package