LEVERAGING FPGA AND CPLD DIGITAL LOGIC TO IMPLEMENT ANALOG TO DIGITAL CONVERTERS

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Introduction

Designers of digital systems are familiar with implementing the “leftovers” of their digital design by using FPGAs and CPLDs to glue together various processors, memories, and standard function components on their printed circuit board. In addition to these digital functions, FPGAs and CPLDs can also implement common analog functions using an LVDS input, a simple Resistor Capacitor (RC) circuit and some FPGA or CPLD digital logic elements to create an Analog to Digital Converter (ADC).

The ADC is a common analog building block and almost always is needed when interfacing digital logic, like that in an FPGA or CPLD, to the “real world” of analog sensors. This white paper will explain the implementation of both a low frequency (DC to 1K Hz) and higher frequency (up to 50K Hz) ADC using reference designs and demo boards available from Lattice Semiconductor. A sample application for each design: one for a system monitor in a network switch, and another for frequency detection in an audio communication system, will be examined.

Analog to Digital Converter Implementation Overview

A simple Analog to Digital Converter can be constructed by adding a small RC circuit to an LVDS input on an FPGA or CPLD. As illustrated in the bottom left of Figure 1, the RC network is placed on one side of the LVDS input and the Analog Input of interest is placed on the other side. The LVDS input will act as a simple analog comparator and will output a digital ‘1’ if the Analog Input voltage is higher than the voltage from the RC network. By changing the voltage on the input to the RC circuit (from the generic output of the FPGA/CPLD), the LVDS comparator can be used to analyze the Analog Input voltage to create an accurate digital representation. The Analog to Digital Control module can be implemented in a variety of ways, depending on the frequency of the Analog Input, the desired resolution and the logic resources available. A low frequency signal can be processed using a simple Successive Approximation Register, as shown in Option 1 at the top left of Figure 1. A higher frequency implementation, shown on the

top right of Figure 1, can be implemented using a Delta Sigma Modulator function, which consists of a sampling register and a Cascade Integrated Comb (CIC) Filter.

Once the digital signal has been constructed, the Digital Output can be optionally filtered to remove any unwanted high frequency components introduced by system noise or feedback jitter (explained in more detail below). After the optional digital filter block, an optional memory buffer can be used for debug/testing purposes. The digital output can be sampled by the memory buffer and then scanned out via a JTAG port into a personal computer running signal analysis software.

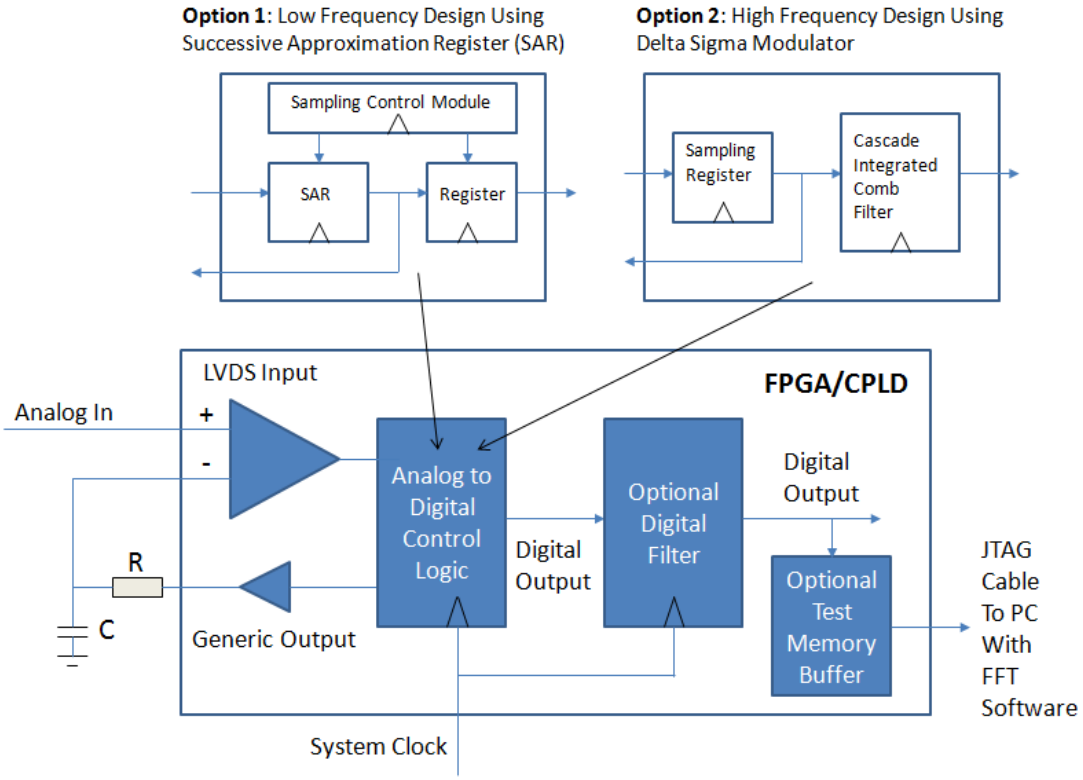

Figure1 - Analog to Digital Converter Basic Block Diagram: Low Frequency and High Frequency Options

Low Frequency/Minimal Logic ADC Implementation Description

In the Low Frequency/Minimal Logic implementation, the Sampling Control Module controls the Successive Approximation Register, varying the time the generic output signal is applied to the RC circuit. The RC circuit voltage thus rises or falls in response to the state of the generic output, a varying amount. The LVDS input compares the changing RC circuit voltage to the Analog Input. Thus the RC circuit voltage is used to "find" the Analog Input voltage. Figure 2 shows an example with a static Analog Input (represented by the orange dotted line) set a little below one half of the full input voltage range. The vertical black dotted lines indicate the number of clocks between the SAR sample points, which are shown as green dotted lines. The first measurement takes 8 clocks, the next 4 clocks, etc.

Initially the RC circuit is set to rise to half of the full voltage swing of the Analog Input by applying a logic '1' on the Generic Output. Once the voltage is at the one half point, the output of the LVDS input will indicate whether the Analog Input value is above or below the RC circuit voltage. If the Analog Voltage is higher, the most significant bit of the digital output is a logic '1'. If the Analog voltage is lower, the digital output is a logic '0'. The SAR moves to the next bit with the sample time cut in half (for a value of one quarter of the full voltage swing). This process is repeated until the desired accuracy of the A to D converter is reached. In the example in Figure 2, observe how the RC circuit voltage gradually approaches the Analog Input value. In this simple example, the 4-bit digital output of the SAR (0101) is shown at the bottom of the diagram.

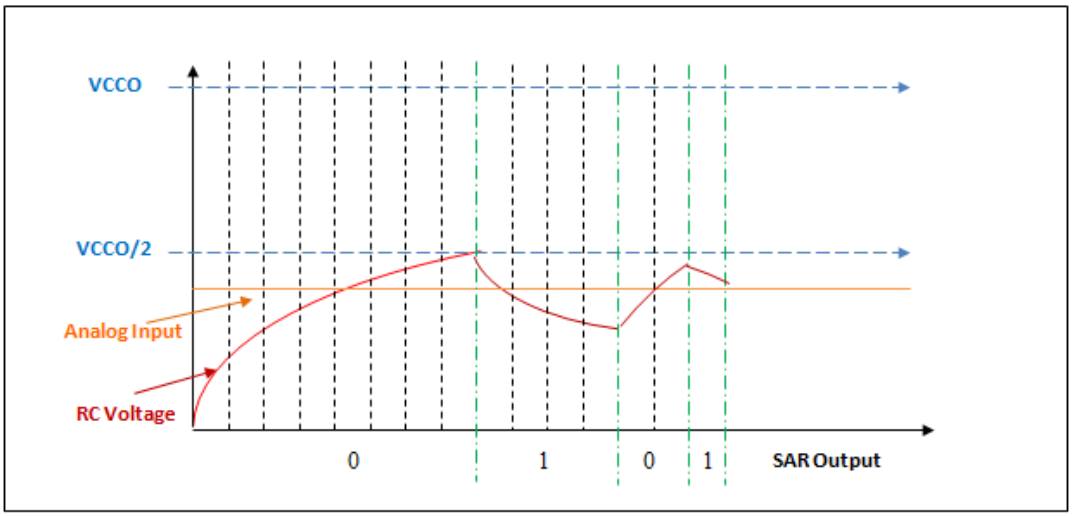

Figure 2 - Example of SAR-based A to D Converter Operation

The Low Frequency design can be used to monitor several analog voltage levels that represent the outputs of various supply voltages and environmental sensors. The CPLD implementation can monitor PCB power supply voltages (3.3V, 2.5V and 1.8V) as well as temperature and humidity sensors and an open cabinet alarm. In order to measure multiple analog inputs one LVDS input will be used for each analog voltage along with additional RC circuits. Because the analog voltages are slowly changing, the LVDS outputs can be multiplexed so that the digital logic function can be shared between each input.

Low Frequency/Minimal Logic ADC Test Results

The Low Frequency/Minimal Logic circuit without the optional digital filter has been implemented in a Lattice MachXO CPLD using an evaluation board and an input signal of .8Hz with a 0V to 3.3V swing was used. The optional memory buffer, shown in Figure 1, was used in conjunction with the Lattice Reveal Logic Analyzer feature of the Lattice ispLever design software. This feature adds the buffer memory to the target design along with the logic needed to control digital signal capture, data buffering and the data export to a computer via a JTAG cable. During testing, an FFT was run on the captured data using the PScope software from Linear Technology. The circuit response to the .8Hz Analog Input is shown in the top half of Figure 3 below.

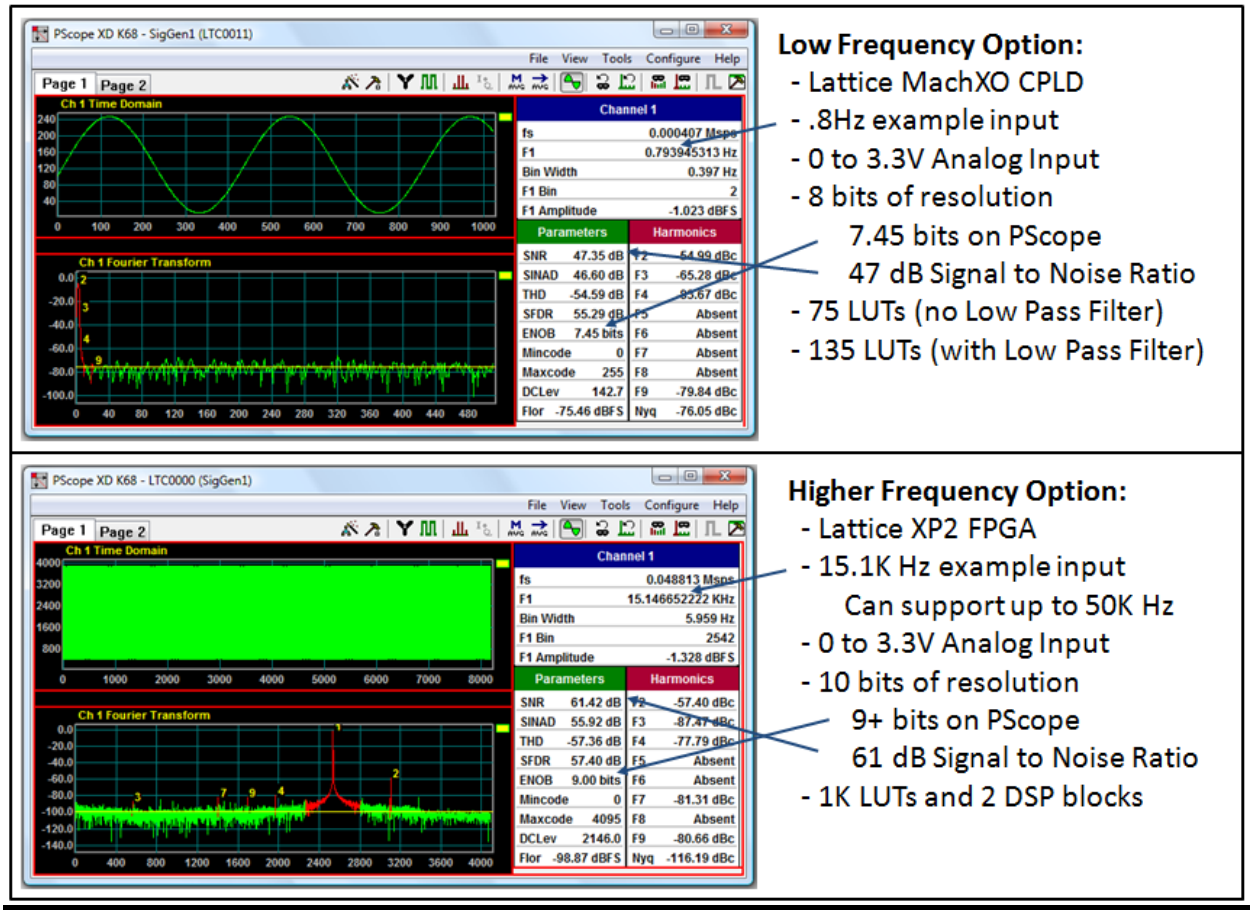

Figure 3 - Results for example A to D Converters-
Low Frequency and Higher Frequency Options

The received digital signal is shown in the top window of the PScope screen capture. The vertical axis is measured in code steps (0 to 255) and the horizontal axis is measured in samples (1024 samples in this example). The frequency is reported in the top right hand sidebar as the f1 (fundamental) frequency. The results of the FFT are shown in the lower window and the harmonic frequencies are displayed according to their dB levels via the vertical axis. A summary of the key parameters derived from the FFT are shown in the lower right sidebar, including Effective Number of Bits (ENOB) and Signal to Noise Ratio (SNR). These results show the input signal has been successfully converted to a digital signal with excellent resolution and SNR.

Higher Frequency ADC Implementation

The front-end of the higher frequency ADC option shown in the upper right side of Figure 1 still uses the RC circuit and LVDS input. An oversampling flip-flop captures the comparator results from the LVDS input. This signal is fed back via the generic LVCMOS output that drives the RC circuit. If the comparator output is a logic '1' this means the analog input is higher than the voltage from the RC circuit. The logic '1' is sampled by the flip-flop and feedback to the RC circuit, allowing the RC circuit voltage to rise. If the output of the comparator is a logic '0', the feedback signal will be a logic '0' and will drive the RC voltage lower. Via this simple feedback mechanism, the digital value with "track" the frequency of the analog input.

The graph at the lower right of Figure 4 shows a sample Analog Input waveform in red and the output of the sampling flip-flop: a blue column represents a logic '1' and a white column represents a logic '0'. Notice the way the '1's and '0's change in a common Pulse Code Modulated (PCM) format. Using a Cascaded Integrator Comb (CIC) Filter the PCM input data can be translated into an output stream that mirrors the frequency of the Analog Input stream. The CIC function basically integrates (adds or subtracts) the single bit PCM signals to generate a continuous output signal of the desired number of bits. In the example at the bottom of Figure 4, treating the blue bits as a '1' and the white bits as a '-1', it is clear by inspection that a summing (integrating) operation will generate a digital representation of the input waveform. (Notice that the output waveform will be shifted by about a half-cycle, since a sequence of '1's will correspond to an increase in the digital value, whereas in the diagram in Figure 4, a sequence of '1's is shown during the 'high' portion of the waveform and a series of '0's is generated during the 'low' portion.)

The voltage from the RC circuit may oscillate around the Analog Input level due to the "tracking" process created b y the feedback loop. The RC circuit voltage will be moved from just above to just below the Analog Input level as the oversampling flip-flop changes between a '1' and '0' result. This process continues until the Analog Input level changes. This high frequency noise can be eliminated by the use of the optional digital filters.

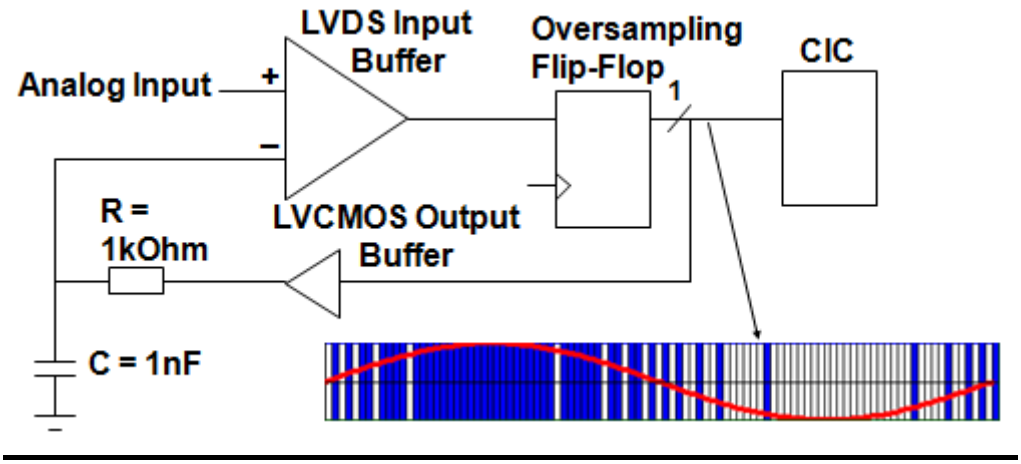

Figure 4 - Results of Conversion Stage of Delta Sigma Modulator

The higher frequency design can monitor multiple audio frequency sidebar signals used to communicate operational and environmental conditions. For example, 5K Hz and 12K Hz signals can be issued periodically to indicate the state of a remote audio monitoring system. These signals can indicate the environmental condition (temperature and humidity) of the equipment. As in the previous example, multiple analog signals can be supported by simply adding more LVDS inputs. The design could be a hub for up to 8 analog signals. By time multiplexing the inputs, only a single copy of the digital logic would need to be used.

Higher Frequency ADC Test Results

The higher frequency ADC circuit has been implemented in a Lattice XP2-17 FPGA using an evaluation board. An input signal of 15K Hz with a 0V to 3.3V swing was used during testing. The analog signal was processed using the Option 2 circuit shown in Figure 1 using a Digital Filter option. The results are shown in the bottom half of Figure 3 above, with the received signal shown in the top window and the FFT in the bottom, with the f1 frequency of 15.1K Hz the most prominent. The results reported in the lower sidebar give the ENOB at 9 and the SNR as 61 dB. These results show the input signal has been successfully converted to a digital signal with excellent resolution and SNR.

Characteristics	**Low Frequency / Minimal Logic**	**High Frequency**
Supported Bandwidth	DC – 1khz	DC – 50Khz
FPGA Logic utilized	75 LUTs	1k LUTs
Optional Low Pass Filter resources	60 LUTs	2 sysDSP blocks
Target Devices	Mach XO1200, MachXO2280	ECP2/M, XP2 or ECP3

Table 1 - Summary of the Major Characteristics of Both Design Options

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