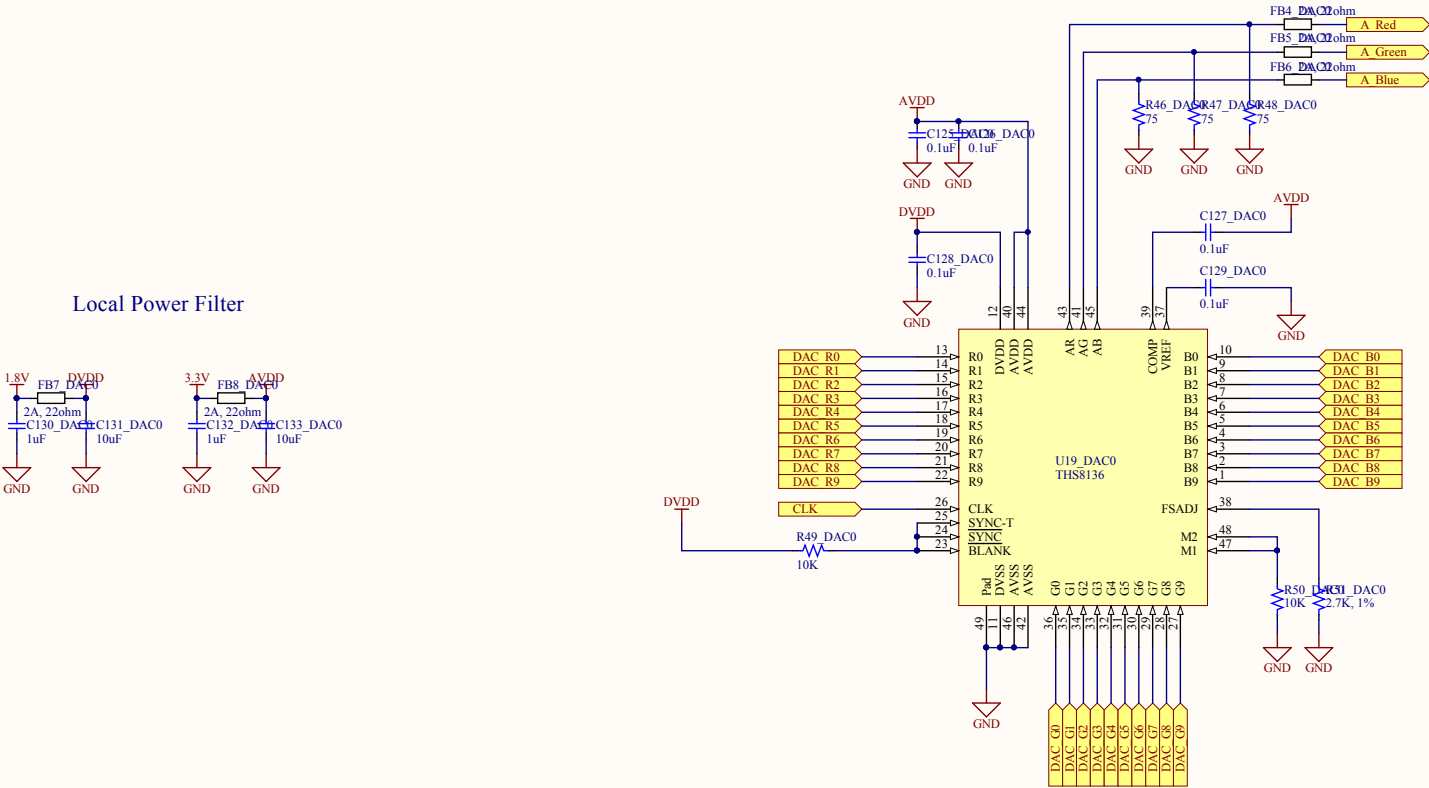
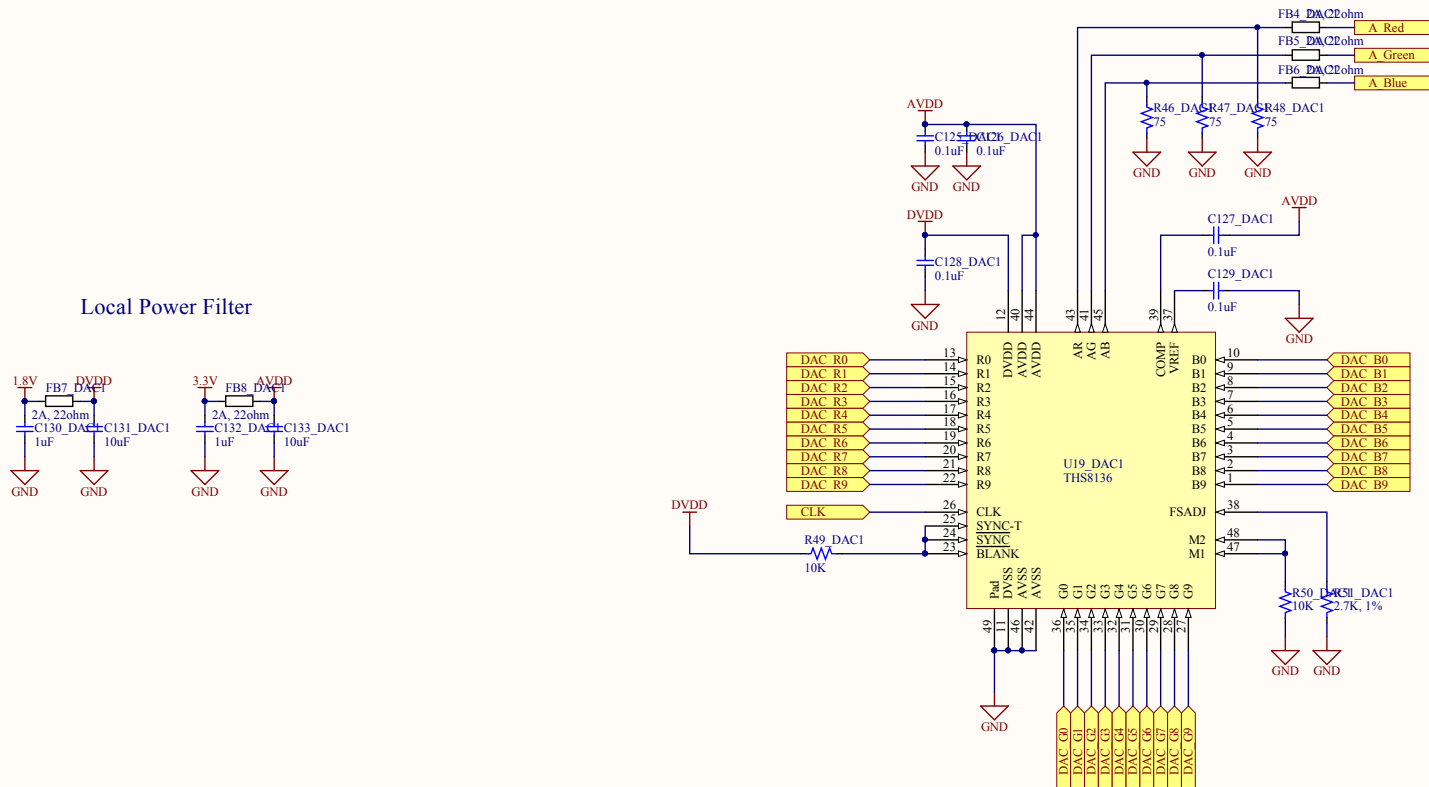


Triple 10-BIT 180-MSPS Video DAC



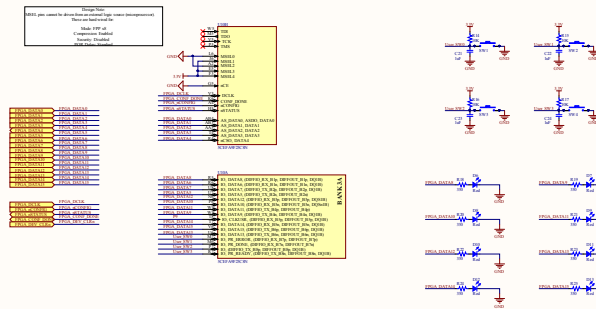
Title		
Size	Number	Revision
B		
Date:	10/29/2015	Sheet of
File:	C:\tmp\10-Bit DAC.SchDoc	Drawn By:

# Triple 10-BIT 180-MSPS Video DAC



Title			
Size B	Number		Revision
Date:	10/29/2015	Sheet of	
File:	C:\tmp\10-Bit DAC.SchDoc	Drawn By:	

## FPGA Configuration + Shared I/O + Push Buttons



## Cyclone 5E A9 FPGA

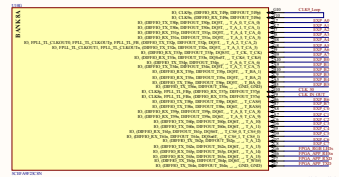
## Power + I/O Voltage

**MultiVolt I/O Interface in Cyclone V Devices**

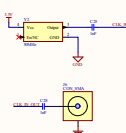
The MultiVolt I/O interface feature allows Cyclone V devices in all packages to interface with systems of different supply voltages.

Table 5-10: MultiVolt I/O Support in Cyclone V Devices

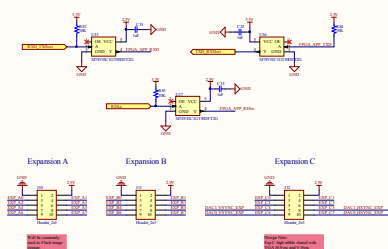
$V_{CC}$ (V)	$V_{CEQ}$ (V)	Input Signal (V)	Output Signal (V)
1.2	2.5	1.2	1.2
1.25	2.5	1.25	1.25
1.35	2.5	1.35	1.35
1.5	2.5	1.5, 1.8	1.5
1.8	2.5	1.5, 1.8	1.8
2.5	2.5	2.5, 3.0, 3.3	2.5
3.0	3.0	2.5, 3.0, 3.3	3.0
3.3	3.3	2.5, 3.0, 3.3	3.3



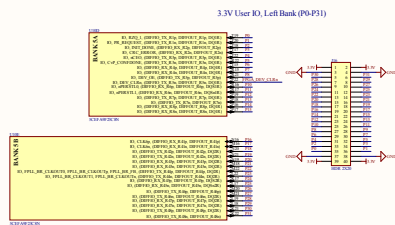
### Clock Sources



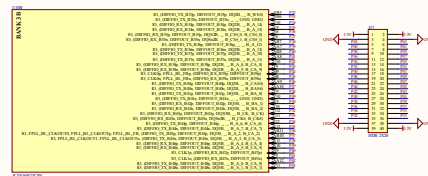
## USB Commes



### User I/O Banks

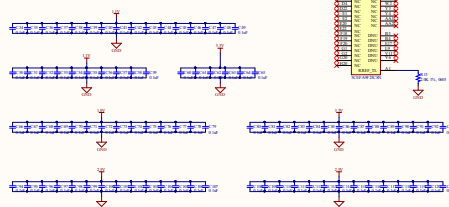


### 3.3V User IO, Left Bank (P0-P31)

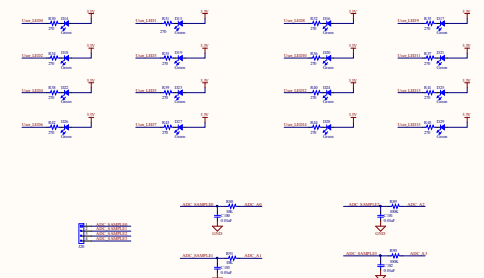
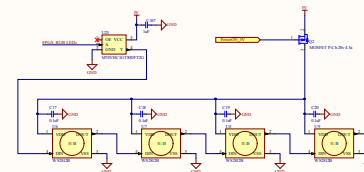
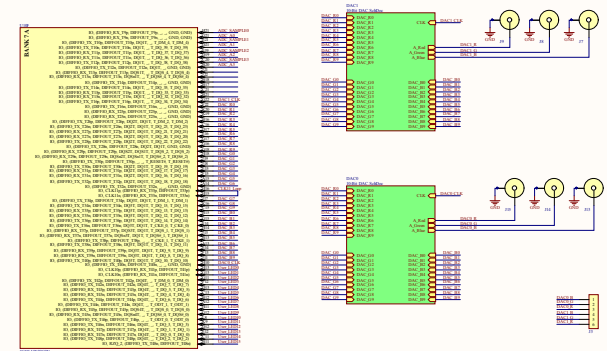
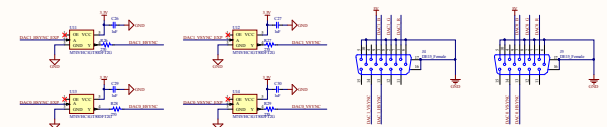


### 3.3V User IO, Right Bank (P32-P63)

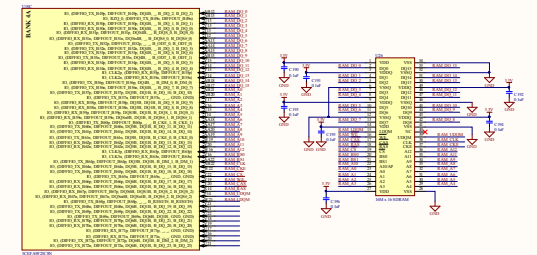
## Local FPGA Power Rail Decoupling Capacitor Banks



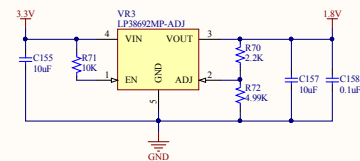
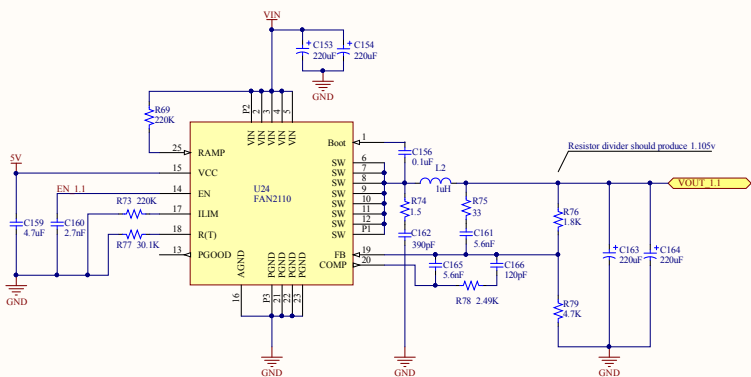
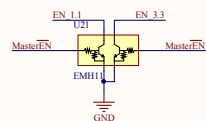
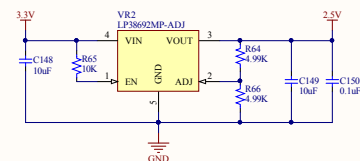
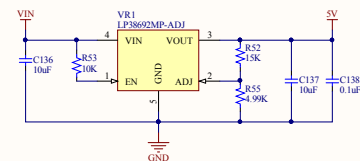
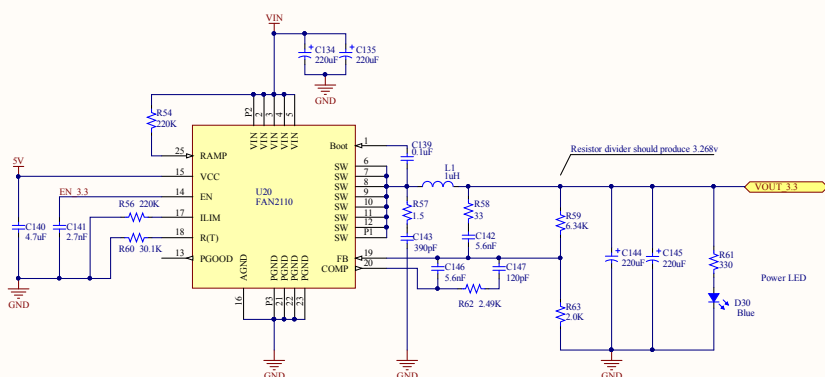
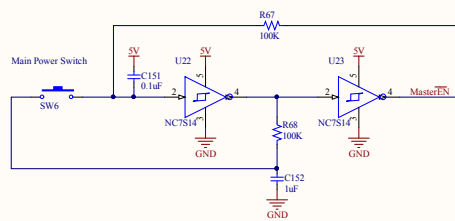
## DACs + VGA + User LEDs



16M x 16 SD RAM



PowerON\_5V MasterEN



Title		
Size	Number	Revision
C		
Date:	10/29/2015	Sheet of
File:	C:\mp_FAN2110_Power_1.1+3.3_Sch	Drawn By:

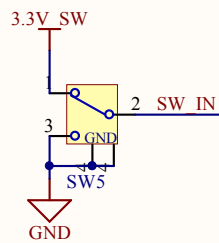


The diagram shows three yellow arrow-shaped boxes on the left, each pointing to a blue line on the right. The top box is labeled 'TXD' and points to the 'UART TX' line. The middle box is labeled 'RXD' and points to the 'UART RX' line. The bottom box is labeled 'RESn' and points to the 'UART RESn' line.

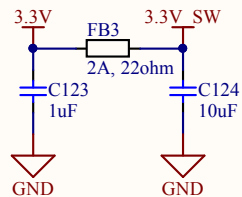
Title		
Size A	Number	Revision
Date:	10/29/2015	Sheet of
File:	C:\tmp\...\FTDLSchDoc	Drawn By:

# Device Configuration Select

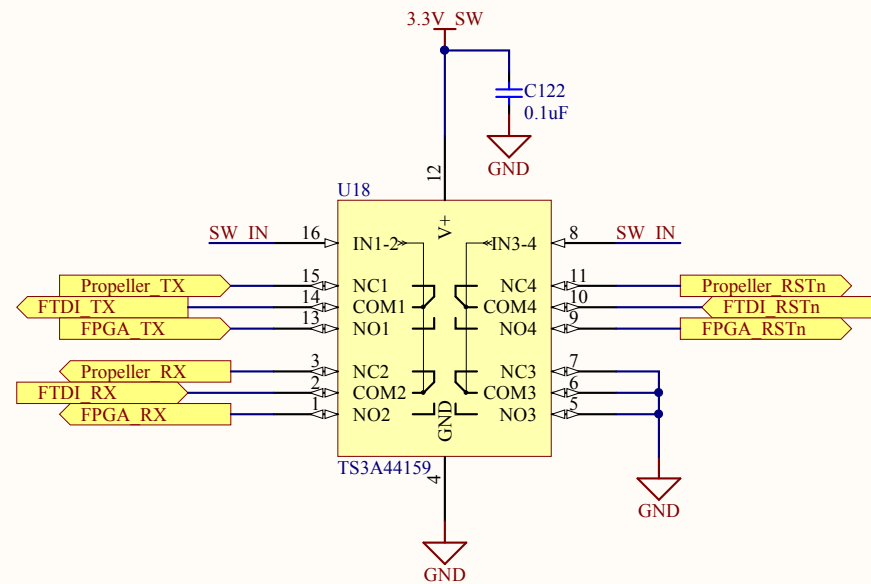
## Device Select Switch



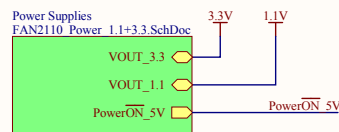
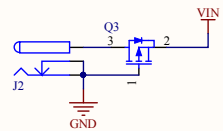
## Power Supply Conditioning



## Device Select MUX/DEMUX



Title		
Size	Number	Revision
A		
Date:	10/29/2015	Sheet of
File:	C:\tmp\...\LogicSwitch.SchDoc	Drawn By:



A

A

B

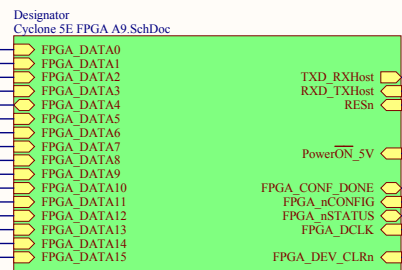
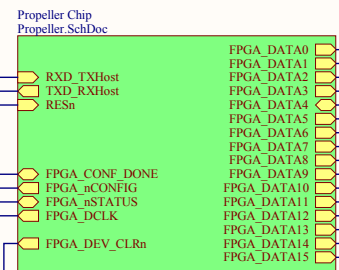
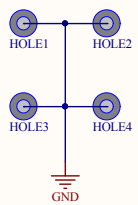
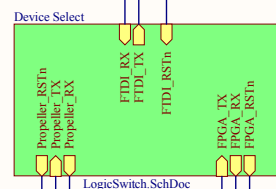
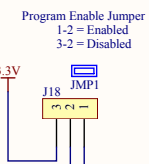
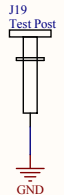
B

C

C

D

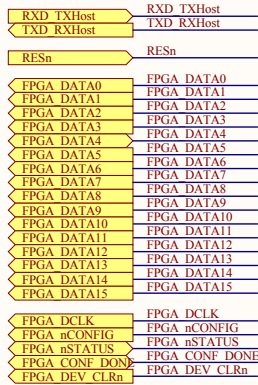
D



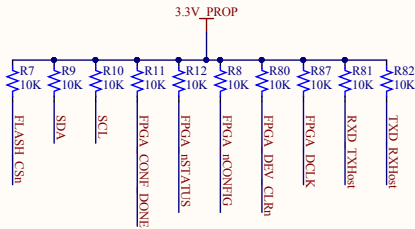
Title		
Size	Number	Revision
B		
Date:	10/29/2015	Sheet of
File:	C:\tmp\...ParallaxA9 FPGA Schematic	3 of 3
Drawn By:		

# Propeller Chip FPGA Configuration Loader

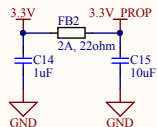
## Off-Sheet Ports



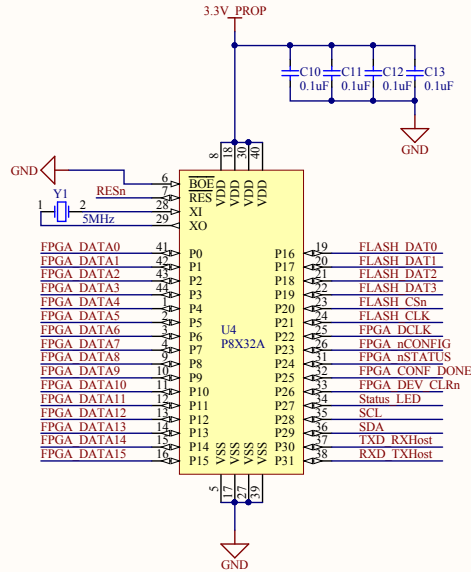
## Pull-ups



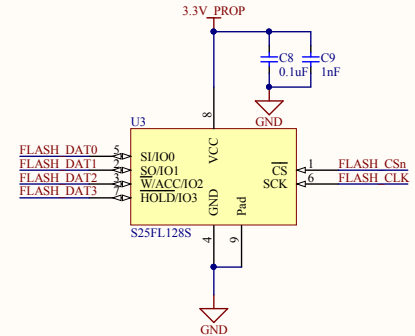
## Local Power Filter



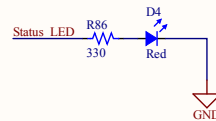
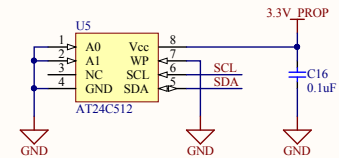
## Propeller Chip



## 8MB Flash



## 64KB EEPROM



Title		
Size	Number	Revision
B		
Date:	10/29/2015	Sheet of
File:	C:\tmp\Propeller SchDoc	Drawn By:



