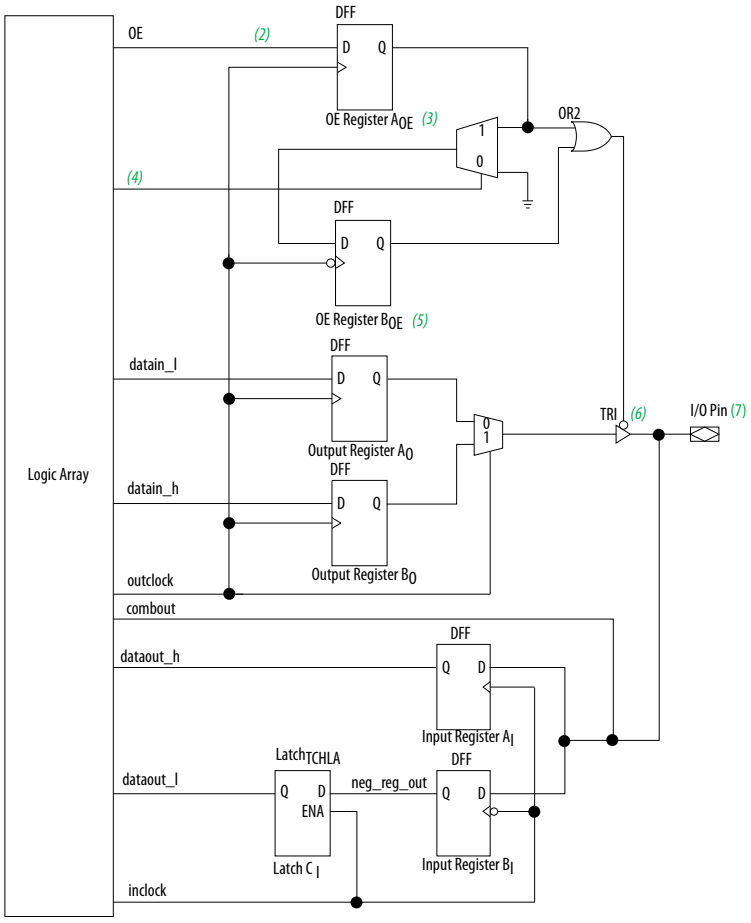
(`dataout_h` and `dataout_l`) can be disabled. These features are especially useful for generating data strobes like DQS.

Figure 5: Bidirectional DDR I/O Path Configuration

This figure shows the bidirectional DDR I/O configuration for Stratix series and APEX II devices.



1) All control signals can be inverted at the IOE.
2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before input to the AOE register during compilation. If desired, you can change the OE back to active low.
3) The AOE register generates the enable signal for general-purpose DDR I/O applications.
4)This line selects whether the OE signal should be delayed by half a clock cycle.
5) The BOE register generates the delayed enable signal for the write strobes or write clocks for memory interfaces.
6) The tri-state enable is by default active low. You can, however, design it to be active high.
7) You can also have combinational output to the I/O pin. This path is not shown in the diagram.

Related Information

- **Stratix II Architecture**
  For more information about clock signals and output enable signals for Stratix series
- **APEX II Programmable Logic Device Family Data Sheet**
  For more information about clock signals and output enable signals for APEX II devices
- **Implementing Double Data Rate I/O Signaling in Cyclone Devices**
  For more information about the DDR registers in Cyclone devices