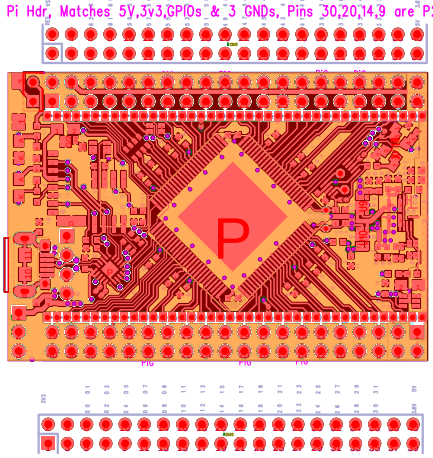
P2D2Pi Pi Header pinout variant, of P2D2

AP7332 -> 2 x NCP187, Better PSRR, Lower Noise, better thermally Higher Io
Added more copper, and many more Thermal Vias
Original Vias Count : 128, Revised : Via Count : 202
Simplified POUR and set up for 4 layer PCB, MAX GND planes

JG: Pi Hdr, Matches 5V,3v3,GPIOs & 3 GNDs, Pins 30,20,14,9 are P2.io



JG: Added RN2, U5,UC1 - PJB revs
JG: Fixed XG1 MSOP10 to 0.5mm

JG: Added C14, J2, J6, C11, XO1a (3225 XO) XO1B (5032) new parts
JG: Added J4,J5 for EFM8UB3 C2D debug
JG: Changed USB to 10118194. moved to board edge
NCP187 LDO similar (NPC) : DFN2020, EN>IN, Higher noise TLV75533PDRVR 0.5A & TLV75733PDRVR 1A
NCP187 PAD 1.12x1.72 TLV75533PDRVR PAD 1x1.6 CL=0.65mm

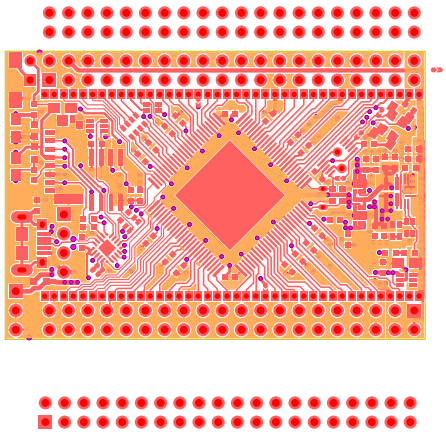
JG:Jumper on VIO on Pi Connector (avoids Pi.3v3 contention P2.3v3 ?)

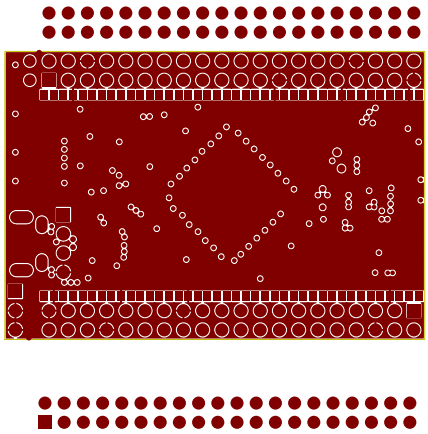
JG: VIO, or VA, VB best to connect to Pi.3v3?

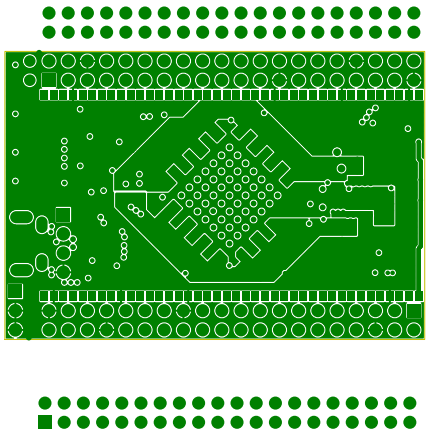
JG: Pi5V to Vcc, or maybe to VIN or VBUS ?

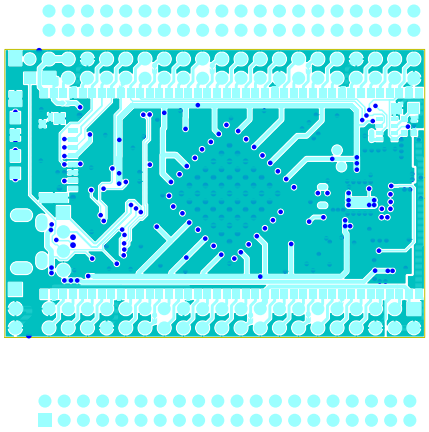
JG: PADS Clearance as imported 23, Min 3.9mils
JG:PADS connectivity as imported 20
JG:P2D2r2p fill areas rationalised, cleanups, Zero DRC Errors

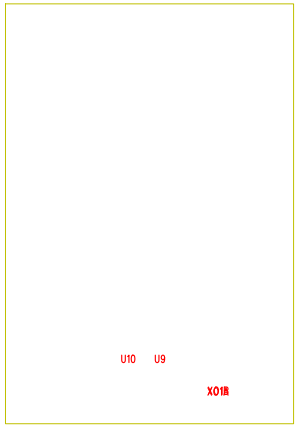
Newer PLD version https://www.ebay.com/itm/3-5-TFT-LCD-Touch-Screen-Display-128M-SPI-Case-For-Raspberry-Pi-3-B-Zero-W/3234072266
LCD example: https://www.raspberrypi.org/forums/viewtopic.php?t=124961










U10
U9
XO1晶