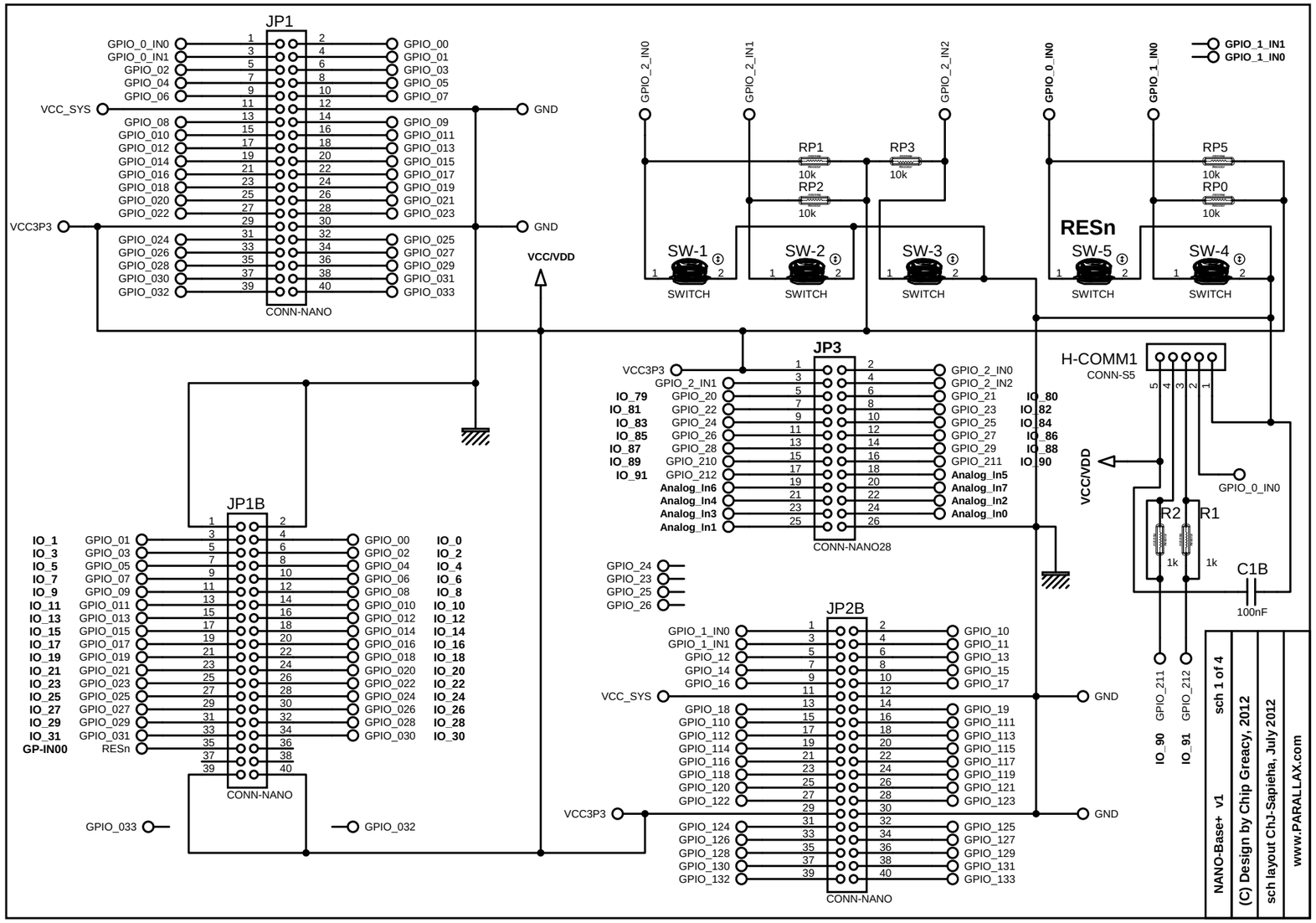
JP1
CONN-NANO
VCC_SYS
VCC3P3
GND
VCC/VDD
JP1B
CONN-NANO
RESn
GPIO_033
GPIO_032
JP3
CONN-NANO28
JP2B
CONN-NANO
RP1
RP2
RP3
RP5
RP0
10k
SW-1
SW-2
SW-3
SW-5
SW-4
SWITCH
H-COMM1
CONN-S5
R2
R1
1k
C1B
100nF
GPIO_0_IN0
GPIO_211
GPIO_212
IO_90
IO_91
NANO-Base+ v1
sch 1 of 4
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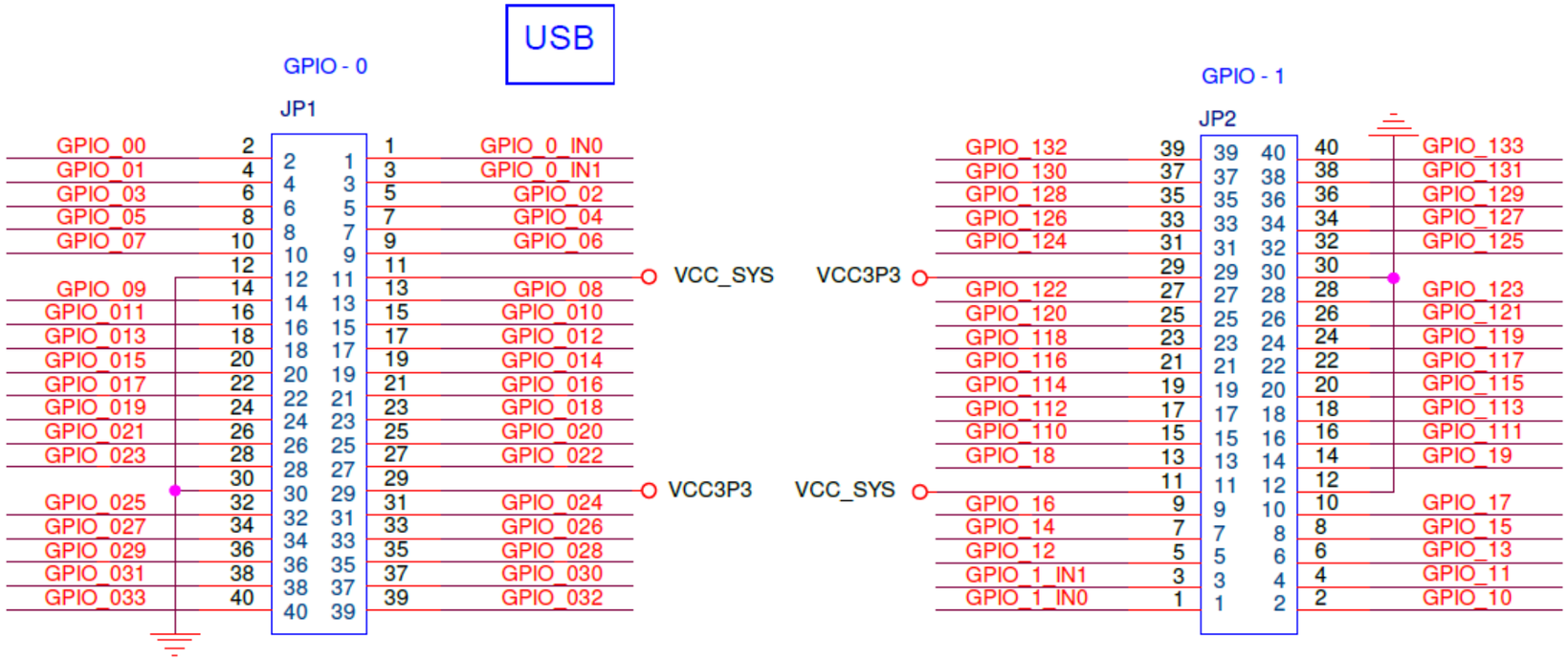
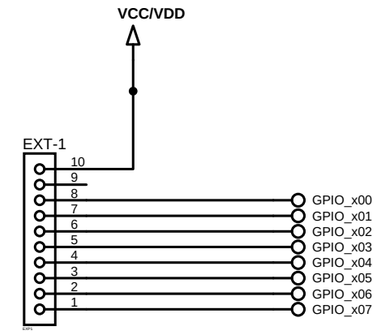
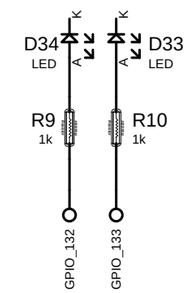


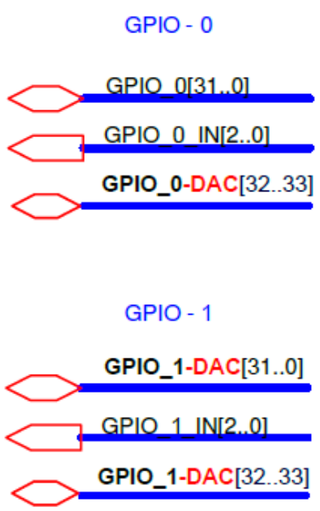


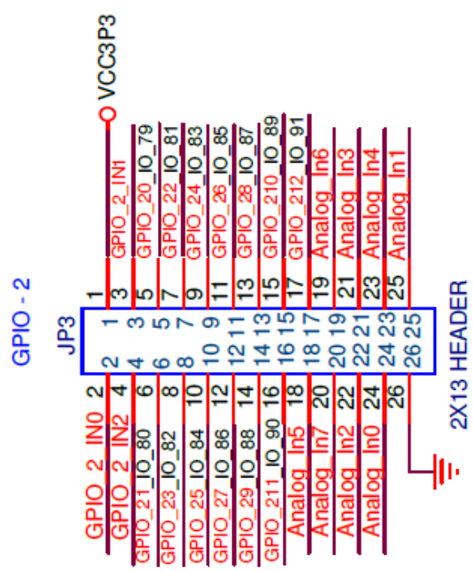
Connector for Analog IN

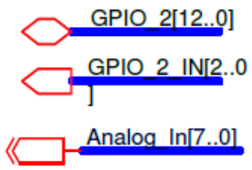
If Chip say that can be implemented



Spare parts







NANO-Base+ v1	sch 2 of 4
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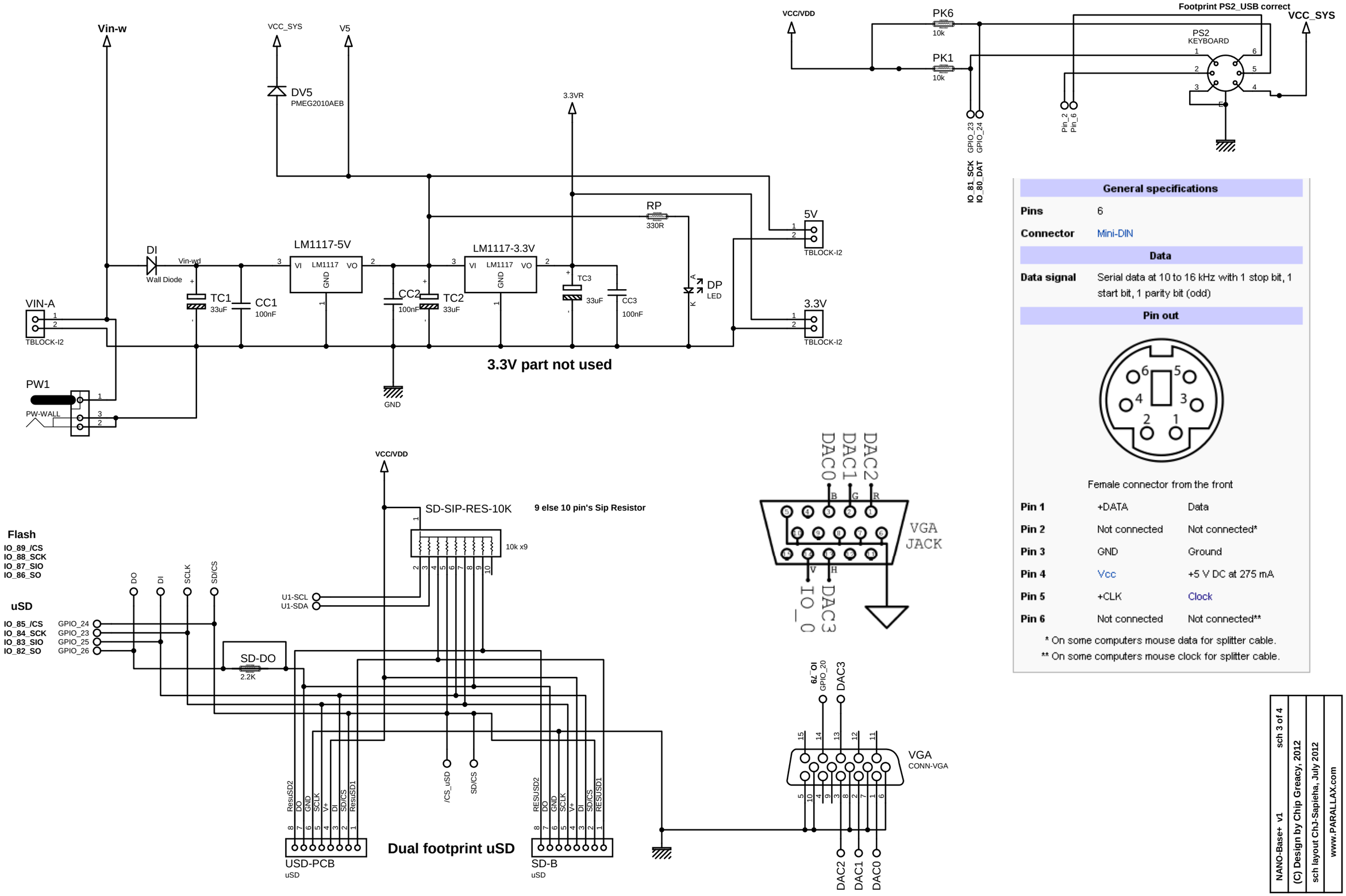

General specifications		
Pins	6	
Connector	Mini-DIN	
Data		
Data signal	Serial data at 10 to 16 kHz with 1 stop bit, 1 start bit, 1 parity bit (odd)	
Pin out		

Female connector from the front

Pin 1	+DATA	Data
Pin 2	Not connected	Not connected*
Pin 3	GND	Ground
Pin 4	Vcc	+5 V DC at 275 mA
Pin 5	+CLK	Clock
Pin 6	Not connected	Not connected**

* On some computers mouse data for splitter cable.

** On some computers mouse clock for splitter cable.

NANO-Base+ v1 sch 3 of 4

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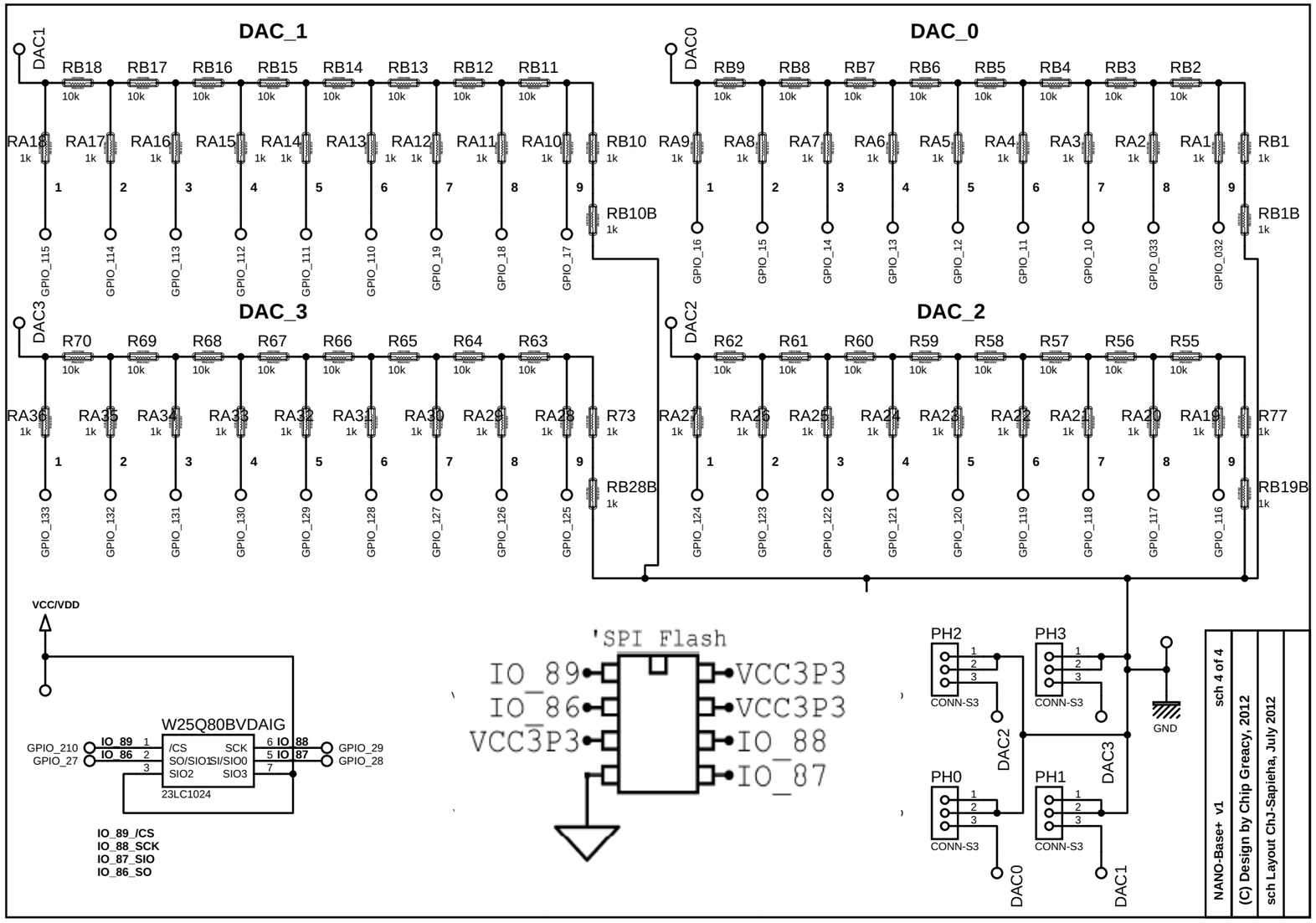
DAC_1
DAC1
RB18 RB17 RB16 RB15 RB14 RB13 RB12 RB11
10k
RA18 RA17 RA16 RA15 RA14 RA13 RA12 RA11 RA10 RB10
1k
RB10B
GPIO_115 GPIO_114 GPIO_113 GPIO_112 GPIO_111 GPIO_110 GPIO_19 GPIO_18 GPIO_17
DAC_0
DAC0
RB9 RB8 RB7 RB6 RB5 RB4 RB3 RB2
RA9 RA8 RA7 RA6 RA5 RA4 RA3 RA2 RA1 RB1
RB1B
GPIO_16 GPIO_15 GPIO_14 GPIO_13 GPIO_12 GPIO_11 GPIO_10 GPIO_033 GPIO_032
DAC_3
DAC3
R70 R69 R68 R67 R66 R65 R64 R63
RA36 RA35 RA34 RA33 RA32 RA31 RA30 RA29 RA28 R73
RB28B
GPIO_133 GPIO_132 GPIO_131 GPIO_130 GPIO_129 GPIO_128 GPIO_127 GPIO_126 GPIO_125
DAC_2
DAC2
R62 R61 R60 R59 R58 R57 R56 R55
RA27 RA26 RA25 RA24 RA23 RA22 RA21 RA20 RA19 R77
RB19B
GPIO_124 GPIO_123 GPIO_122 GPIO_121 GPIO_120 GPIO_119 GPIO_118 GPIO_117 GPIO_116
VCC/VDD
W25Q80BVDAIG
GPIO_210 GPIO_27
IO_89 IO_86
/CS SO/SIO1 SIO2 SCK SI/SIO0 SIO3
IO_88 IO_87
GPIO_29 GPIO_28
23LC1024
IO_89_/CS
IO_88_SCK
IO_87_SIO
IO_86_SO
'SPI Flash
IO_89 IO_86 VCC3P3
VCC3P3 VCC3P3 IO_88 IO_87
PH2 PH3 PH0 PH1
CONN-S3
DAC2 DAC3 DAC0 DAC1
GND
NANO-Base+ v1
sch 4 of 4
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