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DS00VQ100

1. Introduction

The DS00VQ100 is an integrated circuit that controls a laser rangefinder. It is designed to provide all the necessary signals for a pulsed laser with an avalanche photodiode or pin diode detector. Interfacing is via a SPI bus configured in slave mode with an active high chip select. An interrupt indicates when a new result is ready.

The following subsystems are included:

- SPI bus to a master microprocessor.
- Control system for a pulsed laser.
- Control system for an APD detector.
- Time of flight measuring system.
- General purpose control outputs.
- Diagnostics and testing ports.
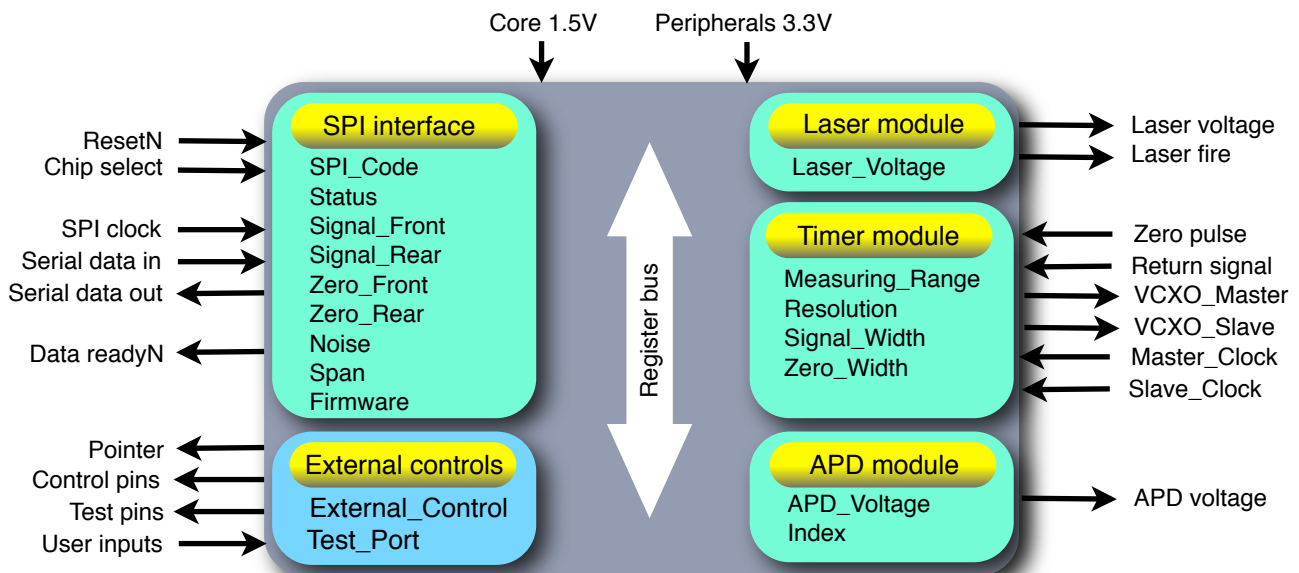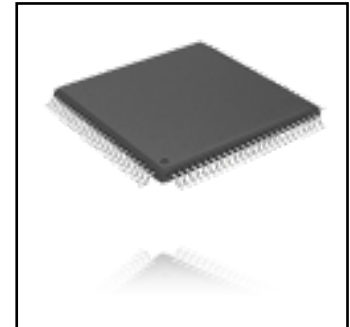
Block diagram of DS00VQ100 subsystems

Advantages

- A system-on-a-chip solution to time-of-flight, laser distance measurement.
- Adjustable measuring range.
- Adjustable resolution.
- Easy to configure.
- 16 bit timing accuracy.
- Management of laser power.
- Management of APD gain and noise.
- The return signal is filtered and verified before measurement.
- Internal signals are visible on test ports.
- User inputs and outputs for auxiliary controls.

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[Table of contents to be inserted here]

Definitions

Within this document the following abbreviations are used:

APD - Avalanche Photo Diode.
LVDS - Low Voltage Differential Signal as per ANSI/TIA/EIA-644
SignalN - Differential signals that are active low are indicated by the letter "N" at the end of their name.
SignalP - Differential signals that are active high are indicated by the letter "P" at the end of their name.
VCXO - Voltage Controlled Crystal Oscillator.

Specifications

Parameter	Standard units	Notes
Operating voltage	Core = 1.5 ± 0.1 VDC	At xxx mA
	I/O = 3.3 ± 0.15 VDC	At xxx mA
Operating power	A mW + B mW	Core + I/O
Package	TQFP 100	
Master clock / Slave clock	12.8 MHz	VCXO pull range ±50ppm
Minimum span	156.25 ns	Equivalent range = 23.44 m
Maximum span	2500.00 ns	Equivalent range = 375.00 m
Highest resolution	< 60 ps	Equivalent resolution < 1 cm
Lowest resolution	> 400 ps	Equivalent resolution > 6 cm
Fastest update rate	> 20 times per second	Determined by VCXO pull range
Slowest update rate	< 1 time per second	Determined by range and resolution
Temperature range	0°C to +70°C	DS00VQ100-C
	-40°C to +85°C	DS00VQ100-I
Firmware number		Hex 40, Dec 64

Summary of External Requirements

- The core and I/O power supplies should be linear regulators with minimum ripple.
- The input for the return signal is LVDS compliant and can interface directly with a differential amplifier.
- The input for the zero signal is 3.3V CMOS compliant and the signal must be inverted.
- The voltage and fire signals to the laser are LVDS compliant.
- The voltage signal to the APD is LVDS compliant.
- The master and slave oscillators must be high stability, low jitter, voltage controlled, crystal oscillator modules (VCXO).

Signals and Pin Assignments

Signal	I/O	Type	Pin	Active	Function
NRESET	Input	3V3 CMOS 10kΩ pull up		Low	System reset on power up
CS	Input	3V3 CMOS 10kΩ pull down		High	Chip select
SPI_Clock	Input	3V3 CMOS 10kΩ pull down		Clock	Clock for SPI interface
Serial_Data_In	Input	3V3 CMOS 10kΩ pull down		Data	SPI data in
Serial_Data_Out	Output	Tri-state, 10kΩ pull down		Data	SPI data out
Data_ReadyN	Output	4mA drive, low slew rate		Low	SPI data ready
Master_Oscillator	Input	3V3 CMOS		Clock	Main system clock
Slave_Oscillator	Input	3V3 CMOS		Clock	Secondary system clock
VCXO_Master	Output	PWM		High	Master_Clock control voltage

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Signal	I/O	Type	Pin	Active	Function
VCXO_Slave	Output	PWM		Low	Slave_Clock control voltage
LaserP	Output	LVDS - PWM		High	Voltage control for laser
LaserN	Output	LVDS - PWM		Low	Voltage control for laser
FireP	Output	LVDS - PWM		High	Laser fire pulse
FireN	Output	LVDS - PWM		Low	Laser fire pulse
SignalP	Input	LVDS		High	Return signal
SignalN	Input	LVDS		Low	Return signal
ZeroN	Input	3V3 CMOS		Low	Outgoing laser signal - inverted
APDP	Output	LVDS - PWM		High	Voltage control for APD
APDN	Output	LVDS - PWM		Low	Voltage control for APD
Pointer_Control	Output	8mA drive, low slew rate		High	Pointer on/off control
Control_1	Output	8mA drive, low slew rate		User	User controllable output
Control_2	Output	8mA drive, low slew rate		User	User controllable output
Control_3	Output	8mA drive, low slew rate		User	User controllable output
Test_0	Output	4mA drive, high slew rate		Multiplex	CS, PWM_Sync, TEX_Sync
Test_1	Output	4mA drive, high slew rate		Multiplex	SPI_Clock, Live_Return, TEX_Return
Test_2	Output	4mA drive, high slew rate		Multiplex	Serial_Data_In, Live_Zero, TEX_Zero
Test_3	Output	4mA drive, high slew rate		Multiplex	Serial_Data_Out, Noise_Window, Return_Valid
Test_4	Output	4mA drive, low slew rate		User	User controllable output
Test_5	Output	4mA drive, low slew rate		User	User controllable output
Input_0	Input	3V3 CMOS 10kΩ pull down		User	User controllable input
Input_1	Input	3V3 CMOS 10kΩ pull down		User	User controllable input
Gnd		1, 9, 25, 38, 46, 51, 67, 75, 88, 99			
Vcc		17, 37, 68, 89			
VccB1		18, 66			
VccB2		39			
VccB3		18			
VccB0		87			

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Power and Reset

The power supply for the core is 1.5V DC at A mA. All power connections should be routed. The I/O peripherals are powered from 3.3V DC at B mA with a separate supply being available for each bank (each side of the chip package). All I/O power pins should be connected. A common or separate 3.3 V supplies may be used.

The ResetN input is an active low, master reset for the entire chip. All internal registers default to low or zero on reset. This means that the laser will be off and the APD voltage will be zero. A minimum reset width of 1us should be used.

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2. SPI Interface

Connections		
CS	Input	Chip select.
SPI_Clock	Input	SPI clock driven by microprocessor.
Serial_Data_In	Input	Data from the microprocessor.
Serial_Data_Out	Output	Data to the microprocessor. This is a tristate port.
Data_ReadyN	Output	Signal to the microprocessor that new data is available for reading. Active low.
Internal registers		
SPI_Code	Write	Determines the source of the latch that saves new SPI data.
Index	Write	3 LSB's flag the data to be used next.
Status	Read	3 LSB's indicate which set of data was used last.

Read and Write Sequence

The SPI interface is used to connect the DS00VQ100 to a microprocessor. The microprocessor acts as the master whilst the DS00VQ100 has a slave configuration. A transmit/receive sequence starts when CS goes high. Data is clocked by SPI_Clock under the control of the microprocessor.
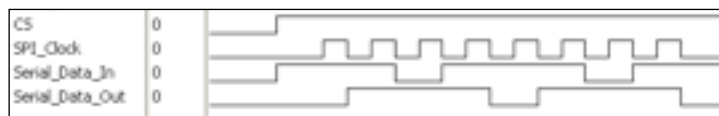
The first 8 bits of a data transfer

Data Stream Format

With each transfer of data, a sequential string of 112 bits is clocked simultaneously into and out of the interface. The data transmitted by the microprocessor is formatted as 1 x 16bit + 12 x 8bit values whilst the data received is formatted as 6 x 16 bit + 2 x 8 bit values. Each value corresponds to an internal data register that connects to the various controllers inside the chip. There are different registers for transmitted and received data.

A full transfer of data initiated by the Data_ReadyN signal

There is no addressing required for the SPI data transfer. A communication consists of a fixed length transmission with simultaneous reception. Every byte is read and written during the transfer.

"Transmit only" and "receive only" data transfers are permitted. For transmit only, ignore the received data. For receive only, transmit a string of zeros or ones. The SPI_Code will be invalid and therefore no data will be written to the internal registers.

The Data_ReadyN output goes low whenever a new reading has been completed. It can be used as an interrupt source for the controlling microprocessor. The rising edge of CS resets Data_ReadyN. If it is not

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reset, Data_ReadyN remains low until the next data transmission. Results continue to be updated even when Data_ResetN is low. This means that the latest result will always be read from the SPI interface. Results are not updated during the data transfer so long as the CS remains high.

Internal Registers

Byte #	Transmit	Register	Receive	Register
0	8 bit	Unused	8 bit	Firmware
1	8 bit	Unused	16 bit	Zero_Rear [MSB]
2	8 bit	Unused		Zero_Rear [LSB]
3	8 bit	Signal_Width	16 bit	Zero_Front [MSB]
4	8 bit	APD_Voltage		Zero_Front [LSB]
5	8 bit	Laser_Voltage	16 bit	Signal_Rear [MSB]
6	8 bit	Index		Signal_Rear [LSB]
7	8 bit	Zero_Width	16 bit	Signal_Front [MSB]
8	8 bit	Test_Port		Signal_Front [LSB]
9	8 bit	Measuring_Range	16 bit	Noise [MSB]
10	16 bit	Resolution_L [LSB]		Noise [LSB]
11		Resolution_H [MSB]	16 bit	Span [MSB]
12	8 bit	External_Control		Span [LSB]
13	8 bit	SPI_Code	8 bit	Status

Transmit and receive registers

SPI_Code Register

Data transmitted by the microprocessor is stored using one of two possible latch sources. The latch source is determined by the last 8 bit value transmitted by the microprocessor, SPI_Code. If this code is set to Hex 77 (Dec 119) then the new data is written as soon as the CS line goes low at the end of the transmission. If SPI_Code is set to Hex AA (Dec 170) then the new data is written synchronously with a measuring cycle by internal control logic. All other values are invalid and prevent data from being written accidentally.

SPI_Code	SPI data latch source
Hex 77 (Dec 119)	CS falling edge - immediate write to registers
Hex AA (Dec 170)	Internal - synchronous write to registers

SPI_Code register values

SPI Index Register

Data written by the microprocessor into the SPI registers configure the DS00VQ100 for its next measuring cycle. In the same transfer, the results that are received by the microprocessor are from the measurement that has just been completed. This means that the active configuration and results are always one transfer sequence apart. If different values are used in each transmission then it is important to keep track of which configuration data is associated with which result.

The 3 LSB's of the Index register are used to tag the transmitted data string so that successive results can later be identified. The microprocessor keeps track of which results are associated with which data by reading back the the Index value in the 3 LSB's of the Status register. The example below shows how a sequence of four different data streams are identified when the results are read back.

Stream	Write	Read
1	Index = 01 & Data A	Status = x4 & Result D
2	Index = 02 & Data B	Status = x1 & Result A
3	Index = 03 & Data C	Status = x2 & Result B
4	Index = 04 & Data D	Status = x3 & Result C
5	Index = 01 & Data A	Status = x4 & Result D
6	Index = 02 & Data B	Status = x1 & Result A
7	Index = 03 & Data C	Status = x2 & Result B
8	Index = 04 & Data D	Status = x3 & Result C
9	Index = 01 & Data A	Status = x4 & Result D

*An example of a data sequence using the Index register*

The primary use of the Index register is to track different values of APD bias voltage that are used in successive readings. These voltages will alter the gain and noise conditions under which a reading is taken thereby allowing for on-the-fly optimization of the return signal.

ADuC842 SPI Configuration

SPIM=1;   // SPI master mode
CPOL=0;   // Clock idles low
CPHA=0;   // Read on rising edge clock, shift on falling edge clock
SPE=1;   // Enable SPI bus
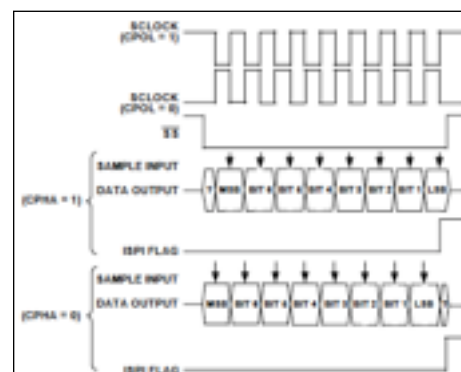
3. Laser Module

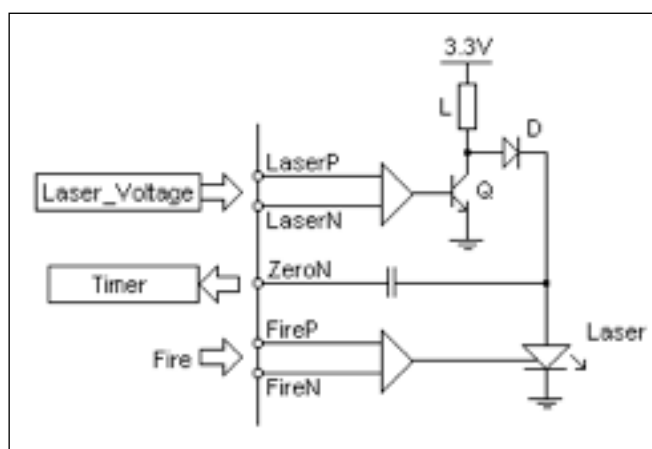| Connections		
LaserP	Output	Positive PWM signal for laser power supply - LVDS.
LaserN	Output	Negative PWM signal for laser power supply - LVDS.
FireP	Output	Positive fire signal for laser - LVDS.
FireN	Output	Negative fire signal for laser - LVDS.
ZeroN	Input	Signal informing the timer module that the laser has fired 3.3V CMOS.
Internal registers		
Laser_Voltage	Write	An 8 bit value that sets the voltage of the laser power supply.

The Laser Module controls the operating voltage and firing signals of a high power, pulsed laser.

The laser module drives a high efficiency, switch-mode power supply that directly feeds the discharge capacitor of an avalanche driver circuit within the laser package. Voltage pulses are generated shortly before the firing of the laser. The LaserP and LaserN voltage control signals are LVDS compatible and are designed to drive a switching transistor through a comparator.

The fire signals are also LVDS compatible and are designed to drive an avalanche transistor or avalanche FET through a high speed comparator. The laser is fired at the Master_Clock frequency divided by 512. For 12.8 MHz crystal this gives a 25 kHz firing rate.

The laser power supply controls are in the form of synchronous, PWM signals. These signals are timed to be active when the laser firing pulse is active. This prevents the avalanche firing transistor from "pumping" the power supply and getting hot. The laser voltage is set by the Laser_Voltage register that is an 8 bit value representing the "on" time of the PWM. If this value is less than 16 (dec) then the power supply is off and the laser is not fired.

The ZeroN input pin monitors the firing of the laser via the avalanche discharge. This negative going signal is fed to one of the channels of the timing module.


Typical laser voltage control and firing configuration.

4. APD Module

Connections		
APDP	Output	Positive PWM signal for APD power supply. LVDS.
APDN	Output	Negative PWM signal for APD power supply. LVDS.
SignalP	Input	Return signal - positive polarity. LVDS.
SignalN	Input	Return signal - negative polarity. LVDS.
Internal registers		
APD_Voltage	Write	An 8 bit value that sets the voltage of the APD power supply.
Noise	Read	A 16 bit value representing the amount of noise detected on the return signal.

The APD Module controls the bias voltage on the APD. This voltage is created by a power supply that uses the APDP and APDN PWM output signals. The width of these signals determines the APD voltage and is set using the APD_Voltage register. Feedback from the APD is monitored by the Noise register.
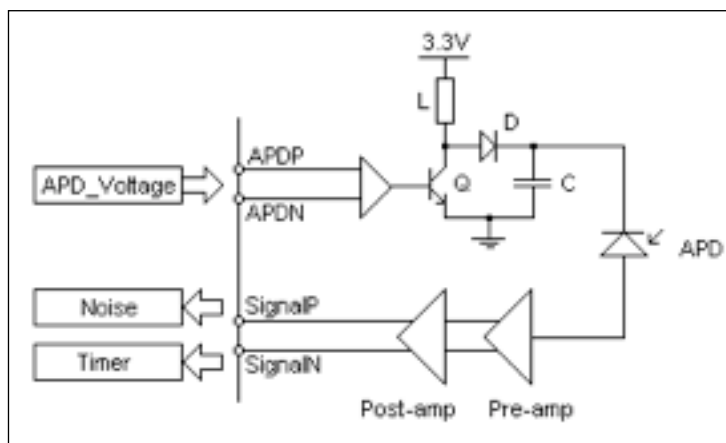
Typical APD configuration with voltage and noise control.

Management of the APD voltage to provide the maximum available gain is done by controlling the noise generated by the APD. As the voltage increases, the gain of the APD will also increase but beyond a certain point the noise suddenly begins to rise. Ideally, the APD should operate at a voltage that is just below this point, however, this optimum voltage changes with temperature and background light.

There are several different strategies that can be used to control the gain of the APD.

1. Fixed APD voltage

   The microprocessor sets the APD voltage and monitors the noise after each measurement. If the noise climbs above a certain value then the APD voltage is dropped by one count. If the noise drops below the desired value then the APD voltage is increased by one count. This simple approach leaves some residual noise mixed in with the return signal.

2. Alternating distance and noise measurements

   The microprocessor sets two APD voltages an alternates between them. The higher voltage is a few counts higher than the lower voltage. When the APD voltage is set to the higher of the two values the noise is measured but the distance readings are ignored. When the APD

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voltage is set to the lower value then the distance readings are used and the noise is ignored.

This strategy permits the noise to be controlled at a higher APD voltage where the noise characteristics are stable and repeatable. During the alternate cycle, the distance is measured at a lower APD voltage where the noise is almost zero. An Index value can be associated with each of the APD voltages so that the correct cycle is always selected.

3. Multiple APD voltages

Several different APD voltages can be used in sequence. The highest voltage is used to control the noise whilst the others are used to measure distance. For each APD voltage there will be a different gain. The lower voltages produce lower APD gain whilst the higher voltages produce higher gain. Taking distance readings at different gains can help a laser range finder to see through glass which might otherwise produce a large reflection that masks a more distant target.

5. Clock Sources

The DS00VQ100 uses two, highly stable clock sources. It is recommended that voltage controlled crystal oscillators be used with a pull range of at least 50ppm. The chip manages the frequencies of these oscillators using the control outputs VCXO_Master and VCXO_Slave.
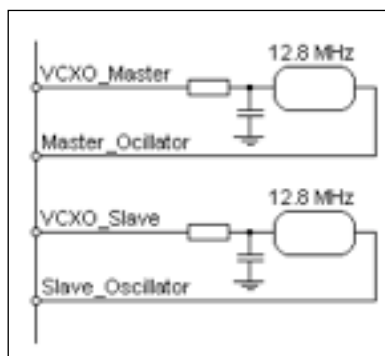
Typical clock configuration.

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6. Timer Module

Connections		
SignalP	Input	Return signal input, positive polarity. LVDS.
SignalN	Input	Return signal input, negative polarity. LVDS.
ZeroN	Input	Zero signal input. Negative polarity. 3,3V CMOS.
VCXO_Master	Output	PWM output to the master clock crystal.
VCXO_Slave	Output	PWM output to the slave clock crystal.
Internal registers		
Measuring_Range	Write	An 8 bit value that determines the maximum measuring range.
Signal_Width	Write	An 8 bit count value that determines the minimum width of a valid return signal.
Zero_Width	Write	An 8 bit count value that determines the minimum width of a valid zero signal.
Resolution_H	Write	An 16 bit value that controls the resolution [MSB's].
Resolution_L	Write	An 16 bit value that controls the resolution [LSB's].
Status	Read	An 8 bit flag register showing: index, valid signals, user input, TEX direction.
Signal_Front	Read	A 16 bit count value indicating the position of a valid front on the return signal.
Signal_Rear	Read	A 16 bit count value indicating the position of a valid rear on the return signal.
Zero_Front	Read	A 16 bit count value indicating the position of a valid front on the zero signal.
Zero_Rear	Read	A 16 bit count value indicating the position of a valid rear on the zero signal.
Span	Read	A 16 bit value indication the number of counts in the measuring range.

Measuring Units

Internal distance values are stored in counts. The Span register contains the number of counts in the entire measuring range. The positions of signal edges such as the front of the return signal are also measured in counts. The conversion of a count value to engineering units can be done as follows:

Distance [m/ft] = Range [m/ft] x Signal position [counts] / Span [counts]

The number of counts in the Span can be set using the Resolution register described later. The maximum Span is 2^{16} - 1.

Measuring Range

The maximum measuring range of the DS00VQ100 is set by the three LSB's of the Measuring_Range register and is an even, exponential multiple of the slave clock period.

Measuring_Range value	Calculation	Time @ 12.8 MHz	Range @ 12.8 MHz
xxxx x000	Slave period x 2	156.25 ns	23.4375 m
xxxx x001	Slave period x 4	312.50 ns	46.875 m
xxxx x010	Slave period x 8	625.00 ns	93.75 m
xxxx x011	Slave period x 16	1.25 us	187.50 m
xxxx x100	Slave period x 32	2.50 us	375.00 m

Permitted measuring ranges

For any given resolution, a shorter measuring range will have a higher update rate than a longer measuring range.

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Resolution Controls

The Resolution register changes the Span of the measurement and the update rate of the results. As the resolution increases, the Span increases and as the resolution increases, the update rate slows down.

Care must be taken when using very small resolutions because the results will take a long time to become available. Under these conditions use the SPI_Code value of Hex 77 to override the existing Resolution register value.

Resolution values below 255 (dec) will lead to the first valid signal being used for the result. Resolution values above 257 (dec) will produce a result using the last valid signal. The resolution at 256 (dec) is undefined.

Resolution register (typical value) Hex/Dec	Resolution [m]	Update time [s]				
		Range 000	Range 001	Range 010	Range 011	Range 100
0000 / 0	0.0600	0.0156	0.0313	0.0625	0.125	0.25
0080 / 128	0.0300	0.0313	0.0625	0.125	0.25	0.5
00C0 / 192	0.0150	0.0625	0.125	0.25	0.5	1.0
00E0 / 224	0.0075	0.125	0.25	0.5	1.0	2.0
0120 / 288	-0.0075	0.125	0.25	0.5	1.0	2.0
0140 / 320	-0.0150	0.0625	0.125	0.25	0.5	1.0
0180 / 384	-0.0300	0.0313	0.0625	0.125	0.25	0.5
01FF / 511	-0.0600	0.0156	0.0313	0.0625	0.125	0.25

The effects of the Resolution register on the update time

Resolution register (typical value) Hex/Dec	Resolution [m]	Span [counts]				
		Range 000	Range 001	Range 010	Range 011	Range 100
0000 / 0	0.0600	391	781	1563	3125	6250
0080 / 128	0.0300	781	1563	3125	6250	12500
00C0 / 192	0.0150	1563	3125	6250	12500	25000
00E0 / 224	0.0075	3125	6250	12500	25000	50000
0120 / 288	-0.0075	3125	6250	12500	25000	50000
0140 / 320	-0.0150	1563	3125	6250	12500	25000
0180 / 384	-0.0300	781	1563	3125	6250	12500
01FF / 511	-0.0600	391	781	1563	3125	6250

The effects of the Resolution register on the span

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Signal Width

The zero and return signals are filtered inside the DS00VQ100 to remove unwanted noise. However, in extremely noisy conditions this filtering will be inadequate. The Signal_Width and Zero_Width registers set a lower limit on the size of the signals that can be considered valid. These width values are in counts, the same as the Span.

Status Register

The Status register is an 8 bit flag that indicates the state of the results at the end of the last measurement made.

Status register bit	Flag	Meaning of the flag
0		This is the index value associated with the data set that was used for this measurement.
1	Index	
2		
3	Input_0	External user input flag linked to the Input_0 pin.
4	Input_1	External user input flag linked to the Input_1 pin.
5	R_Polarity	Resolution polarity: 0 = positive, 1 = negative.
6	Zero_Valid	Indicates that a zero has been detected that is wider than the Zero_Width setting.
7	Signal_Valid	Indicates that a signal has been detected that is wider than the Zero_Width setting.

Status register flags

Front and Rear Registers

The front edge and rear edge count values of the return signal and the outgoing "zero" signal are stored in separate, 16 bit registers.

[sigco explanation]

6. External Controls

Connections			Register map
Pointer_Control	Output	Control bit for a laser pointer.	External_Control [0]
Control_1	Output	User control bit.	External_Control [1]
Control_2	Output	User control bit.	External_Control [2]
Control_3	Output	User control bit.	External_Control [3]
Internal registers			
External_Control	Write	An 8 bit value that determines the state of the control outputs.	

There are four, bit addressable control outputs. They are mapped to the LSB's of the External_Control register. Bit zero is for an aiming device if available. Otherwise, all outputs can be used independently for any external control function.

7. Test Port

Connections		
Test_0	Output	
Test_1	Output	
Test_2	Output	Test signals as per table below.
Test_3	Output	
Test_4	Output	
Test_5	Output	
Internal registers		
Test_Port	Write	An 8 bit value that determines the state of the test outputs.

After reset, the default value of Test_Port is zero and the SPI signals will show on the test pins. This allows for a diagnostic analysis of the SPI bus when the chip is first powered up.

The internal signals that can be viewed on the test pins are as follows:

| Test_Port	Signal	Pin	Meaning of the signal
00	CS	Test_0	Chip select - active high.
	SPI_Clock	Test_1	SPI clock signal.
	Serial_Data_In	Test_2	Incoming SPI data.
	Serial_Data_Out	Test_3	Outgoing SPI data.
	Low	Test_4	Not used
	Low	Test_5	Not used
01	Laser_Sync	Test_0	A synchronization signal for the firing of the laser - falling edge.
	Live_Return	Test_1	The laser return signal (unfiltered) - active high.
	Live_Zero	Test_2	The outgoing laser signal (unfiltered) - active high.
	Laser_PWM	Test_3	The laser power supply PWM output - active high.
	APD_PWM	Test_4	The APD power supply PWM output - active high.
	Noise_Window	Test_5	Indicates when the noise on the signal is being analyzed - active high.

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| Test_Port	Signal	Pin	Meaning of the signal
02	TEX_Sync	Test_0	A slow synchronization signal for the firing of the laser - falling edge.
	TEX_Return_UF	Test_1	The slow laser return signal (unfiltered) - active high.
	TEX_Return	Test_2	The slow laser return signal (filtered) - active high.
	TEX_Zero_UF	Test_3	The slow speed outgoing laser signal (unfiltered) - active high.
	TEX_Zero	Test_4	The slow speed outgoing laser signal (filtered) - active high.
	Return_Valid	Test_5	Indicates when a return signal is valid - rising edge at rear of signal.

Typical signal waveforms

Test_Port = 00
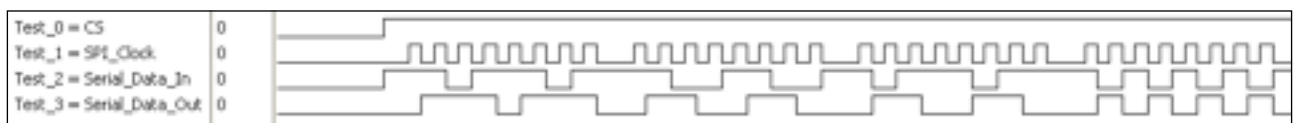
Test_Port = 01
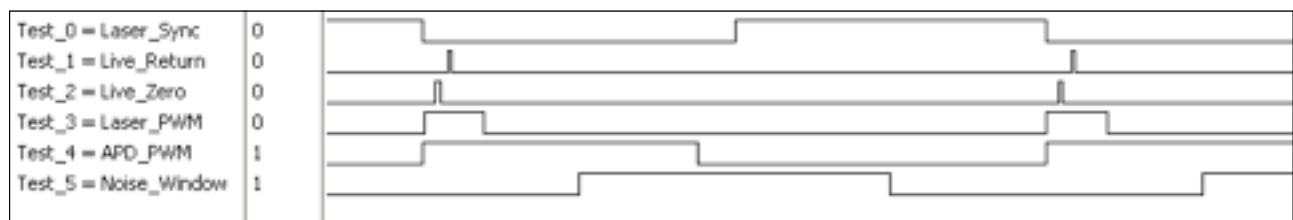
Test_Port = 02
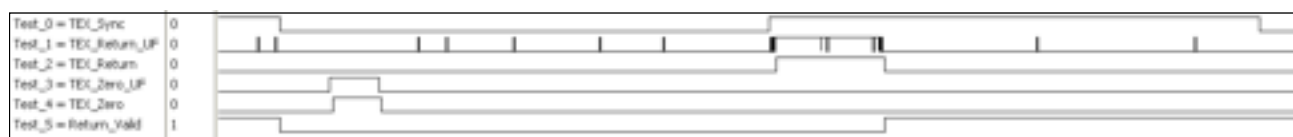
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