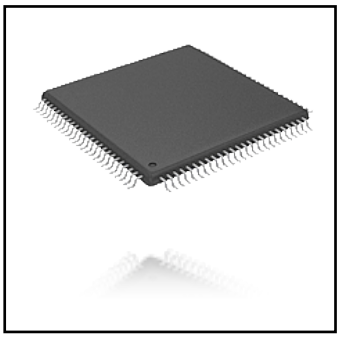
lightware
optical engineering

DS00VQ100

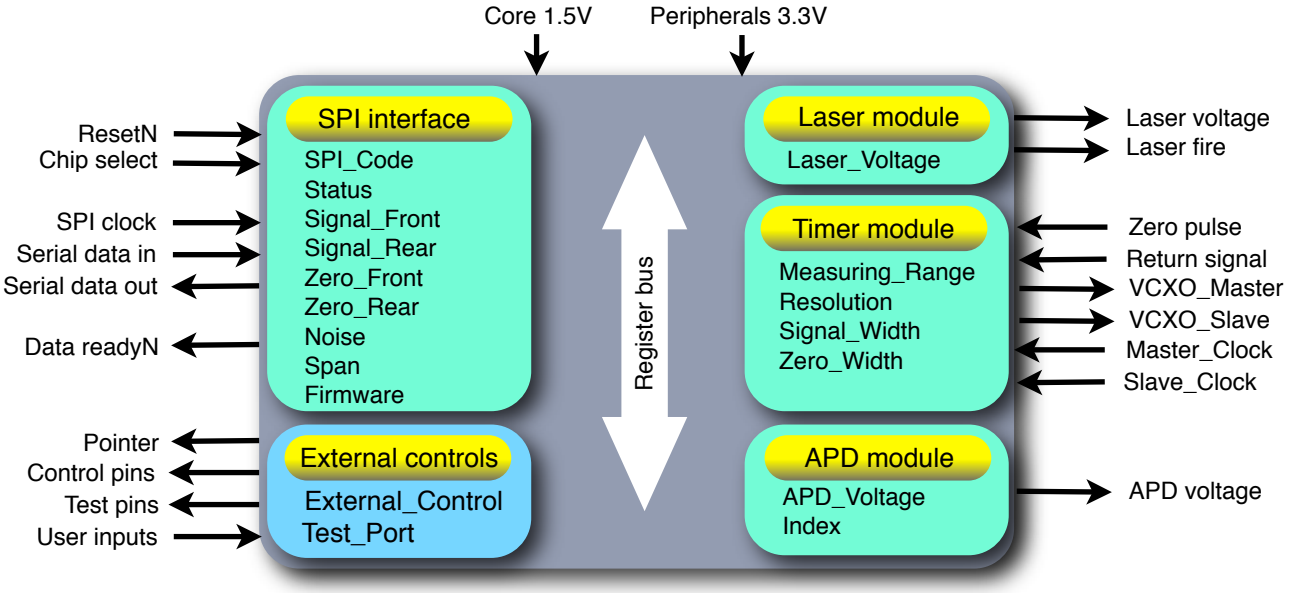
1. Introduction



The DS00VQ100 is an integrated circuit that controls a laser rangefinder. It is designed to provide all the necessary signals for a pulsed laser with an avalanche photodiode or pin diode detector. Interfacing is via a SPI bus configured in slave mode with an active high chip select. An interrupt indicates when a new result is ready.

The following subsystems are included:-

- SPI bus to a master microprocessor.
- Control system for a pulsed laser.
- Control system for an APD detector.
- Time of flight measuring system.
- General purpose control outputs.
- Diagnostics and testing ports.



Block diagram of DS00VQ100 subsystems

1.1 Advantages

- A system-on-a-chip solution to time-of-flight, laser distance measurement.
- Adjustable measuring range.
- Adjustable resolution.
- Easy to configure.
- 16 bit timing accuracy.
- Management of laser power.
- Management of APD gain and noise.
- The return signal is filtered and verified before measurement.
- Internal signals are visible on test ports.
- User inputs and outputs for auxiliary controls.

DS00VQ100

[Table of contents to be inserted here]

1.2 Specifications

Parameter	Standard units	Notes
Operating voltage	Core = 1.5 ± 0.1 VDC	At xxx mA
	I/O = 3.3 ± 0.15 VDC	At xxx mA
Operating power	A mW + B mW	Core + I/O
Package	TQFP 100	
Master clock / Slave clock	12.8 MHz	VCXO pull range ±50ppm
Minimum span	156.25 ns	Equivalent range = 23.44 m
Maximum span	2500.00 ns	Equivalent range = 375.00 m
Highest resolution	< 60 ps	Equivalent resolution < 1 cm
Lowest resolution	> 400 ps	Equivalent resolution > 6 cm
Fastest update rate	> 20 times per second	Determined by VCXO pull range
Slowest update rate	< 1 time per second	Determined by range and resolution
Temperature range	0°C to +70°C	DS00VQ100-C
	-40°C to +85°C	DS00VQ100-I
Firmware number		Hex 40, Dec 64

1.3 Summary of External Requirements

- The core and I/O power supplies should be linear regulators with minimum ripple.
- The input for the return signal is LVDS* compliant and can interface directly with a differential amplifier.
- The input for the zero signal is 3.3V CMOS compliant and the signal must be inverted.
- The voltage and fire signals to the laser are LVDS* compliant.
- The voltage signal to the APD is LVDS* compliant.
- The master and slave oscillators must be high stability, low jitter, voltage controlled, crystal oscillator modules (VCXO).

* as per ANSI/TIA/EIA-644

1.4 Signals and Pin Assignments

Signal	I/O	Type	Pin	Active	Function
NRESET	Input	3V3 CMOS 10kΩ pull up		Low	System reset on power up
CS	Input	3V3 CMOS 10kΩ pull down		High	Chip select
SPI_Clock	Input	3V3 CMOS 10kΩ pull down		Clock	Clock for SPI interface
Serial_Data_In	Input	3V3 CMOS 10kΩ pull down		Data	SPI data in
Serial_Data_Out	Output	Tri-state, 10kΩ pull down		Data	SPI data out
Data_ReadyN	Output	4mA drive, low slew rate		Low	SPI data ready
Master_Oscillator	Input	3V3 CMOS		Clock	Main system clock
Slave_Oscillator	Input	3V3 CMOS		Clock	Secondary system clock
VCXO_Master	Output	PWM		High	Master_Clock control voltage

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Signal	I/O	Type	Pin	Active	Function
VCXO_Slave	Output	PWM		Low	Slave_Clock control voltage
LaserP	Output	LVDS - PWM		High	Voltage control for laser
LaserN	Output	LVDS - PWM		Low	Voltage control for laser
FireP	Output	LVDS - PWM		High	Laser fire pulse
FireN	Output	LVDS - PWM		Low	Laser fire pulse
SignalP	Input	LVDS		High	Return signal
SignalN	Input	LVDS		Low	Return signal
ZeroN	Input	3V3 CMOS		Low	Outgoing laser signal - inverted
APDP	Output	LVDS - PWM		High	Voltage control for APD
APDN	Output	LVDS - PWM		Low	Voltage control for APD
Pointer_Control	Output	8mA drive, low slew rate		High	Pointer on/off control
Control_1	Output	8mA drive, low slew rate		User	User controllable output
Control_2	Output	8mA drive, low slew rate		User	User controllable output
Control_3	Output	8mA drive, low slew rate		User	User controllable output
Test_0	Output	4mA drive, high slew rate		Multiplex	CS, PWM_Sync, TEX_Sync
Test_1	Output	4mA drive, high slew rate		Multiplex	SPI_Clock, Live_Return, TEX_Return
Test_2	Output	4mA drive, high slew rate		Multiplex	Serial_Data_In, Live_Zero, TEX_Zero
Test_3	Output	4mA drive, high slew rate		Multiplex	Serial_Data_Out, Noise_Window, Return_Valid
Test_4	Output	4mA drive, low slew rate		User	User controllable output
Test_5	Output	4mA drive, low slew rate		User	User controllable output
Input_0	Input	3V3 CMOS 10kΩ pull down		User	User controllable input
Input_1	Input	3V3 CMOS 10kΩ pull down		User	User controllable input
Gnd		1, 9, 25, 38, 46, 51, 67, 75, 88, 99			
Vcc		17, 37, 68, 89			
VccB1		18, 66			
VccB2		39			
VccB3		18			
VccB0		87			

1.5 Power and Reset

The power supply for the core is 1.5V DC at A mA. All power connections should be routed. The I/O peripherals are powered from 3.3V DC at B mA with a separate supply being available for each bank (each side of the chip package). All I/O power pins should be connected. A common or separate 3.3 V supplies may be used.

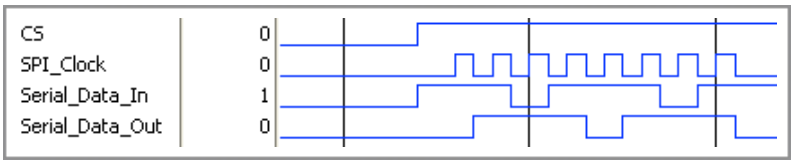
The ResetN input is an active low, master reset for the entire chip. All internal registers default to low or zero on reset. This means that the laser will be off and the APD voltage will be zero. A minimum reset width of 1us should be used.

2. SPI Interface

Connections		
CS	Input	Chip select.
SPI_Clock	Input	SPI clock driven by microprocessor.
Serial_Data_In	Input	Data from the microprocessor.
Serial_Data_Out	Output	Data to the microprocessor. This is a tristate port.
Data_ReadyN	Output	Signal to the microprocessor that new data is available for reading. Active low.
Internal registers		
SPI_Code	Write	Determines the source of the latch that saves new SPI data.
Index	Write	3 LSB's flag the data to be used next.
Status	Read	3 LSB's indicate which set of data was used last.

2.1 Read and Write Sequence

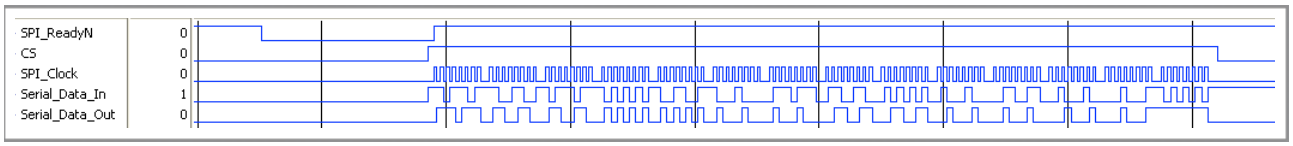
The SPI interface is used to connect the DS00VQ100 to a microprocessor. The microprocessor acts as the master whilst the DS00VQ100 has a slave configuration. A transmit/receive sequence starts when CS goes high. Data is clocked by SPI_Clock under the control of the microprocessor.



The first 8 bits of data transfer

2.2 Data Stream Format

With each transfer of data, a sequential string of 112 bits is clocked simultaneously into and out of the interface. The data transmitted by the microprocessor is formatted as 1 x 16bit + 12 x 8bit values whilst the data received is formatted as 6 x 16 bit + 2 x 8 bit values. Each value corresponds to an internal data register that connects to the various controllers inside the chip. There are different registers for transmitted and received data.



A full transfer of data initiated by the SPI_ReadyN signal

There is no addressing required for the SPI data transfer. A communication consists of a fixed length transmission with simultaneous reception. Every byte is read and written during the transfer.

"Transmit only" and "receive only" data transfers are permitted. For transmit only, ignore the received data. For receive only, transmit a string of zeros or ones. The SPI_Code will be invalid and therefore no data will be written to the internal registers.

The Data_ReadyN output goes low whenever a new reading has been completed. It can be used as an interrupt source for the controlling microprocessor. The rising edge of CS resets SPI_ReadyN. If it is not reset, SPI_ReadyN remains low until the next data transmission. Results continue to be updated even when SPI_ResetN is low. This means that the latest result will always be read from the SPI interface.

2.3 Internal Registers

Byte #	Transmit	Register	Receive	Register
0	8 bit	Unused	8 bit	Firmware
1	8 bit	Unused	16 bit	Zero_Rear [MSB]
2	8 bit	Unused		Zero_Rear [LSB]
3	8 bit	Signal_Width	16 bit	Zero_Front [MSB]
4	8 bit	APD_Voltage		Zero_Front [LSB]
5	8 bit	Laser_Voltage	16 bit	Signal_Rear [MSB]
6	8 bit	Index		Signal_Rear [LSB]
7	8 bit	Zero_Width	16 bit	Signal_Front [MSB]
8	8 bit	Test_Port		Signal_Front [LSB]
9	8 bit	Measuring_Range	16 bit	Noise [MSB]
10	16 bit	Resolution_L [LSB]		Noise [LSB]
11		Resolution_H [MSB]	16 bit	Span [MSB]
12	8 bit	External_Control		Span [LSB]
13	8 bit	SPI_Code	8 bit	Status

Transmit and receive registers

2.4 SPI_Code Register

Data transmitted by the microprocessor is stored using one of two possible latch sources. The latch source is determined by the last 8 bit value transmitted by the microprocessor, SPI_Code. If this code is set to Hex 77 (Dec 119) then the new data is written as soon as the CS line goes low at the end of the transmission. If SPI_Code is set to Hex AA (Dec 170) then the new data is written synchronously with a measuring cycle by internal control logic.

SPI_Code	SPI data latch source
Hex 77 (Dec 119)	CS falling edge - immediate write to registers
Hex AA (Dec 170)	Internal - synchronous write to registers

SPI_Code register values

2.5 SPI Index Register

Data written by the microprocessor into the SPI registers configure the DS00VQ100 for its next measuring cycle. In the same transfer, the results that are received by the microprocessor are from the measurement that has just been completed. This means that the active configuration and results are always one transfer sequence apart. If different values are used in each transmission then it is important to keep track of which configuration data is associated with which result.

The 3 LSB's of the Index register are used to tag the transmitted data string so that successive results can later be identified. The microprocessor keeps track of which results are associated with which data by reading back the the Index value in the 3 LSB's of the Status register. The example below shows how a sequence of four different data streams are identified when the results are read back.

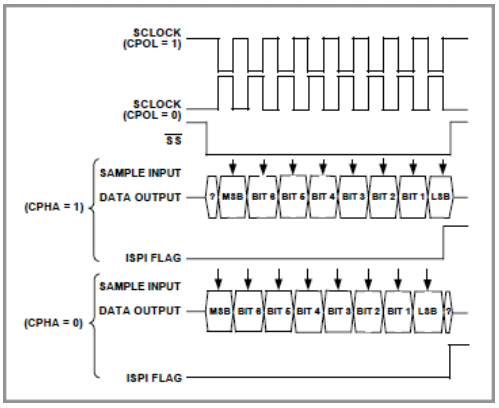
Stream	Write	Read
1	Index = 01 & Data A	Status = x4 & Result D
2	Index = 02 & Data B	Status = x1 & Result A
3	Index = 03 & Data C	Status = x2 & Result B
4	Index = 04 & Data D	Status = x3 & Result C
5	Index = 01 & Data A	Status = x4 & Result D
6	Index = 02 & Data B	Status = x1 & Result A
7	Index = 03 & Data C	Status = x2 & Result B
8	Index = 04 & Data D	Status = x3 & Result C
9	Index = 01 & Data A	Status = x4 & Result D

An example of a data sequence using the Index register

The primary use of the Index Register is to track different values of APD bias voltage that are used in successive readings. These voltages will alter the gain and noise conditions under which a reading is taken thereby allowing for on-the-fly optimization of the return signal.

2.6 ADuC842 SPI Configuration

```
SPIM=1;     // SPI master mode
CPOL=0;     // Clock idles low
CPHA=0;     // Read on rising edge clock, shift on falling
              edge clock
SPE=1;      // Enable SPI bus
```



3. Laser Module

Connections		
LaserP	Output	Positive PWM signal for laser power supply - LVDS.
LaserN	Output	Negative PWM signal for laser power supply - LVDS.
FireP	Output	Positive fire signal for laser - LVDS.
FireN	Output	Negative fire signal for laser - LVDS.
Internal registers		
Laser_Voltage	Write	An 8 bit value that sets the voltage of the laser power supply.

The Laser Module controls the operating voltage and firing signals of a high power, pulsed laser.

The laser power supply is a high efficiency, switch-mode type that directly feeds the discharge capacitor of an avalanche driver circuit. There is no DC output. Instead, voltage pulses are generated shortly before the firing of the laser. The LaserP and LaserN voltage control signals are LVDS compatible and are designed to drive a switching transistor through a comparator.

The fire signals are also LVDS and are designed to drive an avalanche transistor or avalanche FET through a high speed comparator. The laser is fired at the Master_Clock frequency divided by 512. For 12.8 MHz crystal this gives a 25 kHz firing rate.

The laser power supply controls are in the form of synchronous, PWM signals. These signals are timed to be active when the laser firing pulse is active. This prevents the avalanche firing transistor from “pumping” the power supply and getting hot.

The laser voltage is set by the Laser_Voltage register that is an 8 bit value representing the “on” time of the PWM. If this value is less than 16 (dec) then the power supply is off and the laser is not fired.

4. APD Module

Connections		
APDP	Output	Positive PWM signal for APD power supply. LVDS.
APDP	Output	Negative PWM signal for APD power supply. LVDS.
Internal registers		
APD_Voltage	Write	An 8 bit value that sets the voltage of the APD power supply.
Noise	Read	A 16 bit value representing the amount of noise detected on the return signal.

The APD Module controls the bias voltage on the APD. This voltage is created by a power supply that uses the APDP and APDN PWM output signal. The width of the PWM is set using the APD_Voltage register.

Feedback from the APD is contained in the Noise Register. The voltage of the APD is adjusted to manage the noise at the desired value depending upon the gain required. Using the Index register, the noise and gain characteristics of the APD can be cycled in successive data transfers to provide tailored responses to environmental conditions and return signal strength.

5. Timer Module

Connections		
SignalP	Input	Return signal input, positive polarity. LVDS.
SignalN	Input	Return signal input, negative polarity. LVDS.
ZeroN	Input	Zero signal input. Negative polarity. 3,3V CMOS.
VCXO_Master	Output	PWM output to the master clock crystal.
VCXO_Slave	Output	PWM output to the slave clock crystal.
Internal registers		
Measuring_Range	Write	An 8 bit value that determines the maximum measuring range.
Signal_Width	Write	An 8 bit value that determines the minimum width of a valid return signal.
Zero_Width	Write	An 8 bit value that determines the minimum width of a valid zero signal.
Resolution_H	Write	An 16 bit value that controls the resolution [MSB's].
Resolution_L	Write	An 16 bit value that controls the resolution [LSB's].
Status	Read	An 8 bit flag register showing: index, valid signals, user input, TEX direction.
Signal_Front	Read	A 16 bit count value indicating the position of a valid front on the return signal.
Signal_Rear	Read	A 16 bit count value indicating the position of a valid rear on the return signal.
Zero_Front	Read	A 16 bit count value indicating the position of a valid front on the zero signal.
Zero_Rear	Read	A 16 bit count value indicating the position of a valid rear on the zero signal.
Span	Read	A 16 bit count value indication the number of counts in the measuring range.
Noise	Read	A 16 bit count value indicating how much noise was detected on the return signal.

5.1 Measuring Range

The maximum measuring range of the DS00VQ100 is set by the three LSB's of the Measuring _Range register and is an even, exponential multiple of the slave clock period.

Measuring_Range value	Calculation	Time @ 12.8 MHz	Range @ 12.8 MHz
xxxx x000	Slave period x 2	156.25 ns	23.4375 m
xxxx x001	Slave period x 4	312.50 ns	46.875 m
xxxx x010	Slave period x 8	625.00 ns	93.75 m
xxxx x011	Slave period x 16	1.25 us	187.50 m
xxxx x100	Slave period x 32	2.50 us	375.00 m

Permitted measuring ranges

5.2 Signal Width

The zero and return signals are filtered inside the DS00VQ100 to remove unwanted noise. However, in extremely noise conditions this filtering will be inadequate. The Signal_Width and Zero_Width registers set a lower limit on the size of the signals that can be considered valid. The values are in the same units as the Span.

5.3 Resolution Controls

The Resolution Register changes the Span of the measurement and therefore the ultimate resolution of the signals. As the resolution increases the update rate slows down. Care must be taken when using very small resolutions (large Span) because the results will take a long time to become available. At infinite resolution the internal circuitry becomes “frozen” and will not respond to commands. Under these conditions use the SPI_Code value of Hex 77 to override the existing Resolution Register value. There will no damage to the chip or any external components. Resolution values below 256 (dec) will lead to the first valid signal being used for the result. Resolution values above 256 (dec) will produce a result using the last valid signal.

Resolution register (typical value) Hex/Dec	Resolution [m]	Update time [s]			
		Range 00	Range 01	Range 10	Range 11
0000 / 0	0.0600	0.0156	0.0313	0.0625	0.1250
0080 / 128	0.0300	0.0313	0.0625	0.1250	0.2500
00C0 / 192	0.0150	0.0625	0.1250	0.2500	0.500
00E0 / 224	0.0075	0.1250	0.2500	0.500	1.000
0100 / 256	0.0000	∞	∞	∞	∞
0120 / 288	-0.0075	0.1250	0.2500	0.500	1.000
0140 / 320	-0.0150	0.0625	0.1250	0.2500	0.500
0180 / 384	-0.0300	0.0313	0.0625	0.1250	0.2500
01FF / 511	-0.0600	0.0156	0.0313	0.0625	0.1250

The effects of the Resolution Register on resolution and update rate

[Table needs updating to include:- Range option 100; show Span number also]

5.4 Status Register

The Status Register is an 8 bit flag that indicates the state of the results at the end of the last measurement made.

Status_Register bit	Flag	Meaning of the flag
0	Index	This is the index value associated with the data set that was used for this measurement.
1		
2		
3	Input_0	External user input flag linked to the Input_0 pin.
4	Input_1	External user input flag linked to the Input_1 pin.
5	R_Polarity	Resolution polarity: 0 = positive, 1 = negative.
6	Zero_Valid	Indicates that a zero has been detected that is wider than the Zero_Width setting.
7	Signal_Valid	Indicates that a signal has been detected that is wider than the Zero_Width setting.

Status register flags

6. External Controls

Connections			Register map
Pointer_Control	Output	Control bit for a laser pointer.	External_Control [0]
Control_1	Output	User control bit.	External_Control [1]
Control_2	Output	User control bit.	External_Control [2]
Control_3	Output	User control bit.	External_Control [3]
Internal registers			
External_Control	Write	An 8 bit value that determines the state of the control outputs.	

There are four, bit addressable control outputs. They are mapped to the LSB's of the External_Control register. Bit zero is for an aiming device if available. Otherwise, all outputs can be used independently for any external control function.

7. Test Port

Connections			Register map
Test_0	Output	CS, PWM_Sync, TEX_Sync.	
Test_1	Output	SPI_Clock, Live_Return, TEX_Return.	
Test_2	Output	Serial_Data_In, Live_Zero, TEX_Zero.	
Test_3	Output	Serial_Data_Out, Noise_Window, Return_Valid.	
Test_4	Output	User test bit.	Test_Port [2]
Test_5	Output	User test bit.	Test_Port [3]
Internal registers			
Test_Port	Write	An 8 bit value that determines the state of the test outputs.	

The value of bit 0 and bit 1 of Test_Port register determine the configuration of the Test Port. The value of bit 2 is reflected on Test_4 and the value of bit 3 is reflected on Test_5 as shown in the table below:-

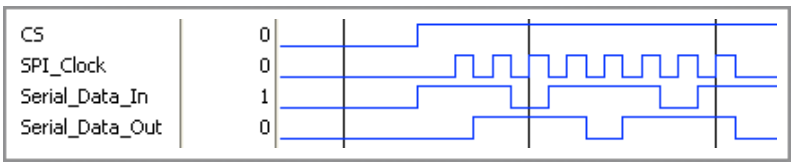
Test_Port value	Test_0	Test_1	Test_2	Test_3	Test_4	Test_5
xxxx xx00	CS	SPI_Clock	Serial_Data_In	Serial_Data_Out	x	x
xxxx xx01	PWM_Sync	Live_Return	Live_Zero	Noise_Window	x	x
xxxx xx10	TEX_Sync	TEX_Return	TEX_Zero	Return_Valid	x	x
xxxx 00xx	x	x	x	x	0	0
xxxx 01xx	x	x	x	x	0	1
xxxx 10xx	x	x	x	x	1	0

Test Port outputs

7.1 Typical signals

Test_Port = xxxx xx00

Test_0
Test_1
Test_2
Test_3



Test_Port = xxxx xx01

[Live signals to be inserted here]

Test_Port = xxxx xx10

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[Timing diagrams]
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