Thoughts on fast gate drive

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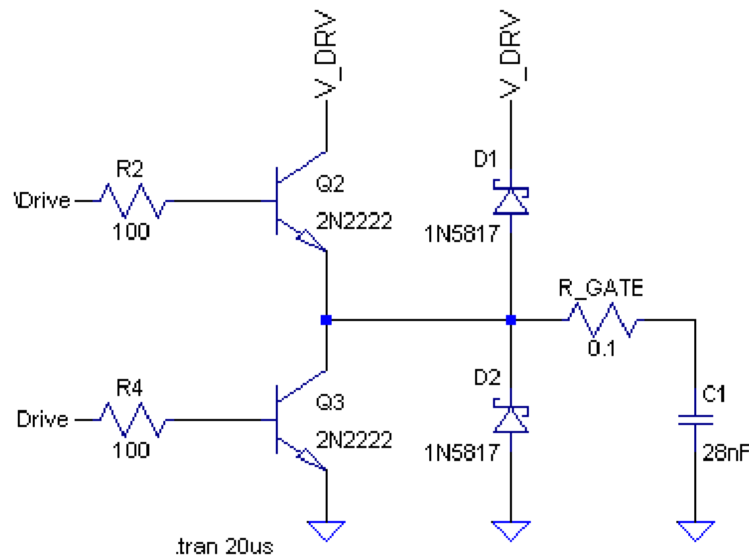
Purpose

- Propose circuit architecture capable to driving a ~28nF MOSFET gate at 500kHz
- Perform ROM calculations of losses

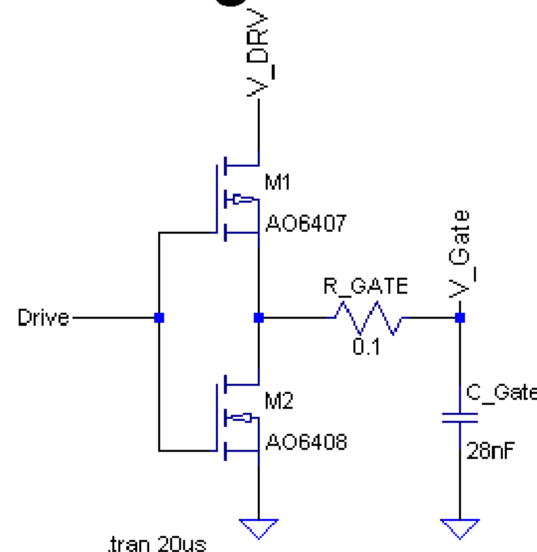
Option 1: Bipolar transistor drive

- Schottkys are needed to provide current path for inevitable ring between gate capacitance and parasitic inductance
- Turnoff speed uninspiring; requires bipolar drive



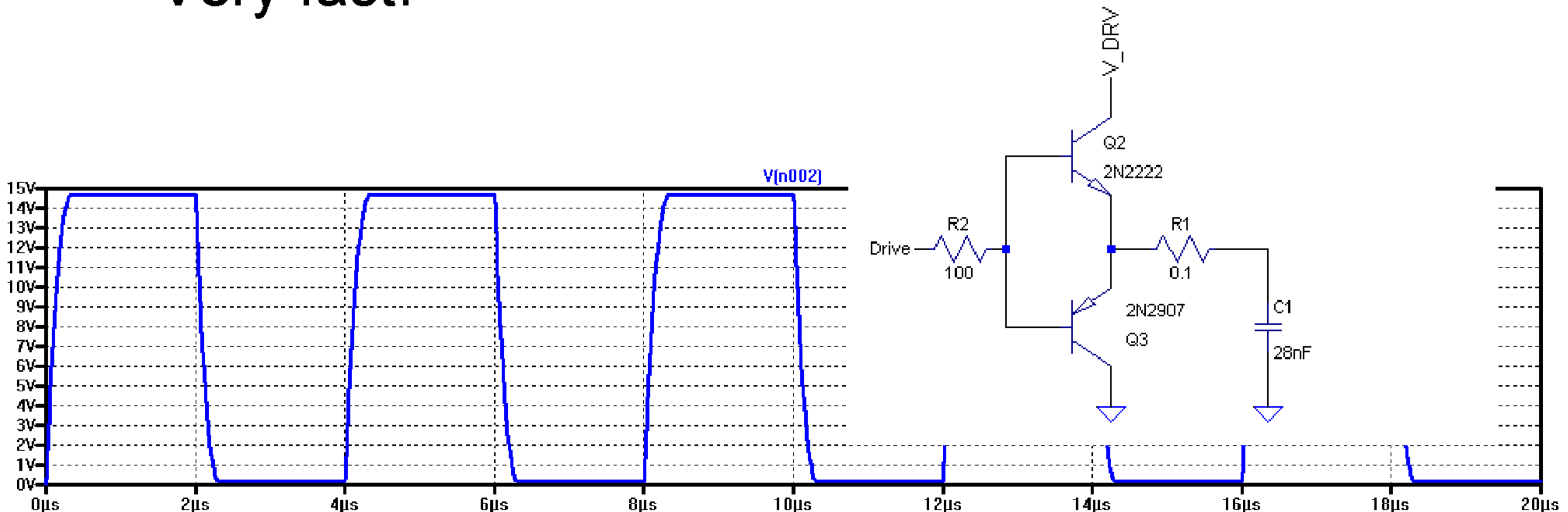
Option 2: MOSFET Totem Pole

- Very fast switching circuit
- Fundamentally flawed: shoot-through current during period when both FETs are in conduction
- Can be mitigated through timing circuitry, but this adds complexity to design



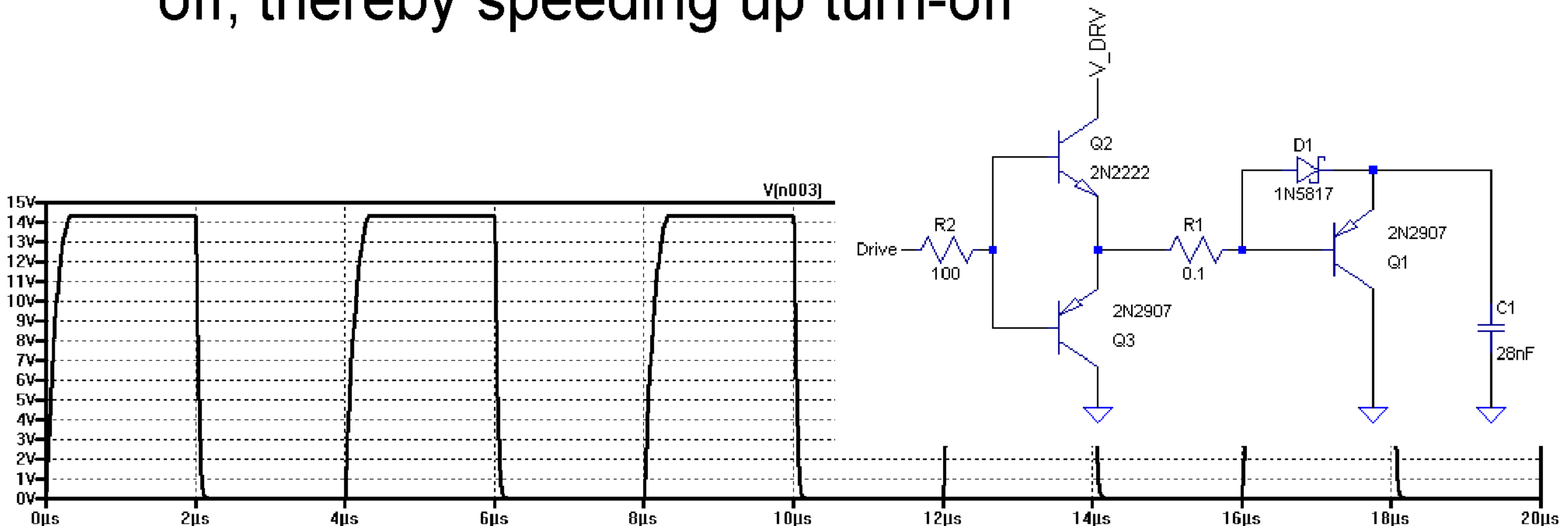
Option 3: Bipolar totem pole

- Avoids shoot-through problem of FET totem pole
- The two B-E junctions protect each other from reverse breakdown; does not require any Schottky diodes for reverse current protection
- Very fast!

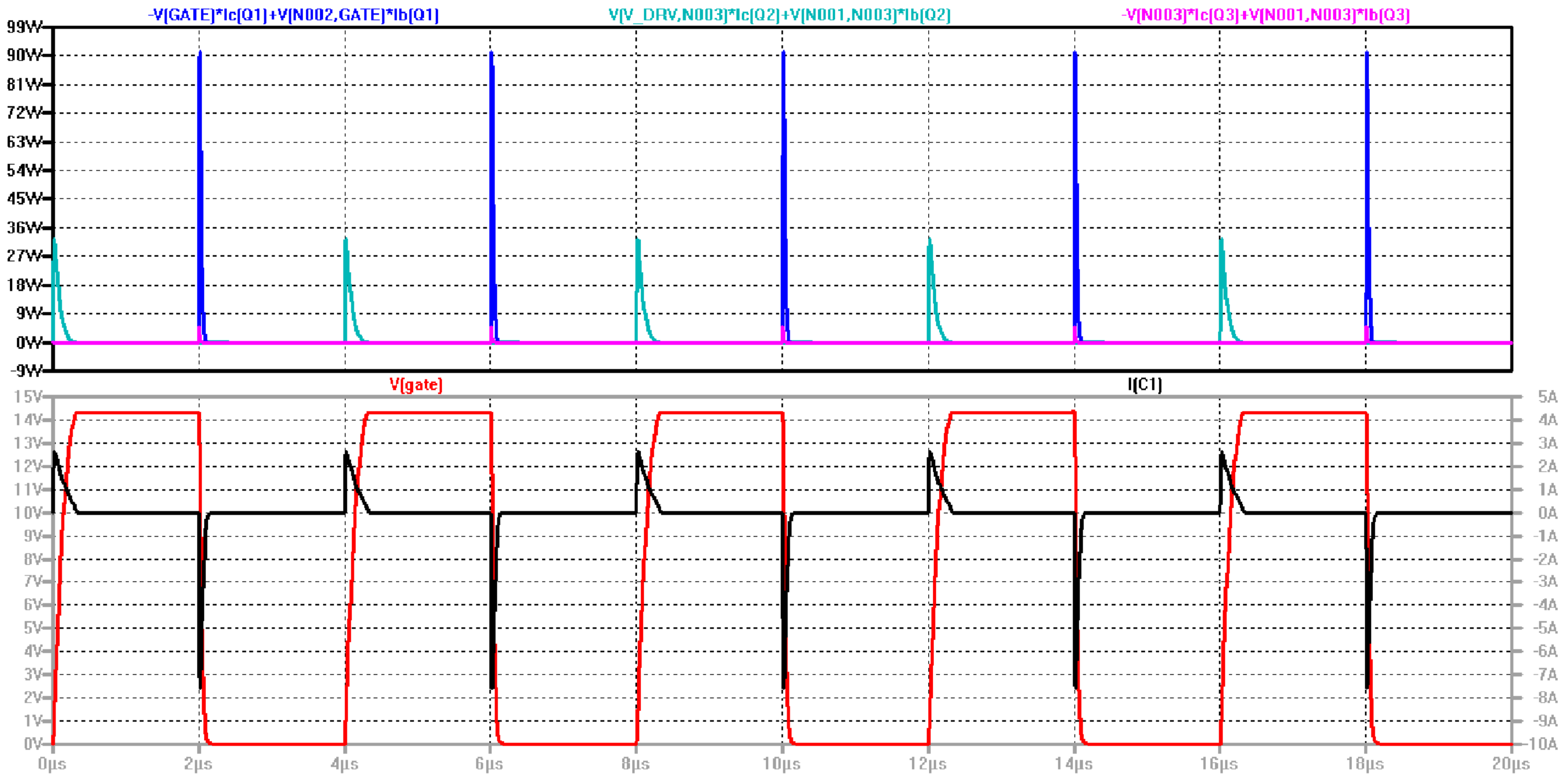


Option 3A: Bipolar totem w/ speedup

- Add a turn-off speed-up subcircuit
- Schottky provides current path to charge gate, and protects Q1 from B-E breakdown
- Q1 provides shunt for gate capacitance at turn-off; thereby speeding up turn-off



Option 3A (totem + speedup)



Option 3A (totem + speedup)

- Observations:
  - Maximum stress is on Q1 (turn-off transistor)
    - Peak power dissipation ~90W; average ~700mW
    - Peak current ~8A; RMS ~720mA
  - Stress on Q2 (NPN, top of totem pole)
    - Peak power dissipation ~33W; average ~700mW
    - Peak current ~2.5A; RMS ~400mA
  - Stress on Q3 (PNP, bottom of totem pole)
    - Peak power dissipation ~5W; average ~15mW
    - Peak current 650mA; RMS ~58mA

Option 3A (totem + speedup)

- Observations:
  - Rise time: ~320ns
  - Fall time: ~40ns
- Peak drive current ~3A

Power FET + Parasitics

- Microsemi APTM20DAM04G module
- Switching 100V @ 200A, purely resistive
- Assumed junction temperature of 125DegC
- 50% duty cycle, 500kHz switching frequency

Data sheet values			
C_ISS	28900	pF	Input capacitance
C_OSS	9320	pF	Output capacitance
C_RSS	580	pF	Reverse transfer capacitance
g_f	86	I/A	Forward transconductance
V_DS_spec	25	V	Voltage at which C_RSS is specified
R_G,I	2.1	Ohm	Internal gate mesh resistance
VT	5	V	Spec sheet threshold
Q_G	5.60E-07	C	Gate charge

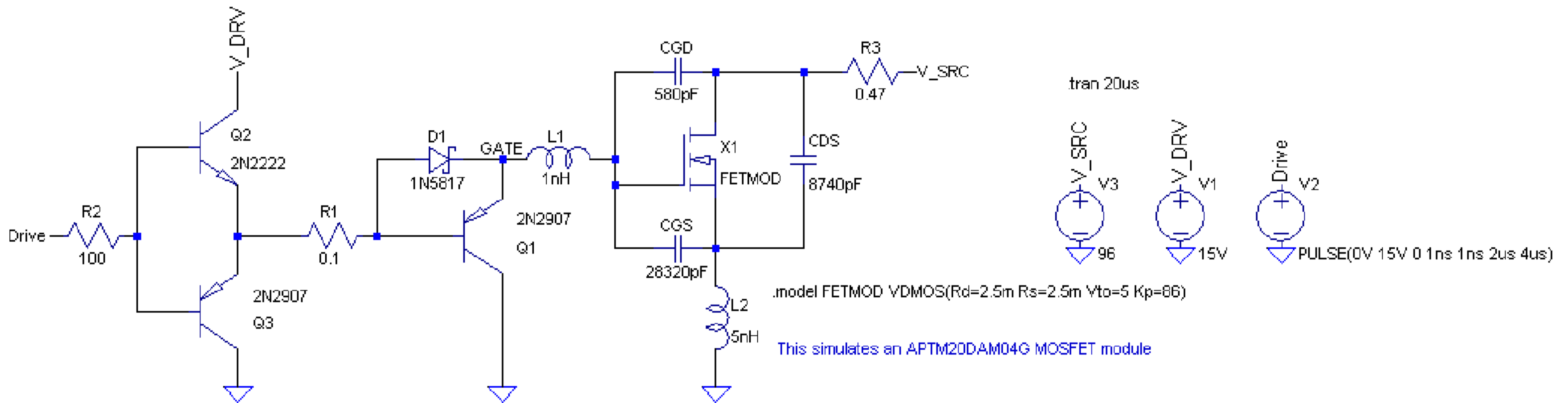
Circuit conditions			
V_DS_off	100	V	Voltage standoff of FET
Temp Rise	100	K	Temperature rise above ambient
Drain current	200	A	Expected drain current, fully saturated
R_Low	0.1	Ohm	Internal impedance of gate driver, low side
R_High	0.1	Ohm	Internal impedance of gate driver, high side
R_Gate	0.1	Ohm	Series resistance between gate driver and gate
F_Drv	500000	Hz	Switching frequency
V_Drv	15	V	Gate drive voltage
L_Source	5	nH	Parasitic source inductance

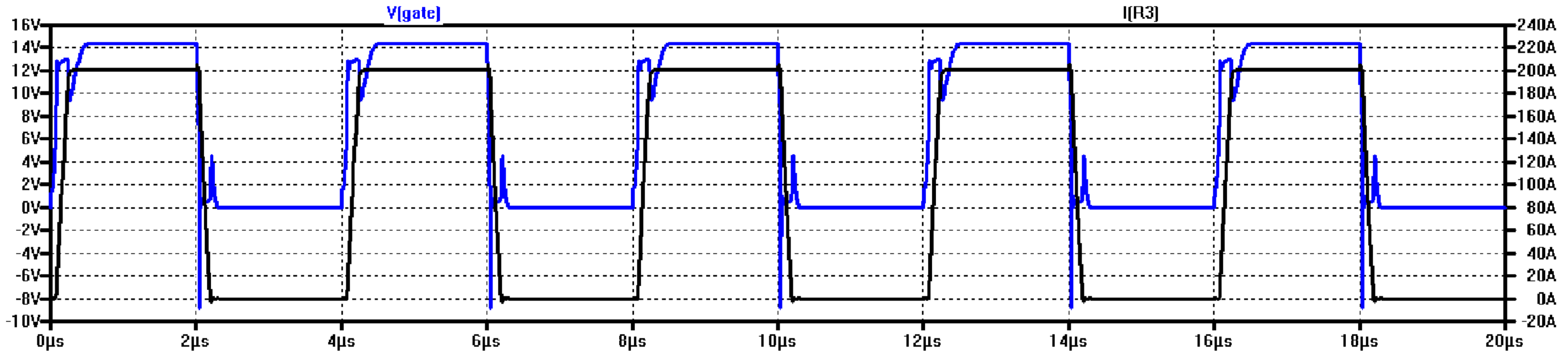
Power FET + Parasitics

- Rule-of-thumb worksheet results
  - Negative R_G optimum means zero added gate resistance is required
  - Parasitic capacitances and temperature-derated thresholds computed
  - WARNING: Switching loss is purely linear region loss, NOT Rds..

Model outputs			
C_GD_AVG	580	pF	Average-case gate / drain capacitance
C_OSS_AVG	9320	pF	Average-case OSS parasitic capacitance
C_GD	580	pF	Gate / drain capacitance
C_GS	28320	pF	Gate / source capacitance
C_DS	8740	pF	Drain / source capacitance
VT_Derated	4.3	V	Turn-on threshold, adjusted for temperature
V_GS,Miller	6.625581395	V	Miller plateau level (gate drive at departure from linear)
P_Gate	4.20E+00	W	Gate charge losses
I_Gate_Avg	2.80E-01	A	Average gate drive current
P_Drv_On	9.13E-02	W	Power dissipation in gate driver, turn on
P_Drv_Off	9.13E-02	W	Power dissipation in gate driver, turn off
P_Drv_Total	1.83E-01	W	Power dissipation in gate driver, total
I_G2	4.1466	A	Drive gate current during interval when Vgs rises from Vt to Miller Plateau
I_G3	3.6411	A	Drive gate current during Miller Plateau region
t_2	1.62E-08	s	Switching time in region 2
t_3	1.59E-08	s	Switching time in region 3
P_SW	1.61E+02	W	Estimate of switching losses in FET
R_G_Optimum	0.00	Ohm	Optimum value of gate resistance to minimize gate drive ringing

Power FET + Parasitics





Power FET + Parasitics

- Average load dissipation: 9kW
- Average MOSFET dissipation: 400W
- Average Q1 dissipation: 580mW
- Average Q2 dissipation: 660mW
- Average Q3 dissipation: 14mW

- Turn-on time: 250ns
- Turn-off time: 210ns

- Drive current into totem pole: 150mAp-p @ 15V

RECOMMENDATION

- The bipolar totem pole with speedup transistor seems to have a lot of promise
- The specific bipolar transistors used in the totem pole need to be optimized
- NOTE: Given the current levels and power dissipation of the NPN and PNP drive transistors, DPAK or TO-220 packages will be needed. Everything must be as close to the MOSFET gate/source terminals as possible, with an absolute minimum possible inductance. Highly effective decoupling capacitors will be needed for drive.