Sitronix

# ST7687S

## 65K 128x128 Color Dot Matrix LCD Controller/Driver

## 1. INTRODUCTION

The ST7687S is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 384 Segment and 128 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

## 2. FEATURES

### Driver Output Circuits

- 384 segment outputs / 128 common outputs

### Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

### Gray-Scale Display

- 4FRC & 31 PWM function circuit to display 64 gray-scale display
- Support 8 color mode (Idle mode)

### On-chip Display Data RAM

- Capacity: 128 x 128 x 16 =262,144 bits

### Color support by Interface

- 4k colors (RGB)=(444) mode
- 65K colors (RGB)=(565) mode

### Microprocessor Interface

- 8 bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line serial interface
- 3-line (9-bits) serial interface

### On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x2~x8) with internal capacitors.
- Extremely Few Outsider Components.
- On-chip Voltage Regulator
- On-chip electronic contrast control function
- Voltage follower (LCD bias: 1/6~1/12)

### Operating Voltage Range

- Supply Digital Voltage (VDD): 1.65 to 3.3V
- Supply Analog Voltage (VDD2~VDD5): 2.4 to 3.3V
- LCD driving voltage (VOP = V0 - VSS): Max: 18V

### LCD Driving Voltage

- Contrast Adjustment Value is stored in the Built-In EEPROM for better display quality.

### LCD Driving setting suggestion

- VOP = 14V, BIAS=1/9. (VDD=2.8V)

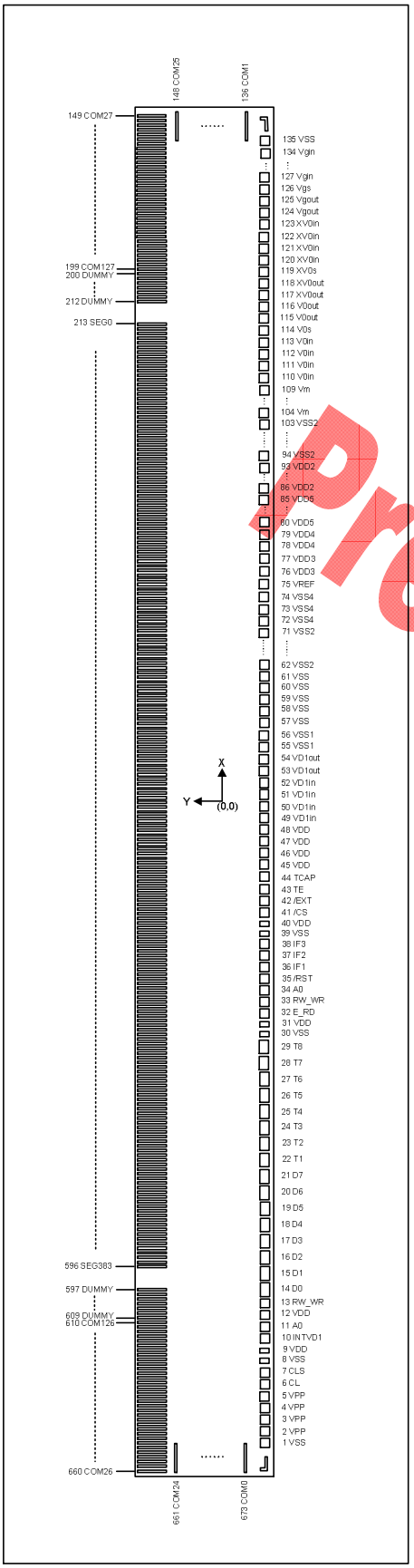
### Package Type

- Application for COG



| ST7687S | 6800, 8080, 4-Line, 3-Line interface | ST |
|---|---|---|

# 3. ST7687S Pad Arrangement (COG)






**Chip Size :**

**11586 um x 686 um**

**Bump Pitch :**

PAD 136~148, 149~212, 213~596, 597~660 661~673 pitch=22um (min, com/seg)

PAD 212~213, 596~597 pitch=110.88um ( com/seg)

PAD 1~7, 10~13, 32~38, 41~57, 59~135 pitch=80um (I/O)

PAD 14~29, pitch=120um(I/O)

PAD 8~9, 30~31, 39~40, pitch=49um(I/O)

PAD 7~8, 9~10, 31~32, 38~39, 40~41, pitch=64.5um(I/O)

PAD 57~58, 58~59=75.5um(I/O)

PAD 13~14, pitch=100um(I/O)

PAD 29~30, pitch=84.5um(I/O)

**Bump Size :**

PAD 136~673

Bump width=12um (min, com/seg)

Bump space=10um (min, com/seg)

Bump length=166.7um(min, com/seg)

Bump area=2000.4um^2(com/seg)

PAD 14~29

Bump width=105um(I/O)

Bump space=15um(I/O)

Bump length=59um(I/O)

Bump area=6195um^2

PAD 58

Bump width=56um(I/O)

Bump space=15um(I/O)

Bump length=59um(I/O)

Bump area=3304um^2

PAD 8~9, 30~31, 39~40

Bump width=34um(I/O)

Bump space=15um(I/O)

Bump length=59um(I/O)

Bump area=2006um^2

PAD 1~7, 10~13, 32~38, 41~57, 59~135

Bump width=65um(I/O)

Bump space=15um(I/O)

Bump length=59um(I/O)

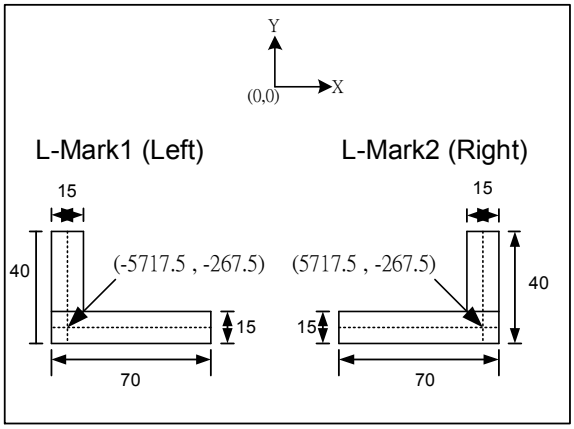
Bump area=3185um^2

**Bump Height : 15 um**

**Chip Thickness: 300 um**

**Alignment mark**

The center of alignment mark: see bellow Table



## 4. Pad Center Coordinates

| PAD | NAME | X | Y |
|---|---|---|---|
| 1 | **VSS** | -5582.5 | -257.5 |
| 2 | **VPP** | -5502.5 | -257.5 |
| 3 | **VPP** | -5422.5 | -257.5 |
| 4 | **VPP** | -5342.5 | -257.5 |
| 5 | **VPP** | -5262.5 | -257.5 |
| 6 | **CL** | -5182.5 | -257.5 |
| 7 | **CLS** | -5102.5 | -257.5 |
| 8 | **VSS** | -5038 | -257.5 |
| 9 | **VDD** | -4989 | -257.5 |
| 10 | **INTVD1** | -4924.5 | -257.5 |
| 11 | **A0** | -4844.5 | -257.5 |
| 12 | **VDD** | -4764.5 | -257.5 |
| 13 | **RW_WR** | -4684.5 | -257.5 |
| 14 | **D0** | -4584.5 | -257.5 |
| 15 | **D1** | -4464.5 | -257.5 |
| 16 | **D2** | -4344.5 | -257.5 |
| 17 | **D3** | -4224.5 | -257.5 |
| 18 | **D4** | -4104.5 | -257.5 |
| 19 | **D5** | -3984.5 | -257.5 |
| 20 | **D6** | -3864.5 | -257.5 |
| 21 | **D7** | -3744.5 | -257.5 |
| 22 | **T1** | -3624.5 | -257.5 |
| 23 | **T2** | -3504.5 | -257.5 |
| 24 | **T3** | -3384.5 | -257.5 |
| 25 | **T4** | -3264.5 | -257.5 |
| 26 | **T5** | -3144.5 | -257.5 |
| 27 | **T6** | -3024.5 | -257.5 |
| 28 | **T7** | -2904.5 | -257.5 |
| 29 | **T8** | -2784.5 | -257.5 |
| 30 | **VSS** | -2700 | -257.5 |
| 31 | **VDD** | -2651 | -257.5 |
| 32 | **E_RD** | -2586.5 | -257.5 |
| 33 | **RW_WR** | -2506.5 | -257.5 |
| 34 | **A0** | -2426.5 | -257.5 |
| 35 | **/RST** | -2346.5 | -257.5 |
| 36 | **IF1** | -2266.5 | -257.5 |
| 37 | **IF2** | -2186.5 | -257.5 |
| 38 | **IF3** | -2106.5 | -257.5 |
| 39 | **VSS** | -2042 | -257.5 |
| 40 | **VDD** | -1993 | -257.5 |
| 41 | **/CS** | -1928.5 | -257.5 |
| 42 | **/EXT** | -1848.5 | -257.5 |
| 43 | **TE** | -1768.5 | -257.5 |
| 44 | **TCAP** | -1688.5 | -257.5 |
| 45 | **VDD** | -1608.5 | -257.5 |
| 46 | **VDD** | -1528.5 | -257.5 |
| 47 | **VDD** | -1448.5 | -257.5 |
| 48 | **VDD** | -1368.5 | -257.5 |
| 49 | **VD1in** | -1288.5 | -257.5 |
| 50 | **VD1in** | -1208.5 | -257.5 |
| 51 | **VD1in** | -1128.5 | -257.5 |
| 52 | **VD1in** | -1048.5 | -257.5 |
| 53 | **VD1out** | -968.5 | -257.5 |
| 54 | **VD1out** | -888.5 | -257.5 |
| 55 | **VSS1** | -808.5 | -257.5 |
| 56 | **VSS1** | -728.5 | -257.5 |
| 57 | **VSS** | -648.5 | -257.5 |
| 58 | **VSS** | -573 | -257.5 |
| 59 | **VSS** | -497.5 | -257.5 |
| 60 | **VSS** | -417.5 | -257.5 |
| 61 | **VSS** | -337.5 | -257.5 |
| 62 | **VSS2** | -257.5 | -257.5 |
| 63 | **VSS2** | -177.5 | -257.5 |
| 64 | **VSS2** | -97.5 | -257.5 |
| 65 | **VSS2** | -17.5 | -257.5 |
| 66 | **VSS2** | 62.5 | -257.5 |
| 67 | **VSS2** | 142.5 | -257.5 |
| 68 | **VSS2** | 222.5 | -257.5 |
| 69 | **VSS2** | 302.5 | -257.5 |
| 70 | **VSS2** | 382.5 | -257.5 |
| 71 | **VSS2** | 462.5 | -257.5 |
| 72 | **VSS4** | 542.5 | -257.5 |

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|---|---|---|---|
| 73 | VSS4 | 622.5 | -257.5 |
| 74 | VSS4 | 702.5 | -257.5 |
| 75 | VREF | 782.5 | -257.5 |
| 76 | VDD3 | 862.5 | -257.5 |
| 77 | VDD3 | 942.5 | -257.5 |
| 78 | VDD4 | 1022.5 | -257.5 |
| 79 | VDD4 | 1102.5 | -257.5 |
| 80 | VDD5 | 1182.5 | -257.5 |
| 81 | VDD5 | 1262.5 | -257.5 |
| 82 | VDD5 | 1342.5 | -257.5 |
| 83 | VDD5 | 1422.5 | -257.5 |
| 84 | VDD5 | 1502.5 | -257.5 |
| 85 | VDD5 | 1582.5 | -257.5 |
| 86 | VDD2 | 1662.5 | -257.5 |
| 87 | VDD2 | 1742.5 | -257.5 |
| 88 | VDD2 | 1822.5 | -257.5 |
| 89 | VDD2 | 1902.5 | -257.5 |
| 90 | VDD2 | 1982.5 | -257.5 |
| 91 | VDD2 | 2062.5 | -257.5 |
| 92 | VDD2 | 2142.5 | -257.5 |
| 93 | VDD2 | 2222.5 | -257.5 |
| 94 | VSS2 | 2302.5 | -257.5 |
| 95 | VSS2 | 2382.5 | -257.5 |
| 96 | VSS2 | 2462.5 | -257.5 |
| 97 | VSS2 | 2542.5 | -257.5 |
| 98 | VSS2 | 2622.5 | -257.5 |
| 99 | VSS2 | 2702.5 | -257.5 |
| 100 | VSS2 | 2782.5 | -257.5 |
| 101 | VSS2 | 2862.5 | -257.5 |
| 102 | VSS2 | 2942.5 | -257.5 |
| 103 | VSS2 | 3022.5 | -257.5 |
| 104 | Vm | 3102.5 | -257.5 |
| 105 | Vm | 3182.5 | -257.5 |
| 106 | Vm | 3262.5 | -257.5 |
| 107 | Vm | 3342.5 | -257.5 |
| 108 | Vm | 3422.5 | -257.5 |
| 109 | Vm | 3502.5 | -257.5 |

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|---|---|---|---|
| 110 | V0in | 3582.5 | -257.5 |
| 111 | V0in | 3662.5 | -257.5 |
| 112 | V0in | 3742.5 | -257.5 |
| 113 | V0in | 3822.5 | -257.5 |
| 114 | V0s | 3902.5 | -257.5 |
| 115 | V0out | 3982.5 | -257.5 |
| 116 | V0out | 4062.5 | -257.5 |
| 117 | XV0out | 4142.5 | -257.5 |
| 118 | XV0out | 4222.5 | -257.5 |
| 119 | XV0s | 4302.5 | -257.5 |
| 120 | XV0in | 4382.5 | -257.5 |
| 121 | XV0in | 4462.5 | -257.5 |
| 122 | XV0in | 4542.5 | -257.5 |
| 123 | XV0in | 4622.5 | -257.5 |
| 124 | Vgout | 4702.5 | -257.5 |
| 125 | Vgout | 4782.5 | -257.5 |
| 126 | Vgs | 4862.5 | -257.5 |
| 127 | Vgin | 4942.5 | -257.5 |
| 128 | Vgin | 5022.5 | -257.5 |
| 129 | Vgin | 5102.5 | -257.5 |
| 130 | Vgin | 5182.5 | -257.5 |
| 131 | Vgin | 5262.5 | -257.5 |
| 132 | Vgin | 5342.5 | -257.5 |
| 133 | Vgin | 5422.5 | -257.5 |
| 134 | Vgin | 5502.5 | -257.5 |
| 135 | VSS | 5582.5 | -257.5 |
| 136 | COM1 | 5642.23 | -189.26 |
| 137 | COM3 | 5642.23 | -167.26 |
| 138 | COM5 | 5642.23 | -145.26 |
| 139 | COM7 | 5642.23 | -123.26 |
| 140 | COM9 | 5642.23 | -101.26 |
| 141 | COM11 | 5642.23 | -79.26 |
| 142 | COM13 | 5642.23 | -57.26 |
| 143 | COM15 | 5642.23 | -35.26 |
| 144 | COM17 | 5642.23 | -13.26 |
| 145 | COM19 | 5642.23 | 8.74 |
| 146 | COM21 | 5642.23 | 30.74 |

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|---|---|---|---|
| 147 | **COM23** | 5642.23 | 52.74 |
| 148 | **COM25** | 5642.23 | 74.74 |
| 149 | **COM27** | 5709.88 | 203.83 |
| 150 | **COM29** | 5687.88 | 203.83 |
| 151 | **COM31** | 5665.88 | 203.83 |
| 152 | **COM33** | 5643.88 | 203.83 |
| 153 | **COM35** | 5621.88 | 203.83 |
| 154 | **COM37** | 5599.88 | 203.83 |
| 155 | **COM39** | 5577.88 | 203.83 |
| 156 | **COM41** | 5555.88 | 203.83 |
| 157 | **COM43** | 5533.88 | 203.83 |
| 158 | **COM45** | 5511.88 | 203.83 |
| 159 | **COM47** | 5489.88 | 203.83 |
| 160 | **COM49** | 5467.88 | 203.83 |
| 161 | **COM51** | 5445.88 | 203.83 |
| 162 | **COM53** | 5423.88 | 203.83 |
| 163 | **COM55** | 5401.88 | 203.83 |
| 164 | **COM57** | 5379.88 | 203.83 |
| 165 | **COM59** | 5357.88 | 203.83 |
| 166 | **COM61** | 5335.88 | 203.83 |
| 167 | **COM63** | 5313.88 | 203.83 |
| 168 | **COM65** | 5291.88 | 203.83 |
| 169 | **COM67** | 5269.88 | 203.83 |
| 170 | **COM69** | 5247.88 | 203.83 |
| 171 | **COM71** | 5225.88 | 203.83 |
| 172 | **COM73** | 5203.88 | 203.83 |
| 173 | **COM75** | 5181.88 | 203.83 |
| 174 | **COM77** | 5159.88 | 203.83 |
| 175 | **COM79** | 5137.88 | 203.83 |
| 176 | **COM81** | 5115.88 | 203.83 |
| 177 | **COM83** | 5093.88 | 203.83 |
| 178 | **COM85** | 5071.88 | 203.83 |
| 179 | **COM87** | 5049.88 | 203.83 |
| 180 | **COM89** | 5027.88 | 203.83 |
| 181 | **COM91** | 5005.88 | 203.83 |
| 182 | **COM93** | 4983.88 | 203.83 |
| 183 | **COM95** | 4961.88 | 203.83 |

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|---|---|---|---|
| 184 | **COM97** | 4939.88 | 203.83 |
| 185 | **COM99** | 4917.88 | 203.83 |
| 186 | **COM101** | 4895.88 | 203.83 |
| 187 | **COM103** | 4873.88 | 203.83 |
| 188 | **COM105** | 4851.88 | 203.83 |
| 189 | **COM107** | 4829.88 | 203.83 |
| 190 | **COM109** | 4807.88 | 203.83 |
| 191 | **COM111** | 4785.88 | 203.83 |
| 192 | **COM113** | 4763.88 | 203.83 |
| 193 | **COM115** | 4741.88 | 203.83 |
| 194 | **COM117** | 4719.88 | 203.83 |
| 195 | **COM119** | 4697.88 | 203.83 |
| 196 | **COM121** | 4675.88 | 203.83 |
| 197 | **COM123** | 4653.88 | 203.83 |
| 198 | **COM125** | 4631.88 | 203.83 |
| 199 | **COM127** | 4609.88 | 203.83 |
| 200 | **DUMMY** | 4587.88 | 203.83 |
| 201 | **DUMMY** | 4565.88 | 203.83 |
| 202 | **DUMMY** | 4543.88 | 203.83 |
| 203 | **DUMMY** | 4521.88 | 203.83 |
| 204 | **DUMMY** | 4499.88 | 203.83 |
| 205 | **DUMMY** | 4477.88 | 203.83 |
| 206 | **DUMMY** | 4455.88 | 203.83 |
| 207 | **DUMMY** | 4433.88 | 203.83 |
| 208 | **DUMMY** | 4411.88 | 203.83 |
| 209 | **DUMMY** | 4389.88 | 203.83 |
| 210 | **DUMMY** | 4367.88 | 203.83 |
| 211 | **DUMMY** | 4345.88 | 203.83 |
| 212 | **DUMMY** | 4323.88 | 203.83 |
| 213 | **SEG0** | 4213 | 203.83 |
| 214 | **SEG1** | 4191 | 203.83 |
| 215 | **SEG2** | 4169 | 203.83 |
| 216 | **SEG3** | 4147 | 203.83 |
| 217 | **SEG4** | 4125 | 203.83 |
| 218 | **SEG5** | 4103 | 203.83 |
| 219 | **SEG6** | 4081 | 203.83 |
| 220 | **SEG7** | 4059 | 203.83 |

| | | | |
|---|---|---|---|
| 221 | **SEG8** | 4037 | 203.83 |
| 222 | **SEG9** | 4015 | 203.83 |
| 223 | **SEG10** | 3993 | 203.83 |
| 224 | **SEG11** | 3971 | 203.83 |
| 225 | **SEG12** | 3949 | 203.83 |
| 226 | **SEG13** | 3927 | 203.83 |
| 227 | **SEG14** | 3905 | 203.83 |
| 228 | **SEG15** | 3883 | 203.83 |
| 229 | **SEG16** | 3861 | 203.83 |
| 230 | **SEG17** | 3839 | 203.83 |
| 231 | **SEG18** | 3817 | 203.83 |
| 232 | **SEG19** | 3795 | 203.83 |
| 233 | **SEG20** | 3773 | 203.83 |
| 234 | **SEG21** | 3751 | 203.83 |
| 235 | **SEG22** | 3729 | 203.83 |
| 236 | **SEG23** | 3707 | 203.83 |
| 237 | **SEG24** | 3685 | 203.83 |
| 238 | **SEG25** | 3663 | 203.83 |
| 239 | **SEG26** | 3641 | 203.83 |
| 240 | **SEG27** | 3619 | 203.83 |
| 241 | **SEG28** | 3597 | 203.83 |
| 242 | **SEG29** | 3575 | 203.83 |
| 243 | **SEG30** | 3553 | 203.83 |
| 244 | **SEG31** | 3531 | 203.83 |
| 245 | **SEG32** | 3509 | 203.83 |
| 246 | **SEG33** | 3487 | 203.83 |
| 247 | **SEG34** | 3465 | 203.83 |
| 248 | **SEG35** | 3443 | 203.83 |
| 249 | **SEG36** | 3421 | 203.83 |
| 250 | **SEG37** | 3399 | 203.83 |
| 251 | **SEG38** | 3377 | 203.83 |
| 252 | **SEG39** | 3355 | 203.83 |
| 253 | **SEG40** | 3333 | 203.83 |
| 254 | **SEG41** | 3311 | 203.83 |
| 255 | **SEG42** | 3289 | 203.83 |
| 256 | **SEG43** | 3267 | 203.83 |
| 257 | **SEG44** | 3245 | 203.83 |
| 258 | **SEG45** | 3223 | 203.83 |
| 259 | **SEG46** | 3201 | 203.83 |
| 260 | **SEG47** | 3179 | 203.83 |
| 261 | **SEG48** | 3157 | 203.83 |
| 262 | **SEG49** | 3135 | 203.83 |
| 263 | **SEG50** | 3113 | 203.83 |
| 264 | **SEG51** | 3091 | 203.83 |
| 265 | **SEG52** | 3069 | 203.83 |
| 266 | **SEG53** | 3047 | 203.83 |
| 267 | **SEG54** | 3025 | 203.83 |
| 268 | **SEG55** | 3003 | 203.83 |
| 269 | **SEG56** | 2981 | 203.83 |
| 270 | **SEG57** | 2959 | 203.83 |
| 271 | **SEG58** | 2937 | 203.83 |
| 272 | **SEG59** | 2915 | 203.83 |
| 273 | **SEG60** | 2893 | 203.83 |
| 274 | **SEG61** | 2871 | 203.83 |
| 275 | **SEG62** | 2849 | 203.83 |
| 276 | **SEG63** | 2827 | 203.83 |
| 277 | **SEG64** | 2805 | 203.83 |
| 278 | **SEG65** | 2783 | 203.83 |
| 279 | **SEG66** | 2761 | 203.83 |
| 280 | **SEG67** | 2739 | 203.83 |
| 281 | **SEG68** | 2717 | 203.83 |
| 282 | **SEG69** | 2695 | 203.83 |
| 283 | **SEG70** | 2673 | 203.83 |
| 284 | **SEG71** | 2651 | 203.83 |
| 285 | **SEG72** | 2629 | 203.83 |
| 286 | **SEG73** | 2607 | 203.83 |
| 287 | **SEG74** | 2585 | 203.83 |
| 288 | **SEG75** | 2563 | 203.83 |
| 289 | **SEG76** | 2541 | 203.83 |
| 290 | **SEG77** | 2519 | 203.83 |
| 291 | **SEG78** | 2497 | 203.83 |
| 292 | **SEG79** | 2475 | 203.83 |
| 293 | **SEG80** | 2453 | 203.83 |
| 294 | **SEG81** | 2431 | 203.83 |

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|---|---|---|---|
| 295 | **SEG82** | 2409 | 203.83 |
| 296 | **SEG83** | 2387 | 203.83 |
| 297 | **SEG84** | 2365 | 203.83 |
| 298 | **SEG85** | 2343 | 203.83 |
| 299 | **SEG86** | 2321 | 203.83 |
| 300 | **SEG87** | 2299 | 203.83 |
| 301 | **SEG88** | 2277 | 203.83 |
| 302 | **SEG89** | 2255 | 203.83 |
| 303 | **SEG90** | 2233 | 203.83 |
| 304 | **SEG91** | 2211 | 203.83 |
| 305 | **SEG92** | 2189 | 203.83 |
| 306 | **SEG93** | 2167 | 203.83 |
| 307 | **SEG94** | 2145 | 203.83 |
| 308 | **SEG95** | 2123 | 203.83 |
| 309 | **SEG96** | 2101 | 203.83 |
| 310 | **SEG97** | 2079 | 203.83 |
| 311 | **SEG98** | 2057 | 203.83 |
| 312 | **SEG99** | 2035 | 203.83 |
| 313 | **SEG100** | 2013 | 203.83 |
| 314 | **SEG101** | 1991 | 203.83 |
| 315 | **SEG102** | 1969 | 203.83 |
| 316 | **SEG103** | 1947 | 203.83 |
| 317 | **SEG104** | 1925 | 203.83 |
| 318 | **SEG105** | 1903 | 203.83 |
| 319 | **SEG106** | 1881 | 203.83 |
| 320 | **SEG107** | 1859 | 203.83 |
| 321 | **SEG108** | 1837 | 203.83 |
| 322 | **SEG109** | 1815 | 203.83 |
| 323 | **SEG110** | 1793 | 203.83 |
| 324 | **SEG111** | 1771 | 203.83 |
| 325 | **SEG112** | 1749 | 203.83 |
| 326 | **SEG113** | 1727 | 203.83 |
| 327 | **SEG114** | 1705 | 203.83 |
| 328 | **SEG115** | 1683 | 203.83 |
| 329 | **SEG116** | 1661 | 203.83 |
| 330 | **SEG117** | 1639 | 203.83 |
| 331 | **SEG118** | 1617 | 203.83 |
| 332 | **SEG119** | 1595 | 203.83 |
| 333 | **SEG120** | 1573 | 203.83 |
| 334 | **SEG121** | 1551 | 203.83 |
| 335 | **SEG122** | 1529 | 203.83 |
| 336 | **SEG123** | 1507 | 203.83 |
| 337 | **SEG124** | 1485 | 203.83 |
| 338 | **SEG125** | 1463 | 203.83 |
| 339 | **SEG126** | 1441 | 203.83 |
| 340 | **SEG127** | 1419 | 203.83 |
| 341 | **SEG128** | 1397 | 203.83 |
| 342 | **SEG129** | 1375 | 203.83 |
| 343 | **SEG130** | 1353 | 203.83 |
| 344 | **SEG131** | 1331 | 203.83 |
| 345 | **SEG132** | 1309 | 203.83 |
| 346 | **SEG133** | 1287 | 203.83 |
| 347 | **SEG134** | 1265 | 203.83 |
| 348 | **SEG135** | 1243 | 203.83 |
| 349 | **SEG136** | 1221 | 203.83 |
| 350 | **SEG137** | 1199 | 203.83 |
| 351 | **SEG138** | 1177 | 203.83 |
| 352 | **SEG139** | 1155 | 203.83 |
| 353 | **SEG140** | 1133 | 203.83 |
| 354 | **SEG141** | 1111 | 203.83 |
| 355 | **SEG142** | 1089 | 203.83 |
| 356 | **SEG143** | 1067 | 203.83 |
| 357 | **SEG144** | 1045 | 203.83 |
| 358 | **SEG145** | 1023 | 203.83 |
| 359 | **SEG146** | 1001 | 203.83 |
| 360 | **SEG147** | 979 | 203.83 |
| 361 | **SEG148** | 957 | 203.83 |
| 362 | **SEG149** | 935 | 203.83 |
| 363 | **SEG150** | 913 | 203.83 |
| 364 | **SEG151** | 891 | 203.83 |
| 365 | **SEG152** | 869 | 203.83 |
| 366 | **SEG153** | 847 | 203.83 |
| 367 | **SEG154** | 825 | 203.83 |
| 368 | **SEG155** | 803 | 203.83 |

| | | | |
|---|---|---|---|
| 369 | **SEG156** | 781 | 203.83 |
| 370 | **SEG157** | 759 | 203.83 |
| 371 | **SEG158** | 737 | 203.83 |
| 372 | **SEG159** | 715 | 203.83 |
| 373 | **SEG160** | 693 | 203.83 |
| 374 | **SEG161** | 671 | 203.83 |
| 375 | **SEG162** | 649 | 203.83 |
| 376 | **SEG163** | 627 | 203.83 |
| 377 | **SEG164** | 605 | 203.83 |
| 378 | **SEG165** | 583 | 203.83 |
| 379 | **SEG166** | 561 | 203.83 |
| 380 | **SEG167** | 539 | 203.83 |
| 381 | **SEG168** | 517 | 203.83 |
| 382 | **SEG169** | 495 | 203.83 |
| 383 | **SEG170** | 473 | 203.83 |
| 384 | **SEG171** | 451 | 203.83 |
| 385 | **SEG172** | 429 | 203.83 |
| 386 | **SEG173** | 407 | 203.83 |
| 387 | **SEG174** | 385 | 203.83 |
| 388 | **SEG175** | 363 | 203.83 |
| 389 | **SEG176** | 341 | 203.83 |
| 390 | **SEG177** | 319 | 203.83 |
| 391 | **SEG178** | 297 | 203.83 |
| 392 | **SEG179** | 275 | 203.83 |
| 393 | **SEG180** | 253 | 203.83 |
| 394 | **SEG181** | 231 | 203.83 |
| 395 | **SEG182** | 209 | 203.83 |
| 396 | **SEG183** | 187 | 203.83 |
| 397 | **SEG184** | 165 | 203.83 |
| 398 | **SEG185** | 143 | 203.83 |
| 399 | **SEG186** | 121 | 203.83 |
| 400 | **SEG187** | 99 | 203.83 |
| 401 | **SEG188** | 77 | 203.83 |
| 402 | **SEG189** | 55 | 203.83 |
| 403 | **SEG190** | 33 | 203.83 |
| 404 | **SEG191** | 11 | 203.83 |
| 405 | **SEG192** | -11 | 203.83 |
| 406 | **SEG193** | -33 | 203.83 |
| 407 | **SEG194** | -55 | 203.83 |
| 408 | **SEG195** | -77 | 203.83 |
| 409 | **SEG196** | -99 | 203.83 |
| 410 | **SEG197** | -121 | 203.83 |
| 411 | **SEG198** | -143 | 203.83 |
| 412 | **SEG199** | -165 | 203.83 |
| 413 | **SEG200** | -187 | 203.83 |
| 414 | **SEG201** | -209 | 203.83 |
| 415 | **SEG202** | -231 | 203.83 |
| 416 | **SEG203** | -253 | 203.83 |
| 417 | **SEG204** | -275 | 203.83 |
| 418 | **SEG205** | -297 | 203.83 |
| 419 | **SEG206** | -319 | 203.83 |
| 420 | **SEG207** | -341 | 203.83 |
| 421 | **SEG208** | -363 | 203.83 |
| 422 | **SEG209** | -385 | 203.83 |
| 423 | **SEG210** | -407 | 203.83 |
| 424 | **SEG211** | -429 | 203.83 |
| 425 | **SEG212** | -451 | 203.83 |
| 426 | **SEG213** | -473 | 203.83 |
| 427 | **SEG214** | -495 | 203.83 |
| 428 | **SEG215** | -517 | 203.83 |
| 429 | **SEG216** | -539 | 203.83 |
| 430 | **SEG217** | -561 | 203.83 |
| 431 | **SEG218** | -583 | 203.83 |
| 432 | **SEG219** | -605 | 203.83 |
| 433 | **SEG220** | -627 | 203.83 |
| 434 | **SEG221** | -649 | 203.83 |
| 435 | **SEG222** | -671 | 203.83 |
| 436 | **SEG223** | -693 | 203.83 |
| 437 | **SEG224** | -715 | 203.83 |
| 438 | **SEG225** | -737 | 203.83 |
| 439 | **SEG226** | -759 | 203.83 |
| 440 | **SEG227** | -781 | 203.83 |
| 441 | **SEG228** | -803 | 203.83 |
| 442 | **SEG229** | -825 | 203.83 |

| | | | |
|---|---|---|---|
| 443 | **SEG230** | -847 | 203.83 |
| 444 | **SEG231** | -869 | 203.83 |
| 445 | **SEG232** | -891 | 203.83 |
| 446 | **SEG233** | -913 | 203.83 |
| 447 | **SEG234** | -935 | 203.83 |
| 448 | **SEG235** | -957 | 203.83 |
| 449 | **SEG236** | -979 | 203.83 |
| 450 | **SEG237** | -1001 | 203.83 |
| 451 | **SEG238** | -1023 | 203.83 |
| 452 | **SEG239** | -1045 | 203.83 |
| 453 | **SEG240** | -1067 | 203.83 |
| 454 | **SEG241** | -1089 | 203.83 |
| 455 | **SEG242** | -1111 | 203.83 |
| 456 | **SEG243** | -1133 | 203.83 |
| 457 | **SEG244** | -1155 | 203.83 |
| 458 | **SEG245** | -1177 | 203.83 |
| 459 | **SEG246** | -1199 | 203.83 |
| 460 | **SEG247** | -1221 | 203.83 |
| 461 | **SEG248** | -1243 | 203.83 |
| 462 | **SEG249** | -1265 | 203.83 |
| 463 | **SEG250** | -1287 | 203.83 |
| 464 | **SEG251** | -1309 | 203.83 |
| 465 | **SEG252** | -1331 | 203.83 |
| 466 | **SEG253** | -1353 | 203.83 |
| 467 | **SEG254** | -1375 | 203.83 |
| 468 | **SEG255** | -1397 | 203.83 |
| 469 | **SEG256** | -1419 | 203.83 |
| 470 | **SEG257** | -1441 | 203.83 |
| 471 | **SEG258** | -1463 | 203.83 |
| 472 | **SEG259** | -1485 | 203.83 |
| 473 | **SEG260** | -1507 | 203.83 |
| 474 | **SEG261** | -1529 | 203.83 |
| 475 | **SEG262** | -1551 | 203.83 |
| 476 | **SEG263** | -1573 | 203.83 |
| 477 | **SEG264** | -1595 | 203.83 |
| 478 | **SEG265** | -1617 | 203.83 |
| 479 | **SEG266** | -1639 | 203.83 |

| | | | |
|---|---|---|---|
| 480 | **SEG267** | -1661 | 203.83 |
| 481 | **SEG268** | -1683 | 203.83 |
| 482 | **SEG269** | -1705 | 203.83 |
| 483 | **SEG270** | -1727 | 203.83 |
| 484 | **SEG271** | -1749 | 203.83 |
| 485 | **SEG272** | -1771 | 203.83 |
| 486 | **SEG273** | -1793 | 203.83 |
| 487 | **SEG274** | -1815 | 203.83 |
| 488 | **SEG275** | -1837 | 203.83 |
| 489 | **SEG276** | -1859 | 203.83 |
| 490 | **SEG277** | -1881 | 203.83 |
| 491 | **SEG278** | -1903 | 203.83 |
| 492 | **SEG279** | -1925 | 203.83 |
| 493 | **SEG280** | -1947 | 203.83 |
| 494 | **SEG281** | -1969 | 203.83 |
| 495 | **SEG282** | -1991 | 203.83 |
| 496 | **SEG283** | -2013 | 203.83 |
| 497 | **SEG284** | -2035 | 203.83 |
| 498 | **SEG285** | -2057 | 203.83 |
| 499 | **SEG286** | -2079 | 203.83 |
| 500 | **SEG287** | -2101 | 203.83 |
| 501 | **SEG288** | -2123 | 203.83 |
| 502 | **SEG289** | -2145 | 203.83 |
| 503 | **SEG290** | -2167 | 203.83 |
| 504 | **SEG291** | -2189 | 203.83 |
| 505 | **SEG292** | -2211 | 203.83 |
| 506 | **SEG293** | -2233 | 203.83 |
| 507 | **SEG294** | -2255 | 203.83 |
| 508 | **SEG295** | -2277 | 203.83 |
| 509 | **SEG296** | -2299 | 203.83 |
| 510 | **SEG297** | -2321 | 203.83 |
| 511 | **SEG298** | -2343 | 203.83 |
| 512 | **SEG299** | -2365 | 203.83 |
| 513 | **SEG300** | -2387 | 203.83 |
| 514 | **SEG301** | -2409 | 203.83 |
| 515 | **SEG302** | -2431 | 203.83 |
| 516 | **SEG303** | -2453 | 203.83 |

| | | | |
|---|---|---|---|
| 517 | **SEG304** | -2475 | 203.83 |
| 518 | **SEG305** | -2497 | 203.83 |
| 519 | **SEG306** | -2519 | 203.83 |
| 520 | **SEG307** | -2541 | 203.83 |
| 521 | **SEG308** | -2563 | 203.83 |
| 522 | **SEG309** | -2585 | 203.83 |
| 523 | **SEG310** | -2607 | 203.83 |
| 524 | **SEG311** | -2629 | 203.83 |
| 525 | **SEG312** | -2651 | 203.83 |
| 526 | **SEG313** | -2673 | 203.83 |
| 527 | **SEG314** | -2695 | 203.83 |
| 528 | **SEG315** | -2717 | 203.83 |
| 529 | **SEG316** | -2739 | 203.83 |
| 530 | **SEG317** | -2761 | 203.83 |
| 531 | **SEG318** | -2783 | 203.83 |
| 532 | **SEG319** | -2805 | 203.83 |
| 533 | **SEG320** | -2827 | 203.83 |
| 534 | **SEG321** | -2849 | 203.83 |
| 535 | **SEG322** | -2871 | 203.83 |
| 536 | **SEG323** | -2893 | 203.83 |
| 537 | **SEG324** | -2915 | 203.83 |
| 538 | **SEG325** | -2937 | 203.83 |
| 539 | **SEG326** | -2959 | 203.83 |
| 540 | **SEG327** | -2981 | 203.83 |
| 541 | **SEG328** | -3003 | 203.83 |
| 542 | **SEG329** | -3025 | 203.83 |
| 543 | **SEG330** | -3047 | 203.83 |
| 544 | **SEG331** | -3069 | 203.83 |
| 545 | **SEG332** | -3091 | 203.83 |
| 546 | **SEG333** | -3113 | 203.83 |
| 547 | **SEG334** | -3135 | 203.83 |
| 548 | **SEG335** | -3157 | 203.83 |
| 549 | **SEG336** | -3179 | 203.83 |
| 550 | **SEG337** | -3201 | 203.83 |
| 551 | **SEG338** | -3223 | 203.83 |
| 552 | **SEG339** | -3245 | 203.83 |
| 553 | **SEG340** | -3267 | 203.83 |

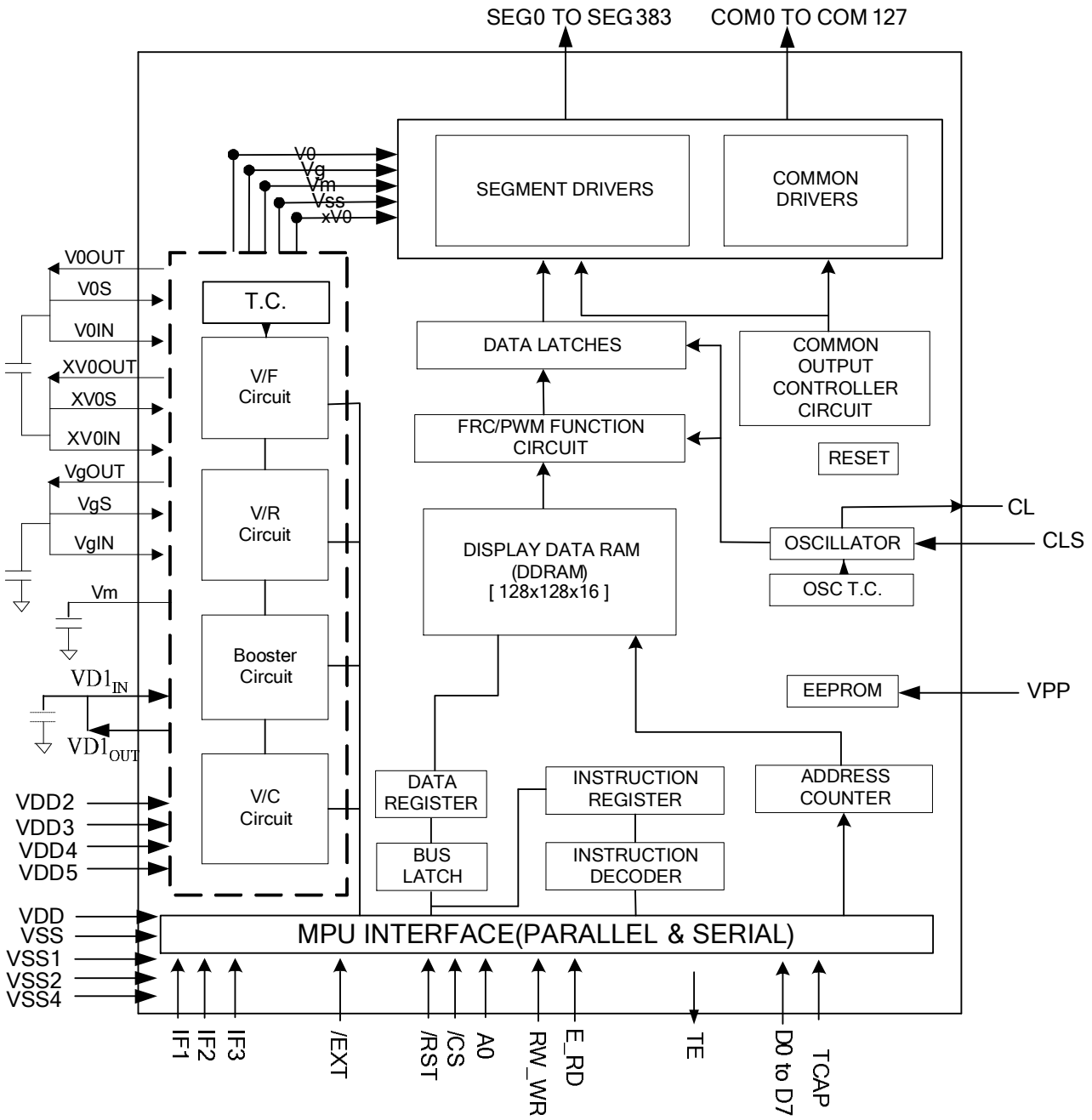
| | | | |
|---|---|---|---|
| 554 | **SEG341** | -3289 | 203.83 |
| 555 | **SEG342** | -3311 | 203.83 |
| 556 | **SEG343** | -3333 | 203.83 |
| 557 | **SEG344** | -3355 | 203.83 |
| 558 | **SEG345** | -3377 | 203.83 |
| 559 | **SEG346** | -3399 | 203.83 |
| 560 | **SEG347** | -3421 | 203.83 |
| 561 | **SEG348** | -3443 | 203.83 |
| 562 | **SEG349** | -3465 | 203.83 |
| 563 | **SEG350** | -3487 | 203.83 |
| 564 | **SEG351** | -3509 | 203.83 |
| 565 | **SEG352** | -3531 | 203.83 |
| 566 | **SEG353** | -3553 | 203.83 |
| 567 | **SEG354** | -3575 | 203.83 |
| 568 | **SEG355** | -3597 | 203.83 |
| 569 | **SEG356** | -3619 | 203.83 |
| 570 | **SEG357** | -3641 | 203.83 |
| 571 | **SEG358** | -3663 | 203.83 |
| 572 | **SEG359** | -3685 | 203.83 |
| 573 | **SEG360** | -3707 | 203.83 |
| 574 | **SEG361** | -3729 | 203.83 |
| 575 | **SEG362** | -3751 | 203.83 |
| 576 | **SEG363** | -3773 | 203.83 |
| 577 | **SEG364** | -3795 | 203.83 |
| 578 | **SEG365** | -3817 | 203.83 |
| 579 | **SEG366** | -3839 | 203.83 |
| 580 | **SEG367** | -3861 | 203.83 |
| 581 | **SEG368** | -3883 | 203.83 |
| 582 | **SEG369** | -3905 | 203.83 |
| 583 | **SEG370** | -3927 | 203.83 |
| 584 | **SEG371** | -3949 | 203.83 |
| 585 | **SEG372** | -3971 | 203.83 |
| 586 | **SEG373** | -3993 | 203.83 |
| 587 | **SEG374** | -4015 | 203.83 |
| 588 | **SEG375** | -4037 | 203.83 |
| 589 | **SEG376** | -4059 | 203.83 |
| 590 | **SEG377** | -4081 | 203.83 |

| | | | |
|---|---|---|---|
| 591 | **SEG378** | -4103 | 203.83 |
| 592 | **SEG379** | -4125 | 203.83 |
| 593 | **SEG380** | -4147 | 203.83 |
| 594 | **SEG381** | -4169 | 203.83 |
| 595 | **SEG382** | -4191 | 203.83 |
| 596 | **SEG383** | -4213 | 203.83 |
| 597 | **DUMMY** | -4323.88 | 203.83 |
| 598 | **DUMMY** | -4345.88 | 203.83 |
| 599 | **DUMMY** | -4367.88 | 203.83 |
| 600 | **DUMMY** | -4389.88 | 203.83 |
| 601 | **DUMMY** | -4411.88 | 203.83 |
| 602 | **DUMMY** | -4433.88 | 203.83 |
| 603 | **DUMMY** | -4455.88 | 203.83 |
| 604 | **DUMMY** | -4477.88 | 203.83 |
| 605 | **DUMMY** | -4499.88 | 203.83 |
| 606 | **DUMMY** | -4521.88 | 203.83 |
| 607 | **DUMMY** | -4543.88 | 203.83 |
| 608 | **DUMMY** | -4565.88 | 203.83 |
| 609 | **DUMMY** | -4587.88 | 203.83 |
| 610 | **COM126** | -4609.88 | 203.83 |
| 611 | **COM124** | -4631.88 | 203.83 |
| 612 | **COM122** | -4653.88 | 203.83 |
| 613 | **COM120** | -4675.88 | 203.83 |
| 614 | **COM118** | -4697.88 | 203.83 |
| 615 | **COM116** | -4719.88 | 203.83 |
| 616 | **COM114** | -4741.88 | 203.83 |
| 617 | **COM112** | -4763.88 | 203.83 |
| 618 | **COM110** | -4785.88 | 203.83 |
| 619 | **COM108** | -4807.88 | 203.83 |
| 620 | **COM106** | -4829.88 | 203.83 |
| 621 | **COM104** | -4851.88 | 203.83 |
| 622 | **COM102** | -4873.88 | 203.83 |
| 623 | **COM100** | -4895.88 | 203.83 |
| 624 | **COM98** | -4917.88 | 203.83 |
| 625 | **COM96** | -4939.88 | 203.83 |
| 626 | **COM94** | -4961.88 | 203.83 |
| 627 | **COM92** | -4983.88 | 203.83 |

| | | | |
|---|---|---|---|
| 628 | **COM90** | -5005.88 | 203.83 |
| 629 | **COM88** | -5027.88 | 203.83 |
| 630 | **COM86** | -5049.88 | 203.83 |
| 631 | **COM84** | -5071.88 | 203.83 |
| 632 | **COM82** | -5093.88 | 203.83 |
| 633 | **COM80** | -5115.88 | 203.83 |
| 634 | **COM78** | -5137.88 | 203.83 |
| 635 | **COM76** | -5159.88 | 203.83 |
| 636 | **COM74** | -5181.88 | 203.83 |
| 637 | **COM72** | -5203.88 | 203.83 |
| 638 | **COM70** | -5225.88 | 203.83 |
| 639 | **COM68** | -5247.88 | 203.83 |
| 640 | **COM66** | -5269.88 | 203.83 |
| 641 | **COM64** | -5291.88 | 203.83 |
| 642 | **COM62** | -5313.88 | 203.83 |
| 643 | **COM60** | -5335.88 | 203.83 |
| 644 | **COM58** | -5357.88 | 203.83 |
| 645 | **COM56** | -5379.88 | 203.83 |
| 646 | **COM54** | -5401.88 | 203.83 |
| 647 | **COM52** | -5423.88 | 203.83 |
| 648 | **COM50** | -5445.88 | 203.83 |
| 649 | **COM48** | -5467.88 | 203.83 |
| 650 | **COM46** | -5489.88 | 203.83 |
| 651 | **COM44** | -5511.88 | 203.83 |
| 652 | **COM42** | -5533.88 | 203.83 |
| 653 | **COM40** | -5555.88 | 203.83 |
| 654 | **COM38** | -5577.88 | 203.83 |
| 655 | **COM36** | -5599.88 | 203.83 |
| 656 | **COM34** | -5621.88 | 203.83 |
| 657 | **COM32** | -5643.88 | 203.83 |
| 658 | **COM30** | -5665.88 | 203.83 |
| 659 | **COM28** | -5687.88 | 203.83 |
| 660 | **COM26** | -5709.88 | 203.83 |
| 661 | **COM24** | -5642.23 | 74.74 |
| 662 | **COM22** | -5642.23 | 52.74 |
| 663 | **COM20** | -5642.23 | 30.74 |
| 664 | **COM18** | -5642.23 | 8.74 |

| | | | |
|---|---|---|---|
| 665 | **COM16** | -5642.23 | -13.26 |
| 666 | **COM14** | -5642.23 | -35.26 |
| 667 | **COM12** | -5642.23 | -57.26 |
| 668 | **COM10** | -5642.23 | -79.26 |
| 669 | **COM8** | -5642.23 | -101.26 |
| 670 | **COM6** | -5642.23 | -123.26 |
| 671 | **COM4** | -5642.23 | -145.26 |
| 672 | **COM2** | -5642.23 | -167.26 |
| 673 | **COM0** | -5642.23 | -189.26 |
| | **LMARK1** | -5717.5 | -267.5 |
| | **LMARK2** | 5717.5 | -267.5 |

## 5. Block diagram



# 6. PIN DESCRIPTION

## 6.1 Power Supply

| Name | I/O | Description |
|---|---|---|
| VDD | Supply | Power supply for logic circuit. |
| VDD2 | Supply | Power supply for Booster circuit. |
| VDD3 | Supply | Power supply for LCD. |
| VDD4 | Supply | Power supply for LCD. |
| VDD5 | Supply | Power supply for LCD. |
| VSS | Supply | Ground for logic circuit. Ground system should be connected together. |
| VSS1 | Supply | Ground for OSC circuit. Ground system should be connected together. |
| VSS2 | Supply | Ground for Booster circuit. Ground system should be connected together. |
| VSS4 | Supply | Ground for LCD. Ground system should be connected together. |

## 6.2 LCD Power Supply Pins

| Name | I/O | Description |
|---|---|---|
| $V0_{OUT}$<br>$V0_{IN}$<br>$V0_S$ | I/O | Positive LCD driver supply voltages.<br>$V0_{OUT}$ is the output voltage of V0 generated by ST7687S.<br>$V0_{IN}$ is the input pin of power supply to generate V0 voltage for LCD.<br>$V0_S$ is the input pin of power supply to sense the V0 voltage.<br>$V0_{OUT}$ 、$V0_{IN}$ & $V0_S$ should be connected together by FPC. |
| $XV0_{OUT}$<br>$XV0_{IN}$<br>$XV0_S$ | I/O | Negative LCD driver supply voltages.<br>$XV0_{OUT}$ is the output voltage of XV0 generated by ST7687S.<br>$XV0_{IN}$ is the input pin of power supply to generate XV0 voltage for LCD.<br>$XV0_S$ is the input pin of power supply to sense the XV0 voltage.<br>$XV0_{OUT}$ 、$XV0_{IN}$ & $XV0_S$ should be connected together by FPC. |
| $Vg_{OUT}$<br>$Vg_{IN}$<br>$Vg_S$<br>Vm | I/O | Bias LCD driver supply voltages.<br>$Vg_{OUT}$ is the output voltage of Vg generated by ST7687S.<br>$Vg_{IN}$ is the input pin of power supply to generate Vg voltage for LCD.<br>$Vg_S$ is the input pin of power supply to sense the Vg voltage.<br>$Vg_{OUT}$ 、$Vg_{IN}$ & $Vg_S$ should be connected together by FPC.<br>Vm is the I/O pin of LCD bias supply voltage<br>Voltages should have the following relationship;<br>V0 ＞ Vg ＞ Vm ＞ VSS ＞ XV0.<br>VDDA-0.7V＞Vm＞0.7V , 2 x VDDA≧Vg＞1.8V<br>When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias. |

| LCD bias | Vg | Vm |
|---|---|---|
| 1/N bias | (2/N) x V0 | (1/N) x V0 |

NOTE: N = 6 to 12

<table>
<tr>
<td>$VD1_{out}$<br>$VD1_{in}$</td>
<td>I/O</td>
<td>Voltage regulator for digital circuit.<br>$VD1_{out}$ is voltage output from regulator circuit.<br>$VD1_{in}$ is voltage input to digital circuit.<br>$VD1_{in}$ and $VD1_{out}$ should be connected together by FPC.
<table>
<tr><td>Typical VDDI</td><td>Tolerance</td><td>Capacitor of VD1 to VSS</td><td>Level of INTVD1</td></tr>
<tr><td>1.8V</td><td>1.65V~2V</td><td>Unnecessary</td><td>VSS</td></tr>
<tr><td>2.8V</td><td>2.6V~3V</td><td>Unnecessary</td><td>VSS</td></tr>
<tr><td>3.0V</td><td>2.8V~3.2V</td><td>necessary</td><td>VDD</td></tr>
<tr><td>3.3V</td><td>3V~3.6V</td><td>necessary</td><td>VDD</td></tr>
</table>
</td>
</tr>
</table>

## 6.3 System Control

| Name | I/O | Description |
|---|---|---|
| CLS | I | Reserved for testing only.<br>Please fix this pin to VDD. |
| CL | I/O | Reserved for testing only. Leave this pin open. |
| VREF | O | Reference voltage output for monitor only. Left it opened. |
| TCAP | I/O | Test pin. Left it opens. |
| VPP | I | When writing EEPROM, it needs external power supply voltage 18V~19.8V input to write successfully. |
| INTVD1 | I | <table><tr><td>Typical VDDI</td><td>Tolerance</td><td>Capacitor of VD1 to VSS</td><td>Level of INTVD1</td></tr><tr><td>1.8V</td><td>1.65V~2V</td><td>Unnecessary</td><td>VSS</td></tr><tr><td>2.8V</td><td>2.6V~3V</td><td>Unnecessary</td><td>VSS</td></tr><tr><td>3.0V</td><td>2.8V~3.2V</td><td>necessary</td><td>VDD</td></tr><tr><td>3.3V</td><td>3V~3.6V</td><td>necessary</td><td>VDD</td></tr></table> |

## 6.4 Microprocessor Interface

| Name | I/O | Description |
|---|---|---|
| /RST | I | Reset input pin<br>When /RST is “L”, initialization is executed. |

<table>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF3</th><th>IF2</th><th>IF1</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Reserved</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Reserved</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>8-bit serial (4 line)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>9-bit serial (3 line)</td></tr>
</table>
Note:<br>Refer to Table 7.2-1 for detail interface connections.</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins<br>Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D7 become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin<br>In parallel interface:<br>A0 = "H": D0 to D7 or SI are display data<br>A0 = "L": D0 to D7 or SI are control Command<br>In 3-line/4-line interface:<br>This pad will be used for SCL function.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>RW_WR pin is only used in parallel interface.
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin<br>Write status: RW = “L”.<br>Read status: RW = “H”.</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin<br>The data on D0 to D7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When in the serial interface, connect it to VDDI.</td></tr>
</table>

<table>
<tr><td>E_RD</td><td>I</td><td>E_RD pin is only used in parallel interface.<br><table><tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr><tr><td>6800-series</td><td>E</td><td>Enable clock pin:<br>Write status: The data on D0 to D7 are latched at the falling edge of the E signal.<br>Read status: The data on D0 to D7 are latched at the rising edge of the E signal.</td></tr><tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin<br>The data on D0 to D7 are latched at the falling edge of the /WR signal.</td></tr></table>When in the serial interface, connect it to VDDI.</td></tr>
<tr><td>D7 to D0</td><td>I/O</td><td>They connect to the standard 8-bit MPU bus via the 8bit bi-directional bus.<br>When the following interface is selected and the /CS pin is high, the following pins become high impedance.<br>1. In 3-line/4-line interface D0 pad will be used for SI function<br>2. In 4-line interface D1 pad will be used for A0 function<br>3. In Serial interface: unused pins are in the state of high impedance should connect to VDD.</td></tr>
<tr><td>SI</td><td>I</td><td>SI is used to input serial data when the serial interface is selected.(3 line and 4 line)<br>It is used by “D0” pad, See Table 7.2-1.</td></tr>
<tr><td>SCL</td><td>I</td><td>SCL is used to input serial clock when the serial interface is selected.<br>The data is converted in the rising edge. (3 line and 4 line)<br>It is used by “A0” pad , See Table 7.2-1.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output.</td></tr>
<tr><td>/EXT</td><td>I</td><td>EEPROM burn-in control Pin.<br>There is a pull-high resistor between /EXT &VDD in ST7687S.<br>When burning EEPROM, please add an external VSS on /EXT. (needs external power supply voltage VPP=18V~19.8V)</td></tr>
</table>

NOTE:

1. Microprocessor interface pins should not be floating in any operation mode.
2. Unused pin should connect to VDDI (Supply Digital Voltage).

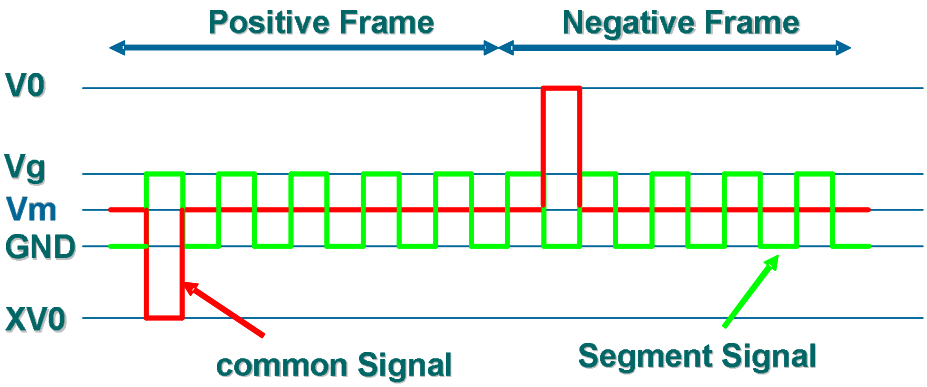
## 6.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0<br>to<br>SEG383</td><td>O</td><td>LCD segment driver outputs<br>The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>Vg</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>L</td><td>Vg</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0<br>to<br>COM127</td><td>O</td><td>LCD common driver outputs<br>The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>XV0</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>Vm</td></tr>
<tr><td>L</td><td>L</td><td>Vm</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>DUMMY</td><td>-</td><td>It’s reserved for test, do not connect ITO or any other electrical-conducted material with it.</td></tr>
</table>

## 6.6 TEST PINS

| | | |
|---|---|---|
| T1 to T8 | - | Reserved for testing only. Please fix these pins to VDDI. |

## Driving Waveform




### ST7687S I/O PIN ITO Resister Limitation

| Pin Name | ITO Resister |
|---|---|
| VDD, VDD2~VDD5, VSS,VSS1,VSS2,VSS4,SI(in parallel interface is D0), $VD1_{in}$, $VD1_{out}$ | <100Ω |
| $V0_{IN}$, $V0_{OUT}$, $V0_S$ ,$XV0_{IN}$, $XV0_{OUT}$ ,$XV0_S$ , $Vg_{IN}$, $Vg_{OUT}$ ,$Vg_S$ ,Vm | <300Ω |
| VPP | <50Ω |
| A0, E_RD, RW_WR, /CS, D0(in parellel interface),D1, ...D7, (SCL), TE, INTVD1 | <1KΩ |
| /RST | <10KΩ |
| IF[3:1], CLS, /EXT | <1KΩ |
| TCAP, CL, VREF | Floating |

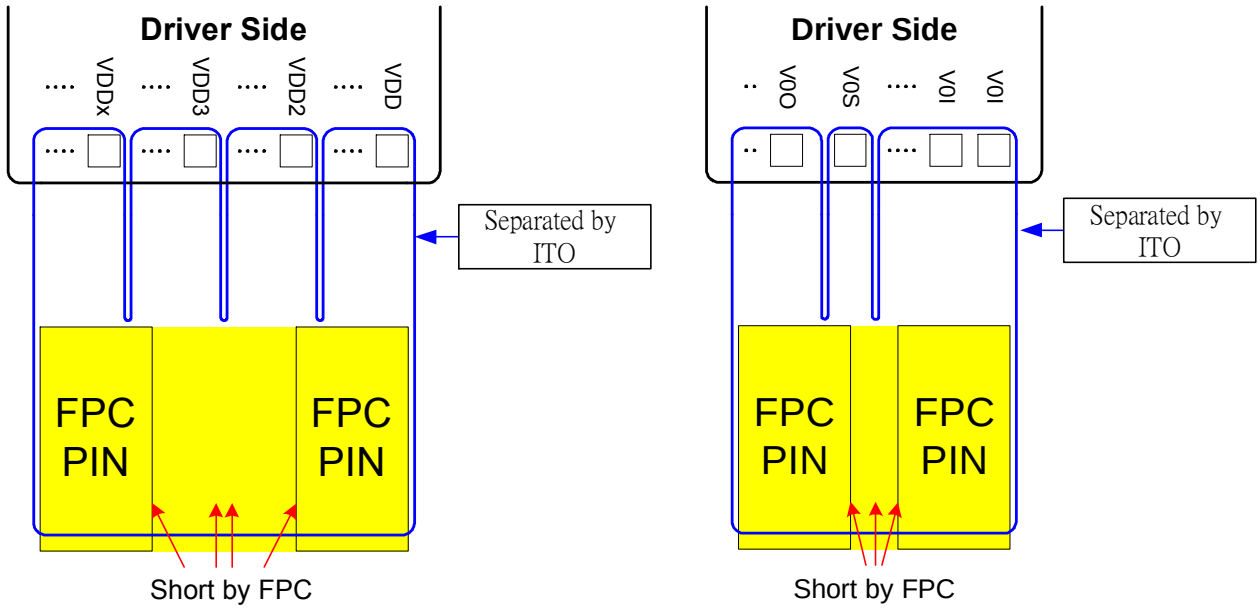


NOTE:

1. Make sure that the ITO resistance of COM0 ~ COM127 is equal, and so is it of SEG0 ~ SEG383.

These limitations include the bottleneck of ITO layout.

2. ITO layout suggestion is shown as below:



# 7. FUNCTIONAL DESCRIPTION

## 7.1 MICROPROCESSOR INTERFACE

### Chip Select Input

/CS pin is chip selection. The ST7687S is active when /CS=L. In serial interface mode, the internal shift register and the counter are reset when /CS=H.

## 7.2 Selecting Parallel / Serial Interface

ST7687S has four types of interfaces with an MPU, which are two serial and two parallel interfaces. These parallel or serial interfaces are determined by IF pin as shown in Table 7.2-1.

| I/F Mode | | | I/F Description | Pin Assignment | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| IF3 | IF2 | IF1 | | /CS | A0 | E_RD | RW_WR | Used Data Bus | D1 | D0 |
| H | H | L | 80 serial 8-bit parallel | /CS | A0 | /RD | /WR | D7~D2 | D1 | D0 |
| H | L | L | 68 serial 8-bit parallel | /CS | A0 | E | R/W | D7~D2 | D1 | D0 |
| L | H | H | 8-bit SPI mode (4 line) | /CS | SCL | -- | -- | -- | A0 | SI |
| L | H | L | 9-bit SPI mode (3 line) | /CS | SCL | -- | -- | -- | -- | SI |

**Table 7.2-1 Parallel / Serial Interface Mode**



### 7.2.1. 8-bit Parallel Interface

The ST7687S identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (R/W) signals, as shown in Table 7.2-2.

| Common | 6800-series | | 8080-series | | Description |
|---|---|---|---|---|---|
| A0 | R/W | E | /WR | /RD | |
| H | H | ↑ | H | ↓ | Display data read out |
| H | H | ↑ | H | ↓ | Register status read |
| L | L | ↓ | ↑ | H | Instruction write |
| H | L | ↓ | ↑ | H | Display data write |

**Table 7.2-2 Parallel Data Transfer**

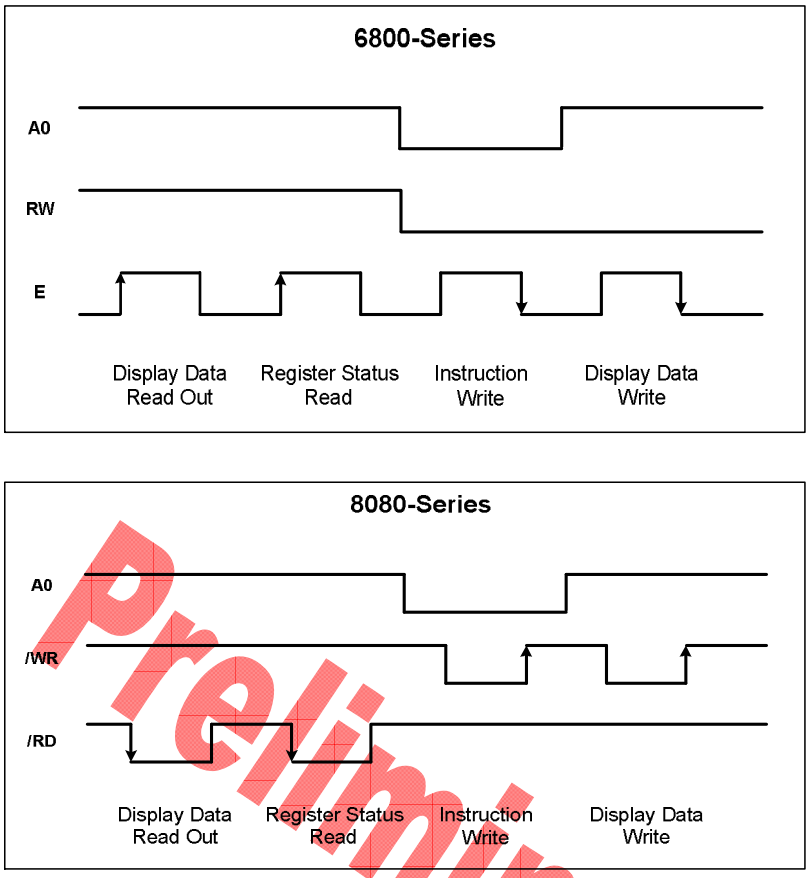





**Figure 7.2-3 Parallel Data Transfer Example Chart**

**Relation between Data Bus and Gradation Data**

ST7687S offers 4096, 65K color display. When using 4096, 65K color display; you can specify color for each of R, G, and B using the palette function. Use the command for switching between these modes.

**(1) 4096-color display**

*(1-1) Type A 4096 color display*

*1. 8-bit mode*

**D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGG** 1st-write

**D7, D6, D5, D4, D3, D2, D1, D0: BBBBRRRR** 2nd-write

**D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB** 3rd-write

There are 3 write operations for 2 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes, and 2nd pixel data is written in the display data RAM when 3rd–write operation finishes.

*(1-2) Type B 4096 color display*

*1. 8-bit mode*

**D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR** 1st-write

**D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB** 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

**(2) 65K color input mode**

*1. 8-bit mode*

**D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG** 1st-write

**D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB** 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes.

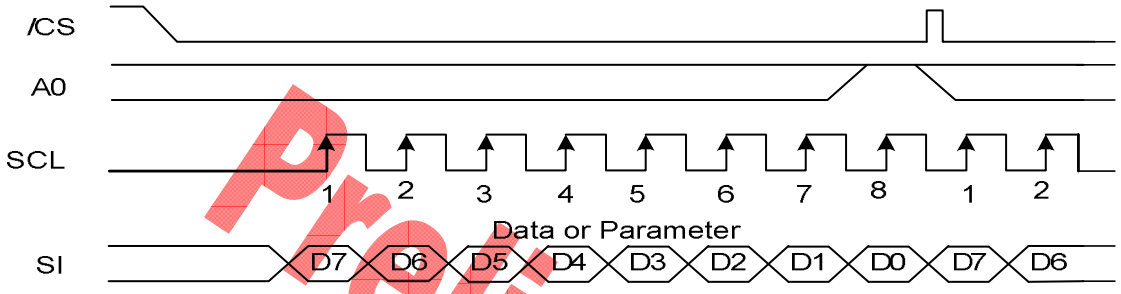
### 7.2.2. 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to write in commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

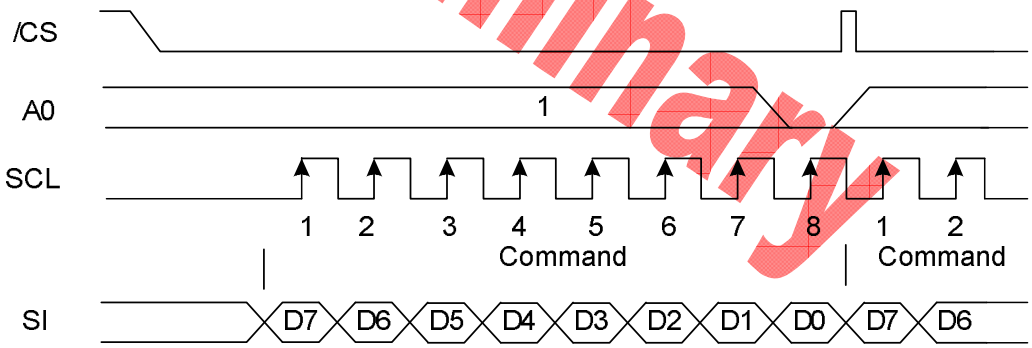
Data read is not available in the serial interface. Data must write to IC with 8 bits for each time. The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

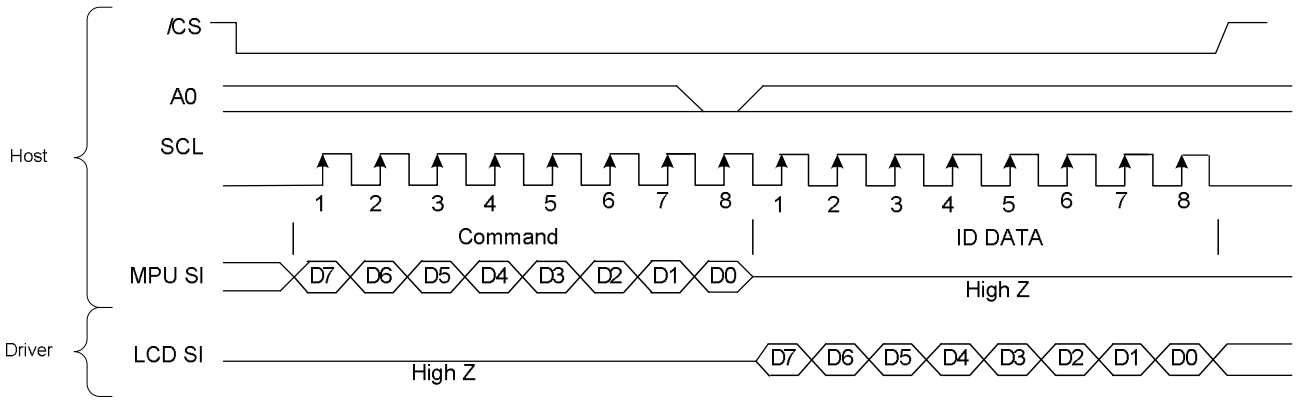
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.




When entering command: A0= LOW at the rising edge of the 8th SCL

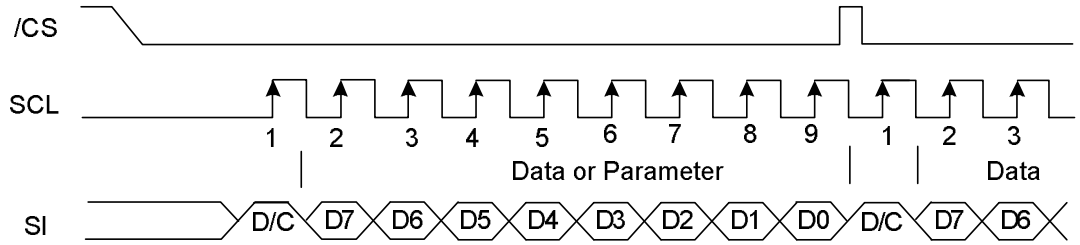



When entering reading command:

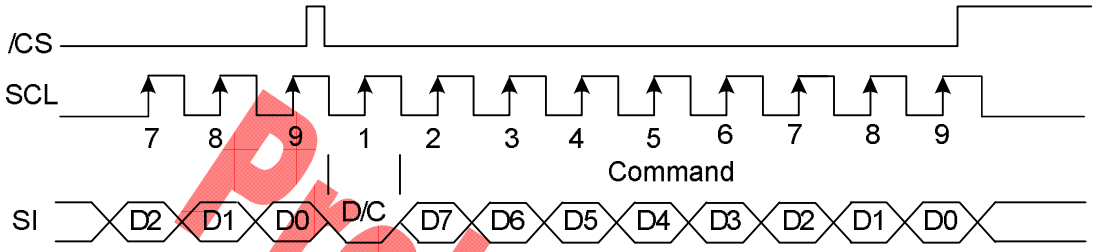


(2) 9-bit serial interface (3-line)

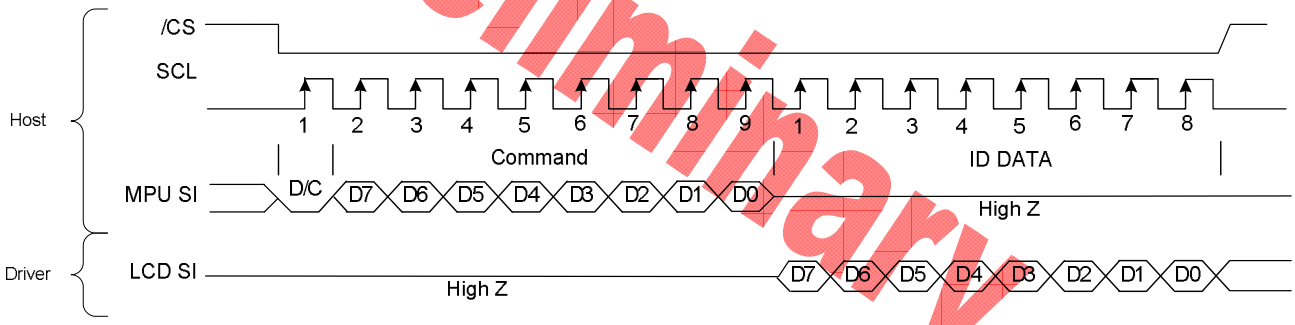
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.




When entering command: SI= LOW at the rising edge of the 1st SCL.




When entering reading command:






- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.

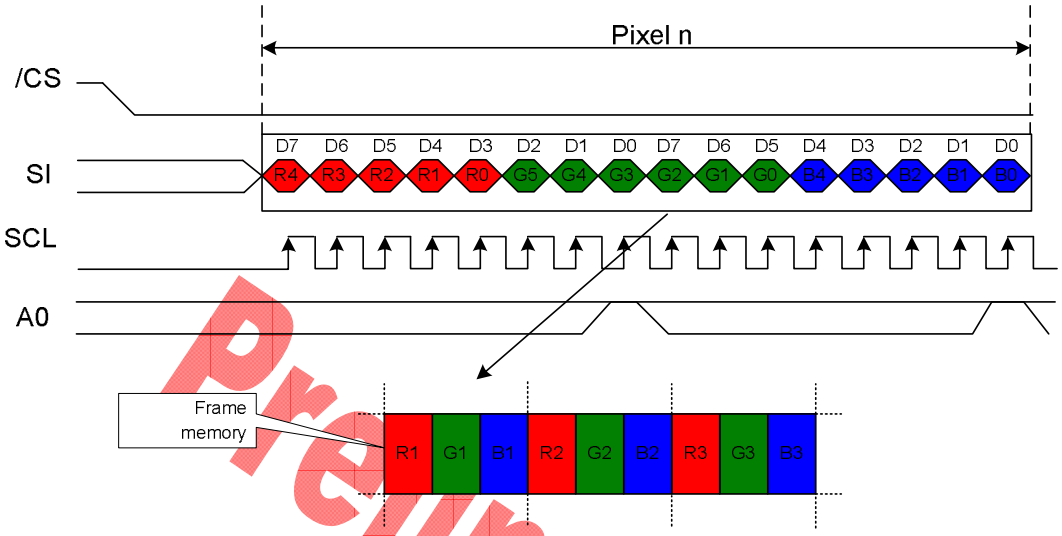
### 7.2.3. 8-bit and 9-bit Serial Interface Data Color Coding

**8-bit serial interface (4-line)**

**R 5-bit, G 6-bit, B 5-bit, 65,536 colors**

There is 1 pixel ( = 3 sub-pixels ) per 2 byte.

There is 1 pixel ( = 3 sub-pixels ) per 2 byte.




Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

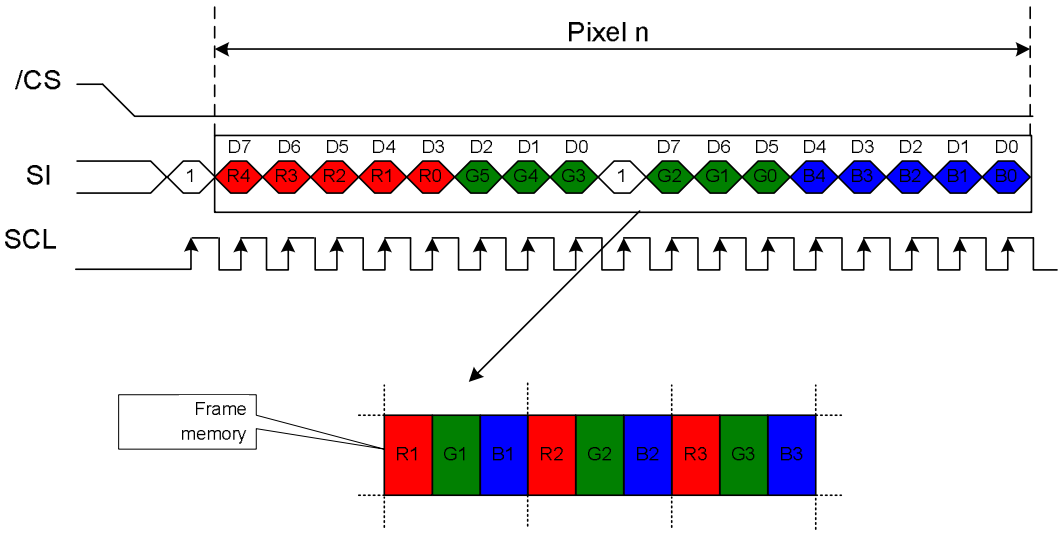


**9-bit serial interface (3-line)**

**R 5-bit, G 6-bit, B 5-bit, 65,536 colors**

There is 1 pixel ( = 3 sub-pixels ) per 2 byte.

There is 1 pixel ( = 3 sub-pixels ) per 2 byte.




Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

## 7.3 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7687S realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.3-1 illustrates these relations.

In 80-series interface mode:

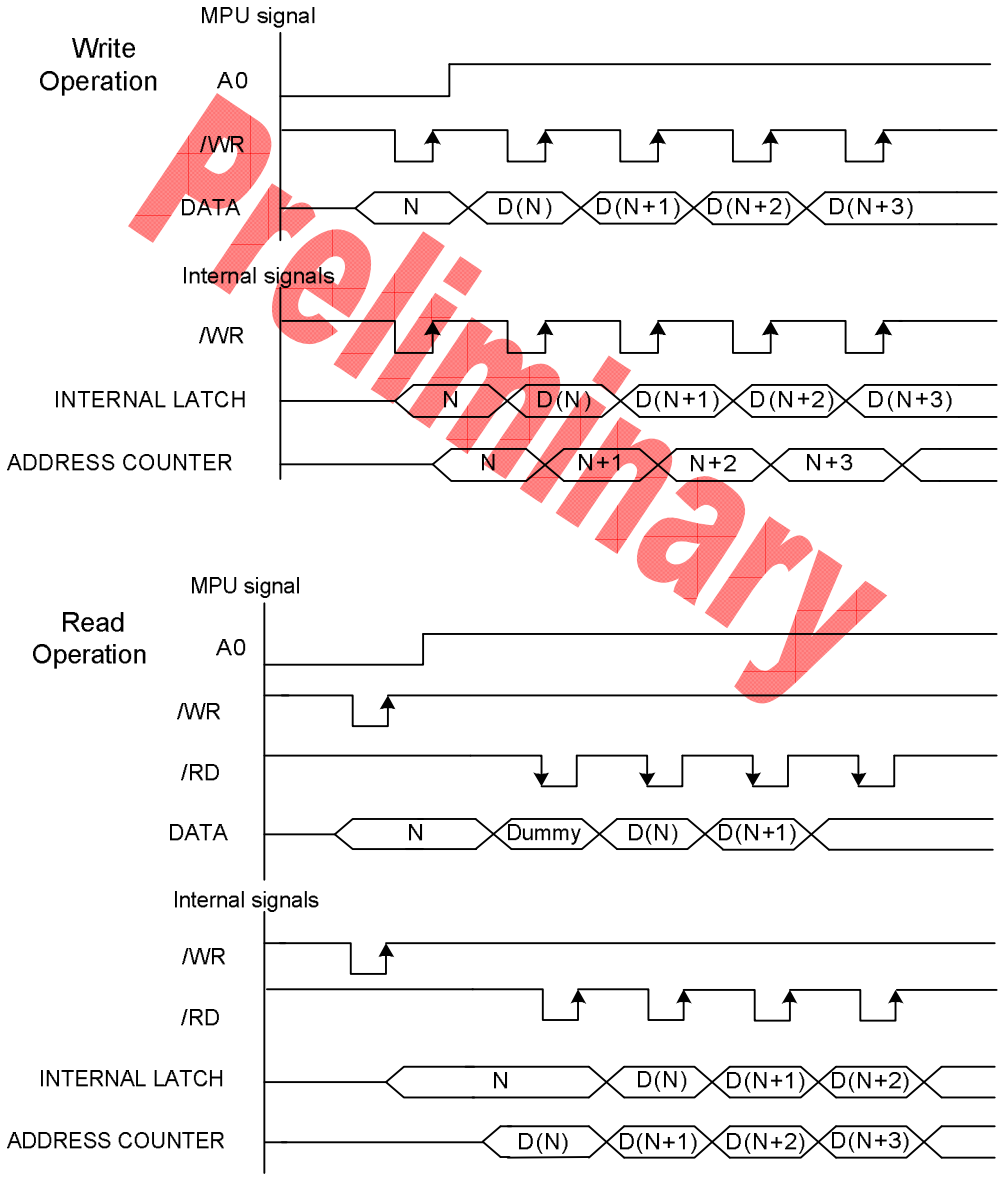





**Figure 7.3-1**

## 7.4 DISPLAY DATA RAM (DDRAM)

### 7.4.1. DDRAM

It is 128 X 128 X 16 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

**Memory Map**

| RGB alignment | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data control command** | | | **Column** | | | | | | | | | |
| | **(MADCTR) MX=0** | | **0** | | | **1** | | | | | **127** | |
| | **(MADCTR) MX=1** | | **127** | | | **126** | | | | | **0** | |
| | **Color** | | **R** | **G** | **B** | **R** | **G** | **B** | | **R** | **G** | **B** |
| | **Data / Page** | | | | | | | | | | | |
| | **(MADCTR) MY=0** | **(MADCTR) MY=1** | | | | | | | | | | |
| | **0** | **127** | | | | | | | | | | |
| | **1** | **126** | | | | | | | | | | |
| | **2** | **125** | | | | | | | | | | |
| | **3** | **124** | | | | | | | | | | |
| | **4** | **123** | | | | | | | | | | |
| | **5** | **122** | | | | | | | | | | |
| | **6** | **121** | | | | | | | | | | |
| | **7** | **120** | | | | | | | | | | |
| | **:** | **:** | | | | | | | | | | |
| | **120** | **7** | | | | | | | | | | |
| | **121** | **6** | | | | | | | | | | |
| | **122** | **5** | | | | | | | | | | |
| | **123** | **4** | | | | | | | | | | |
| | **124** | **3** | | | | | | | | | | |
| | **125** | **2** | | | | | | | | | | |
| | **126** | **1** | | | | | | | | | | |
| | **127** | **0** | | | | | | | | | | |
| **SEGout** | | | **0** | **1** | **2** | **3** | **4** | **5** | | **381** | **382** | **383** |



You can change position of R and B with MADCTR command.

### 7.4.2. Address Control

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel into the RAM matrix of ST7687S. The data for one pixel or two pixels is collected (RGB 5-6-5-bit), according to the data formats. As soon as this pixel-data information is complete, the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=127 (7Fh) and Y=0 to Y=127 (7Fh). Addresses outside these ranges are not allowed.

Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the

command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (7Fh), YE=127 (7Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR”, define flags MV, MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Figure 7.4-1show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

| Condition | Column Counter | Row Counter |
|---|---|---|
| When RAMWR command is accepted | Return to “Start Column (XS)” | Return to “Start Row (YS)” |
| Complete Pixel Read / Write action | Increment by 1 | No change |
| The Column counter value is larger than “End Column (XE)” | Return to “Start Column (XS)” | Increment by 1 |
| The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)” | Return to “Start Column (XS)” | Return to “Start Row (YS)” |

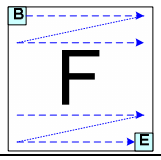
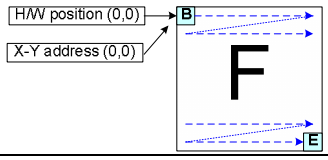
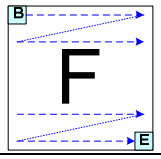
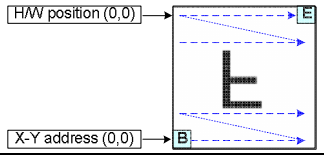
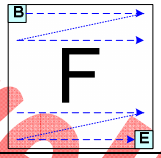
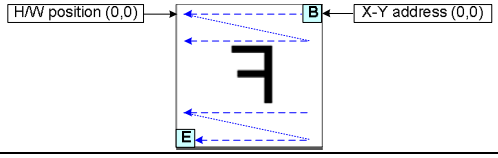
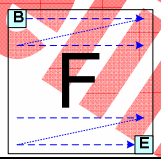
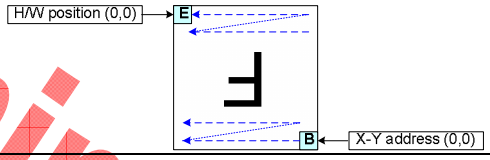
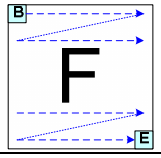
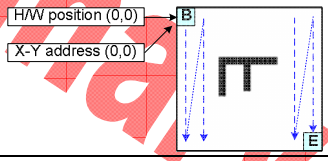
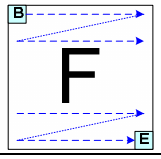
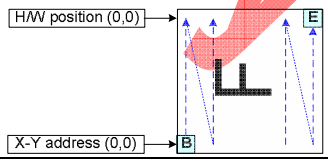
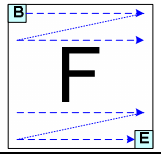
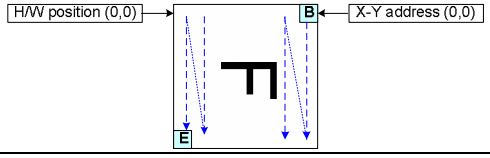
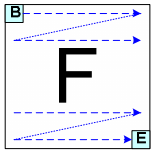
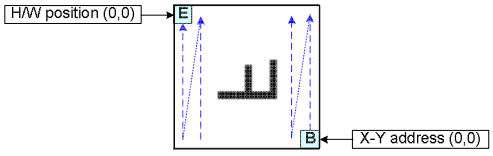
| Display Data Direction | MADCTR Parameter | | | Image in the Host (MPU) | Image in the Driver (DDRAM) |
|---|---|---|---|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 |  |  |
| Y-Mirror | 0 | 0 | 1 |  |  |
| X-Mirror | 0 | 1 | 0 |  |  |
| X-Mirror Y-Mirror | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange Y-Mirror | 1 | 0 | 1 |  |  |
| X-Y Exchange X-Mirror | 1 | 1 | 0 |  |  |
| X-Y Exchange X-Mirror Y-Mirror | 1 | 1 | 1 |  |  |



**Figure 7.4-1 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)**

### 7.4.3. I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

### 7.4.4. Scroll Address Circuit

The circuit associates lines on DDRAM with COM output. ST7687S processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

### 7.4.5. Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

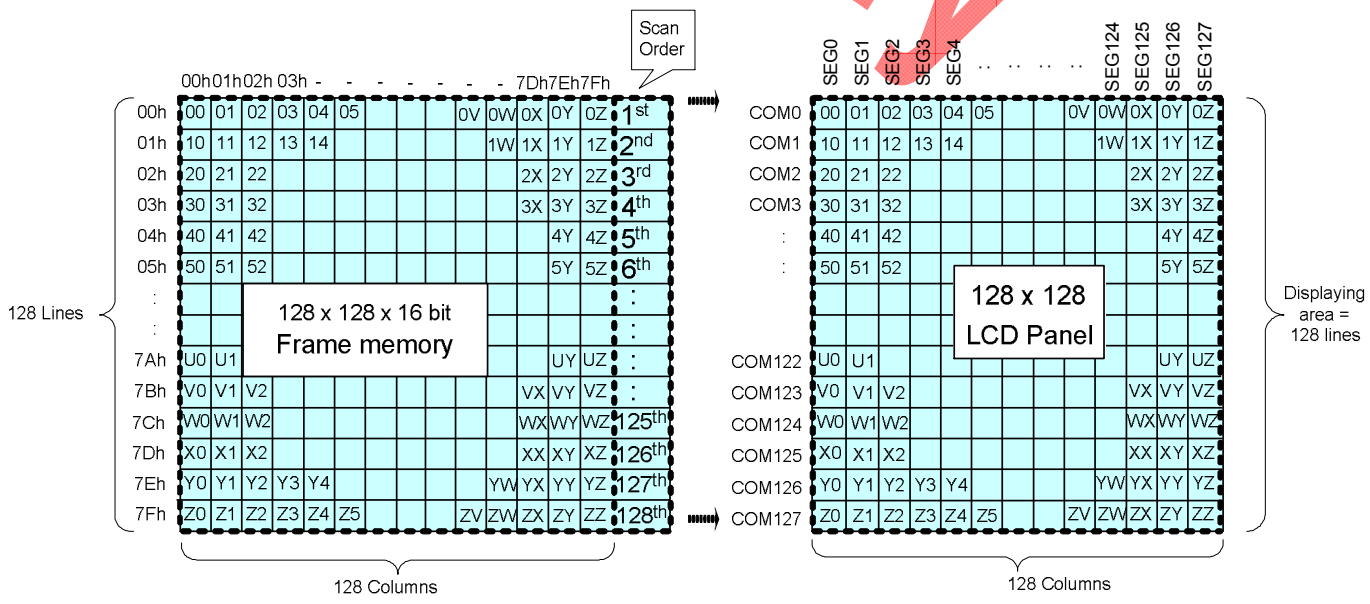


### 7.4.6. Normal Display On or Partial Mode On, Vertical Scroll Off

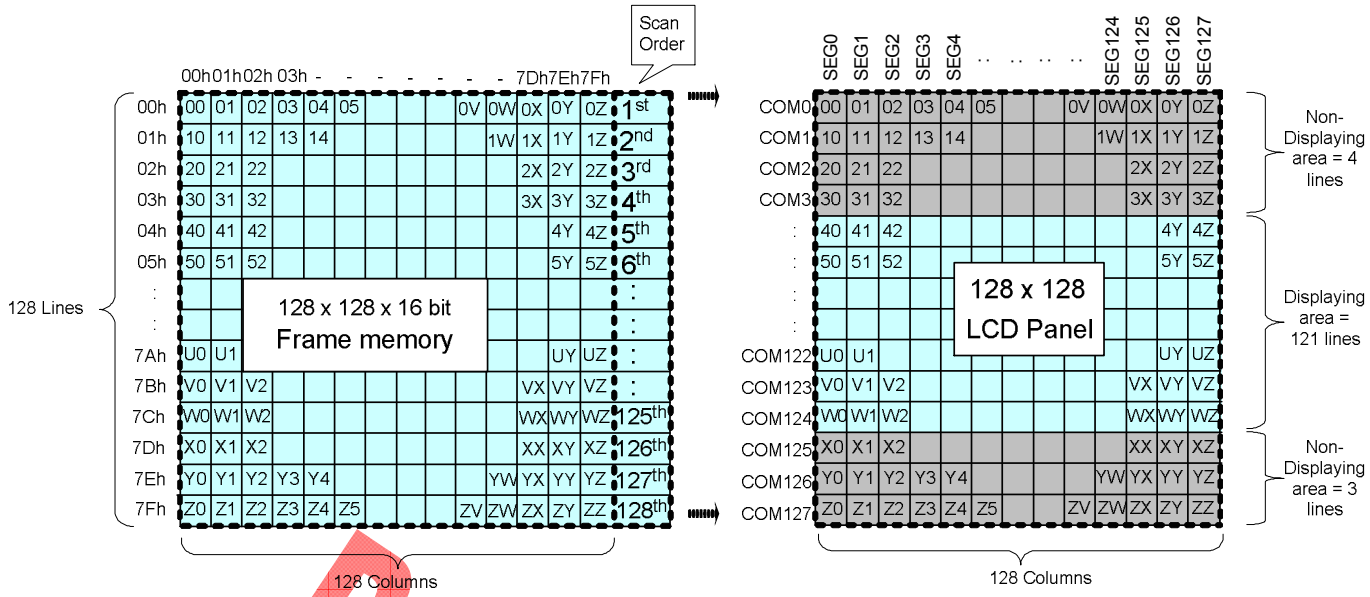
In this mode, contents of the frame memory within an area where column address is 00h to 7Fh and row address is 00h to 7Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On




Example2) Partial Display On: PSL[6:0] = 04h, PEL[6:0] = 7Ch, MADCTR (ML)=0



### 7.4.7. Vertical Scroll/Rolling Scroll

#### 7.4.7.1. Rolling Scroll

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

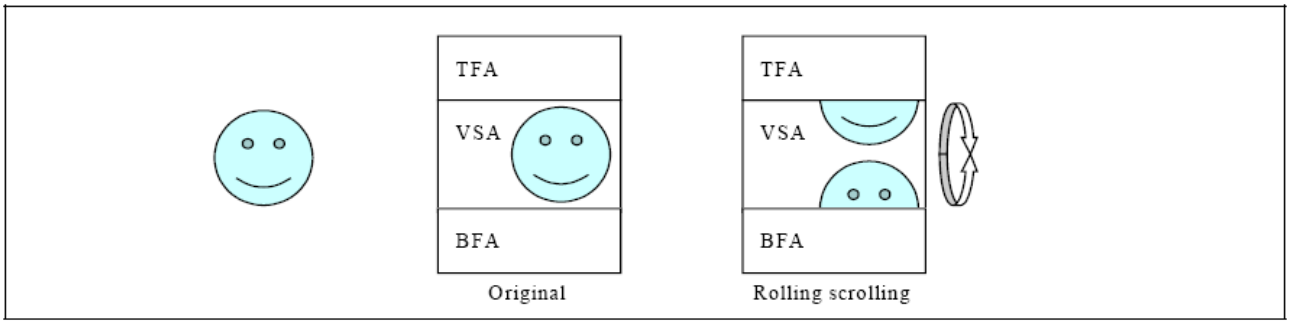
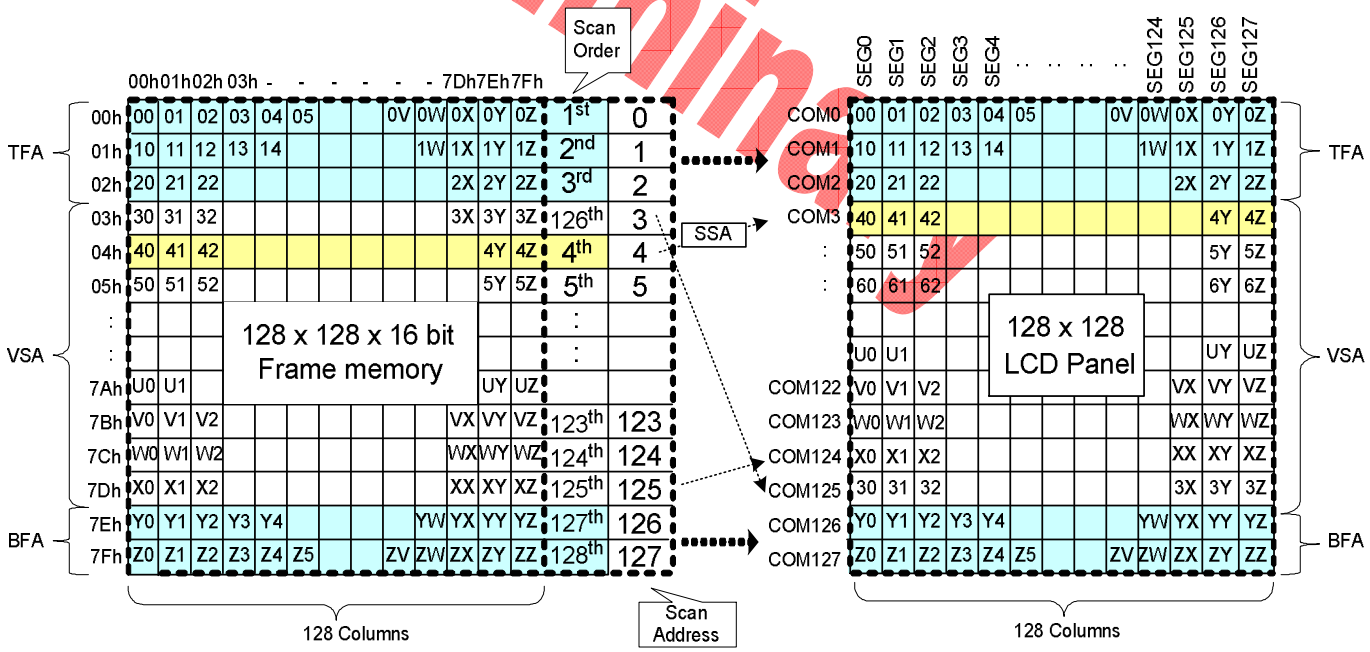



**Figure 7.4-2 Rolling Scroll Definition**

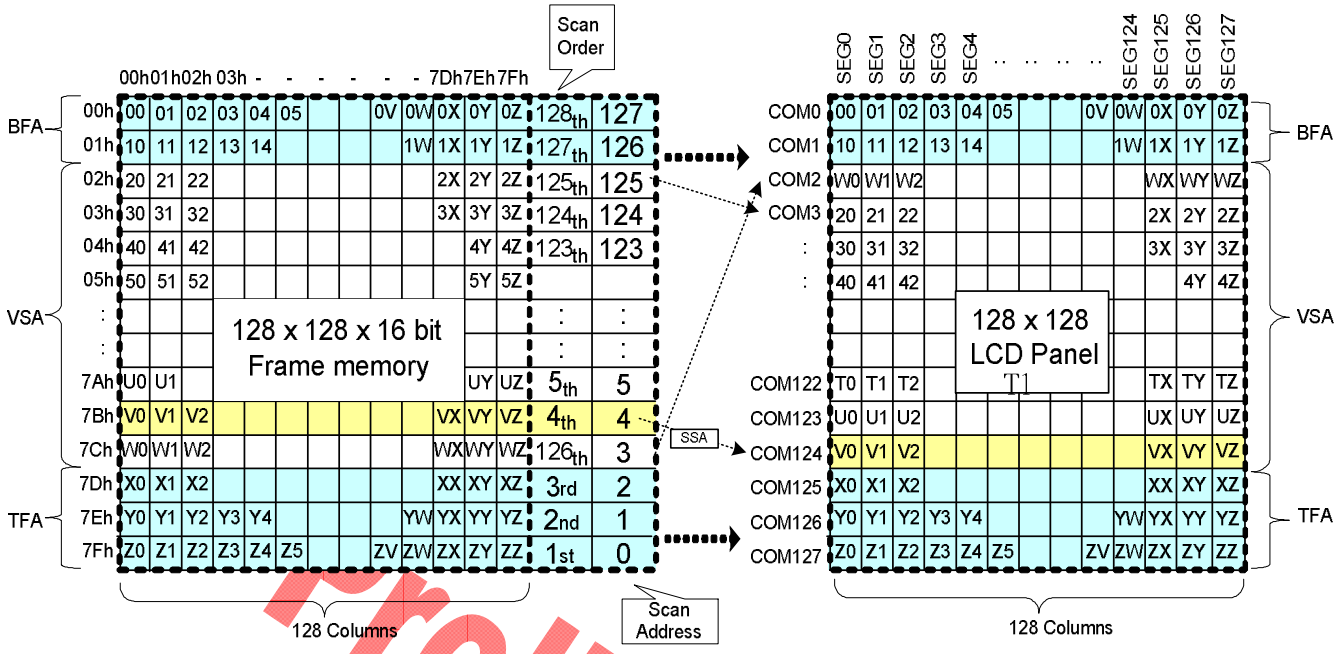


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =128. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=128 x 128, TFA =3, VSA=123, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



Example2) Panel size=128 x 128, TFA =3, VSA=123, BFA=2, SSA=4, MADCTR ML=1: Rolling Scroll (TFA and BFA are exchanged)






### 7.4.7.2. Vertical Scroll Example

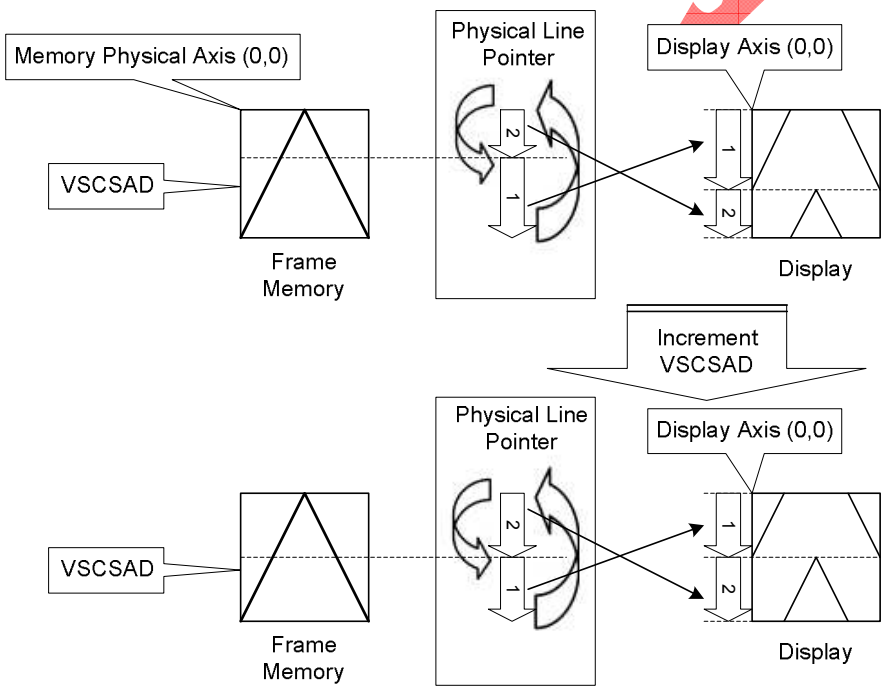
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA<128

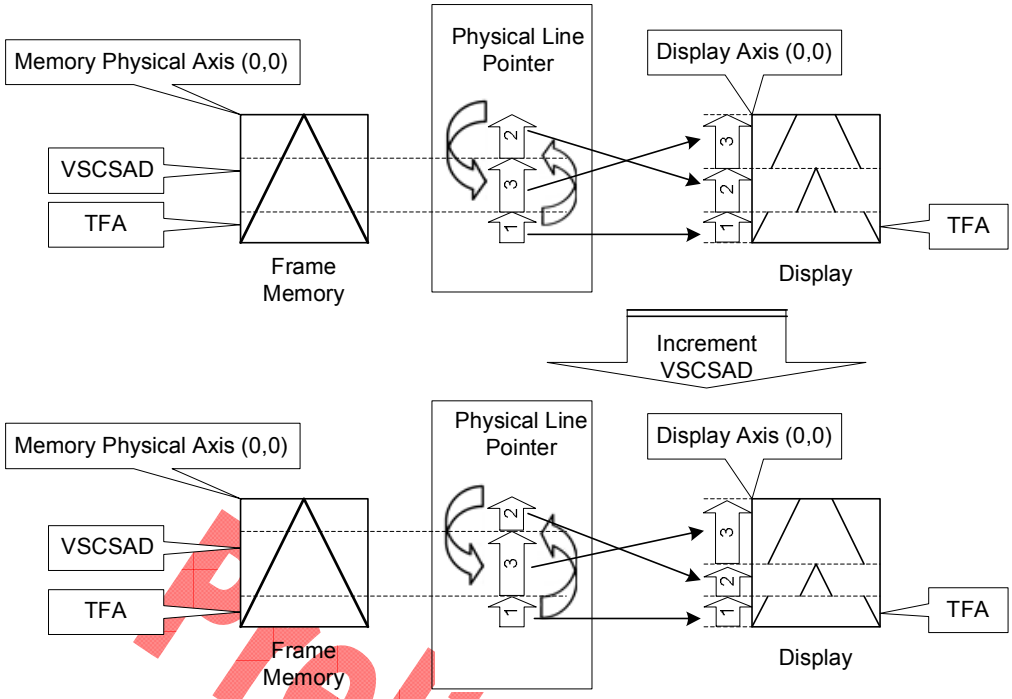
N/A. Do not set TFA + VSA + BFA<128. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=128 (Rolling Scrolling)

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=128, BFA=0 and VSCSAD=40.



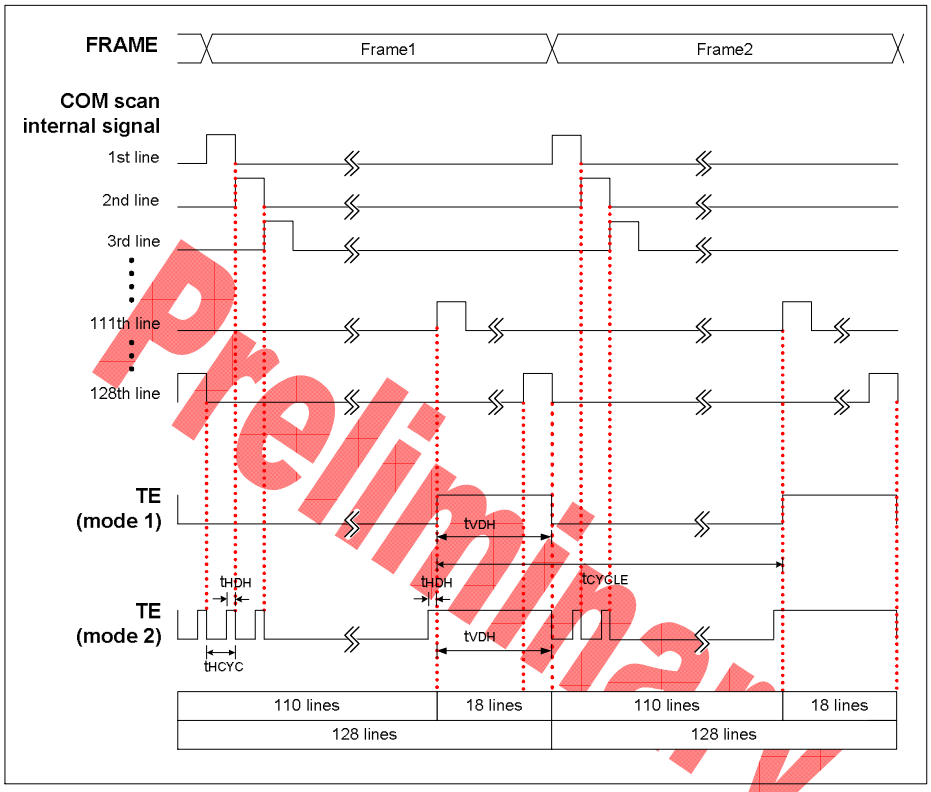
Example2) When MADCTR parameter ML="1", TFA=10, VSA=118, BFA=0 and VSCSAD=30.



### 7.4.8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

#### 7.4.8.1. Tearing Effect Line Modes






**Mode 1**, the Tearing Effect Output signal consists of V-Sync (tVHD) information. It starts at 111th line signal and ends at the 128th line signal. There is one high pulse during each frame.

**Mode 2**, the Tearing Effect Output signal consists of both H-Sync(tHDH) and V-Sync(tVDH) information. TE pin outputs tHDH pulse on each COM scan signal. During 111th ~ 128th line signal, it output a high pulse which equals:
1 tHDH + 1 tVDH.

*Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.*

### 7.4.8.2. Tearing Effect Line Timing

The Tearing Effect signal is described below:

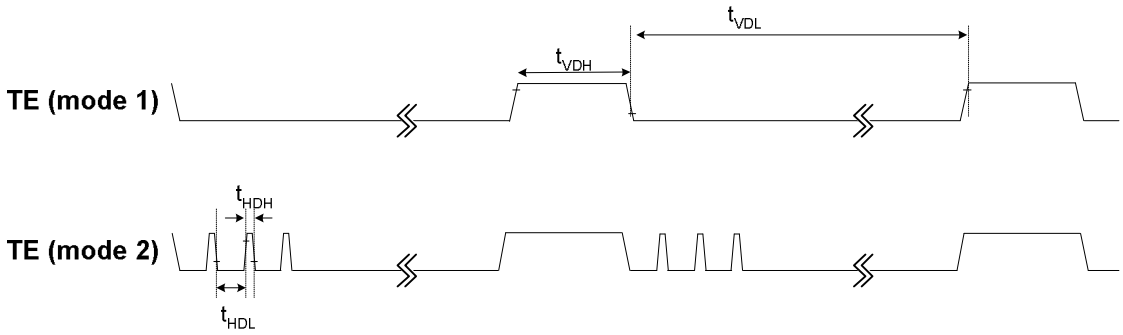
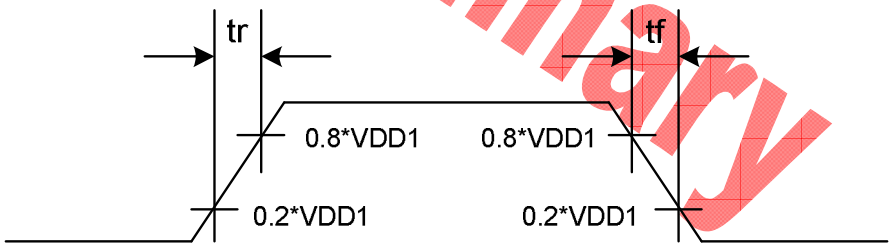



**Figure 7.4-3 AC characteristics of Tearing Effect Signal**

Idle Mode Off (Frame Rate = 77Hz, Nline=0x00)

| Symbol | Parameter | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|---|
| tVDL | Vertical Timing Low Duration | -- | 11.11 | -- | ms | Mode1 |
| tVDH | Vertical Timing High Duration | 1 | 1.82 | -- | ms | |
| tHDL | Horizontal Timing Low Duration | - | 92 | -- | us | Mode2 |
| tHDH | Horizontal Timing High Duration | 3 | 6 | -- | us | |

*Note: The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.*



## 7.5 Gray-Scale Display

ST7687S incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

## 7.6 Oscillation circuit

ST7687s is built-in an oscillator circuit. It provides internal clock without external resistor. This oscillator signal is used in the voltage converter and display timing generation circuit.

## 7.7 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock , which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.7-1.



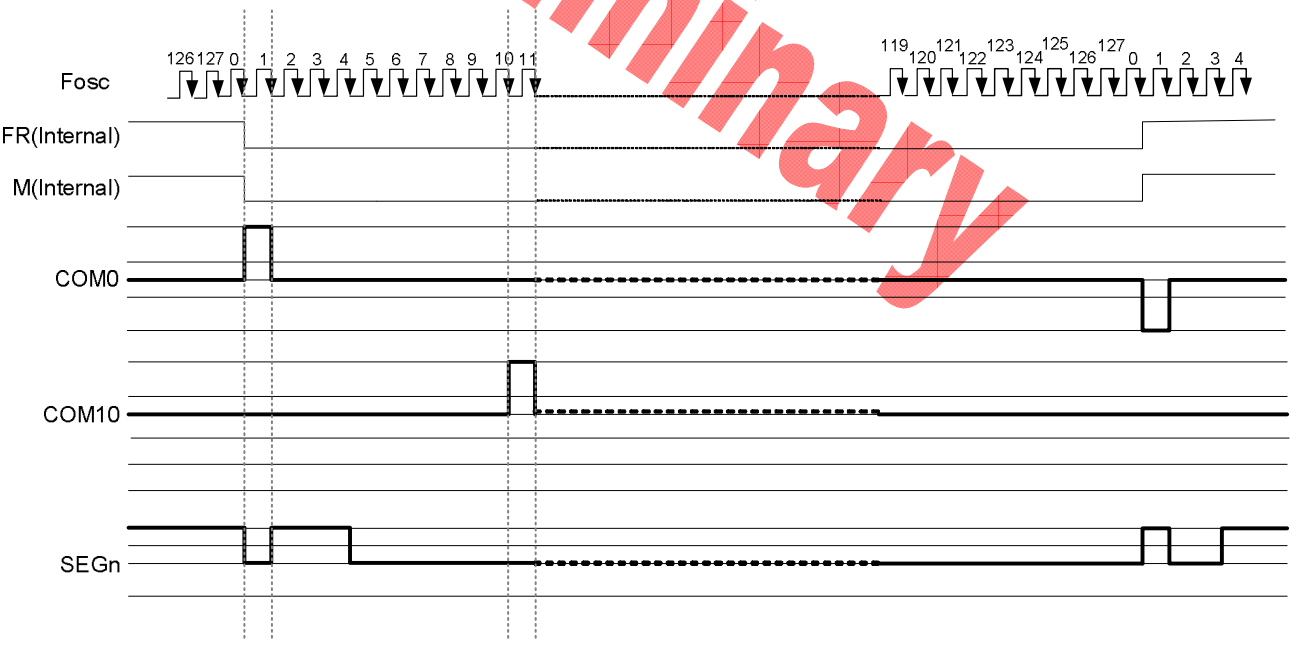



**Figure 7.7-1 2-frame AC Driving Waveform (Duty Ratio: 1/128)**

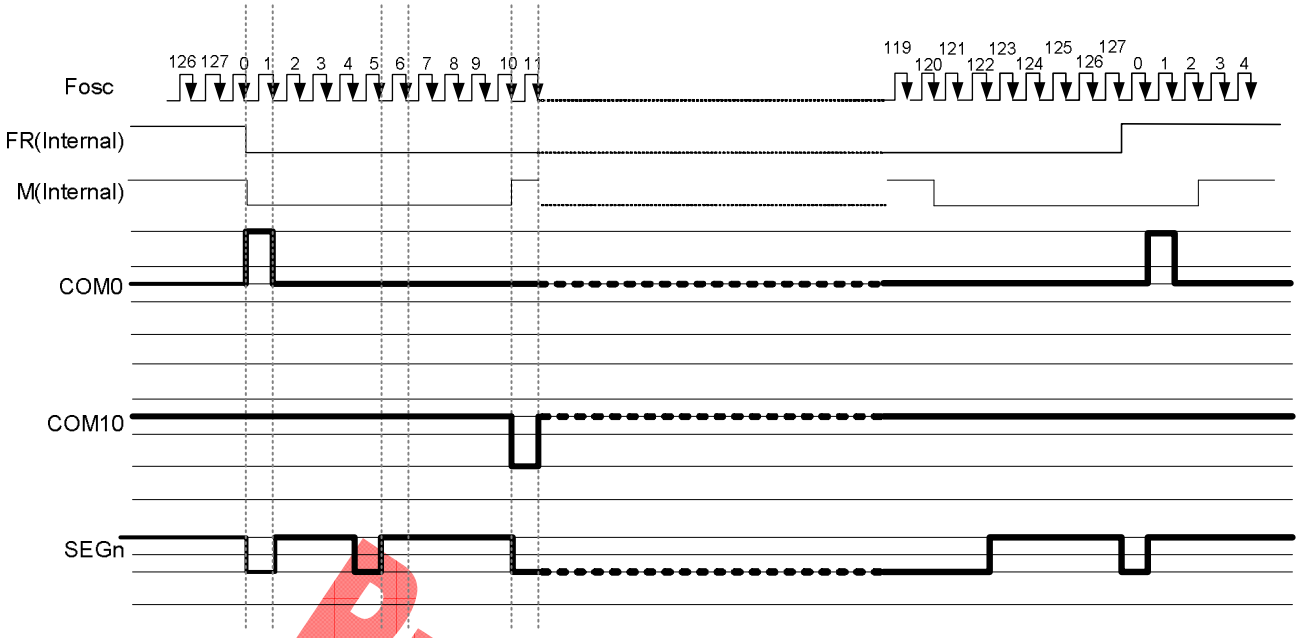





**Figure 7.7-2 N-Line Inversion Driving Waveform (N=10, Duty Ratio=1/128)**

## 7.8 POWER LEVEL DEFINITION

### 7.8.1. Power ON/OFF SEQUENCE

**NOTE: VDDI=VDD; VDDA=VDD2, VDD3, VDD4, VDD5**

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 120msec after /RST has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after /RST has been released.

/CS can be applied at any timing or can be permanently grounded. /RST has priority over /CS.

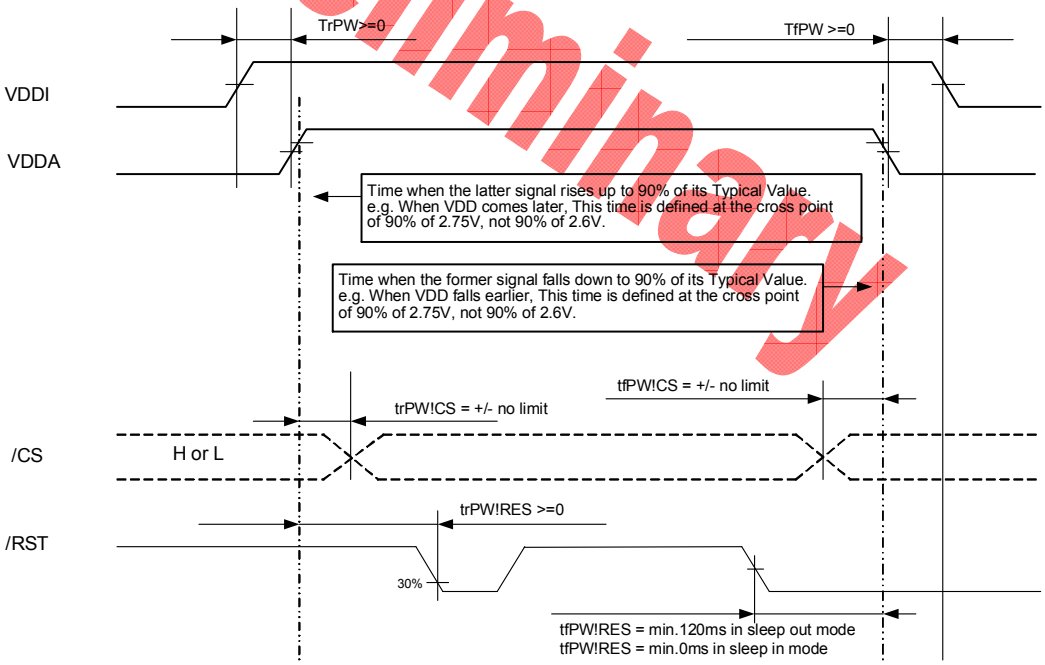
If /RST line is not held stable by host during Power On Sequence as defined in Sections case1 and case2, then it will be necessary to apply a Hardware Reset (/RST) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

**/RST line is held High or Unstable by Host at Power On**

If /RST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDDA and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.






*Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

### 7.8.2. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

***1. Normal Mode On (full display), Idle Mode Off, Sleep Out:***

In this mode, the display is able to show maximum 65K colors.

***2. Partial Mode On, Idle Mode Off, Sleep Out:***

In this mode part of the display is used with maximum 65K colors.

***3. Normal Mode On (full display), Idle Mode On, Sleep Out:***

In this mode, the full display area is used but with 8 colors.

***4. Partial Mode On, Idle Mode On, Sleep Out:***

In this mode, part of the display is used but with 8 colors.

***5. Sleep In Mode:***

In this mode, the DC:DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDD power supply. Contents of the memory are safe.

***6. Power Off Mode:***

In this mode, both Analog VDD and Digital VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

## 7.9 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Figure 7.9-1 shows the referenced combinations in using Power Supply circuits.

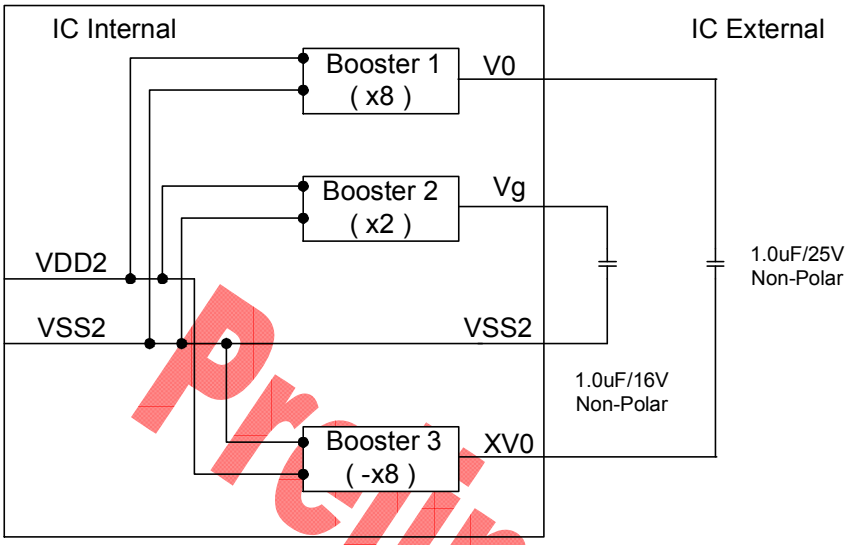



**Figure 7.9-1 DC/DC Booster Block Diagram**



### 7.9.1. Voltage Regulator Circuits

There is a built-in voltage regulator circuits in ST7687S for generating V0. After internal voltage is regulated by voltage regulator circuit, V0 is generated. Detail explanation of V0 set is listed below:

#### 7.9.1.1. SET V0 (Temperatue = 24℃)

**V0=a+{Vop[8:0]+Vop-offset[4:0]+(EV[6:0]-3Fh)}xb (V)**

Example:

Vop[8:0]=011010010

Vop-offset[4:0]=00000

EV[6:0]=0111111

V0=3.6 + { 210 + 0 + (63-63) } x 0.04 =12 (V)

- a is a fixed constant value (see Table 7.9-2).
- b is a fixed constant value (see Table 7.9-2).
- Vop [8:0] is the programmed VOP value. The programming range for Vop[8:0] is 0 to 410 (19Ahex).
- The range of contrast is 128 steps for fine tuning VOP.

| SYMBOL | VALUE | UNIT |
|---|---|---|
| a | 3.6 | V |
| b | 0.04 | V |

**Table 7.9-2**

The Vop [8:0] value must be in the V0 programming range as given in Figure 7.9-3. Evaluating V0 equation, values outside the programming range indicated in many result. V0 range equals from 3.6V to 18V (V0=3.6+{vop[8:0]+vop-offset[4:0]+(EV[6:0]-3Fh)}x0.04).

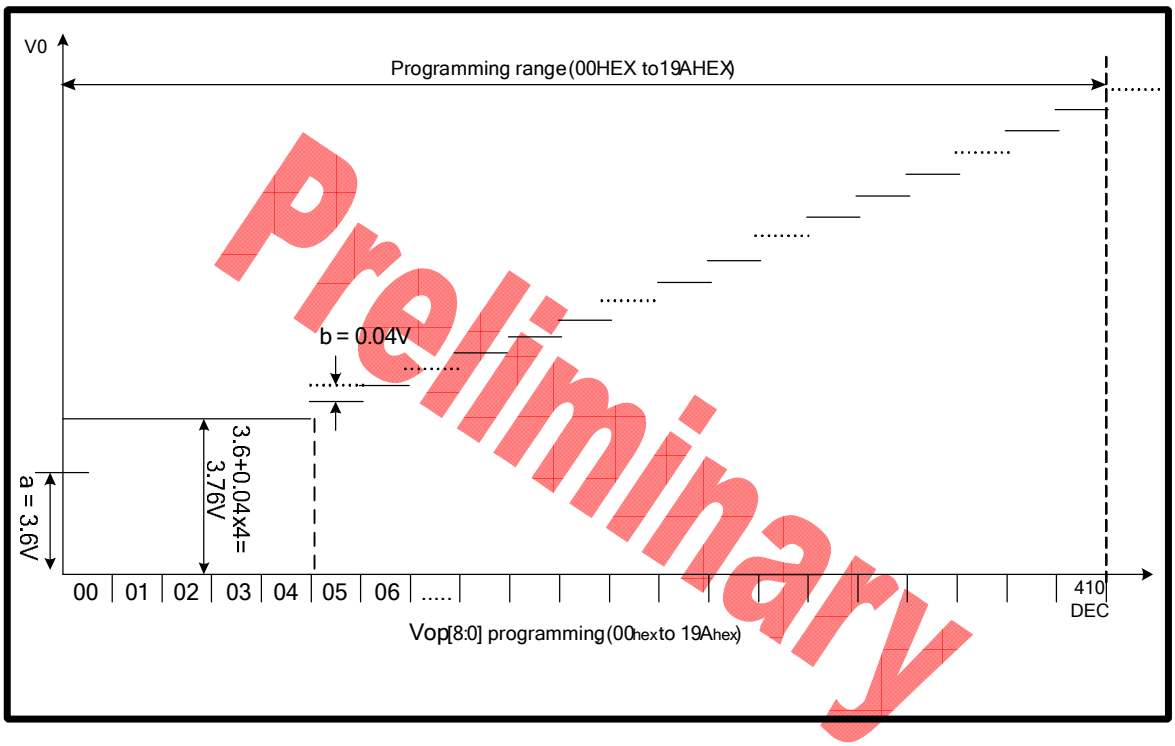





**Figure 7.9-3 V0 programming range**

As the programming range for the internally generated V0 voltage is above the limited V0 (18V), users has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains below 18V.

#### 7.9.1.2. SET V0 with temperature compensation

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficiency for each temperature step. Each temperature step is 8°C. Please see Figure 7.9-4 as below.

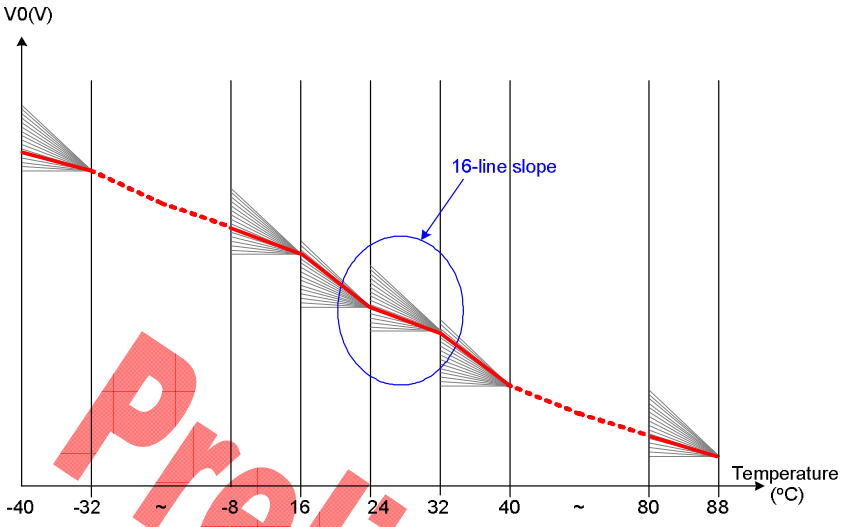
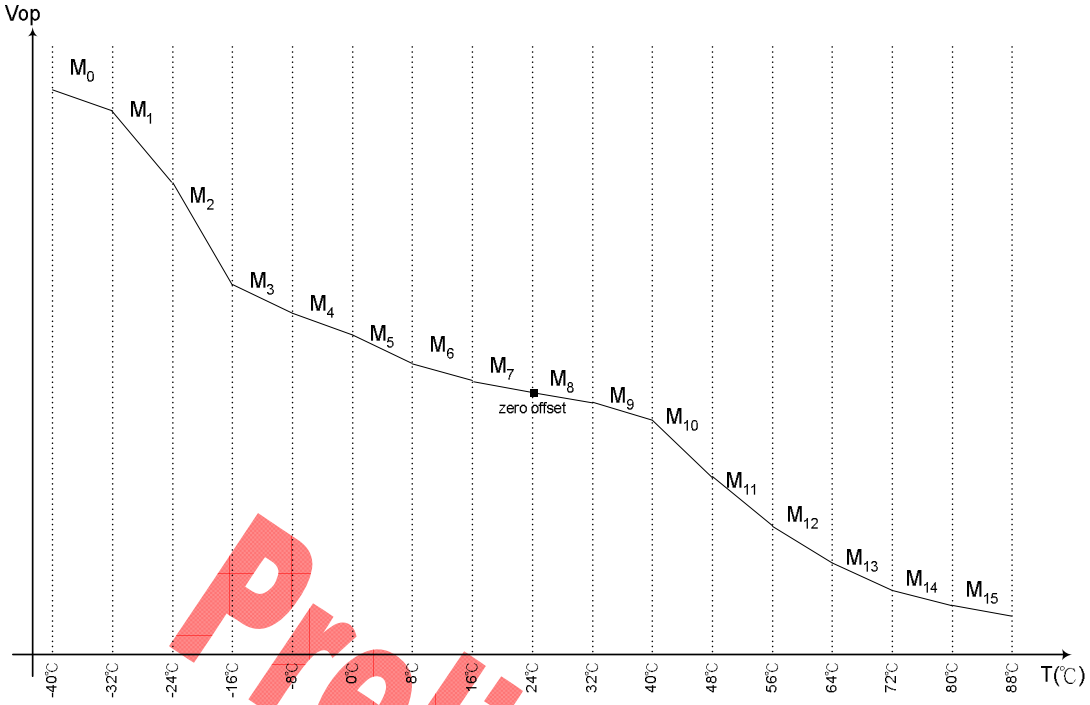



**Figure 7.9-4**

In command TEMPSEL (see section 8.1.62) each MTx, where x=0, 1, 2,..., E, F, has a value between 0 and 15. MTx = 0 results in 0V increment on V0, MTx = 1 results in Mx=5mV increment, ..., MTx = 15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; The relations between Mx and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

| Temperature range | Equation V0(V) at temperature=T℃ |
|---|---|
| -40℃ ≦ T ＜ -32℃ | $V0(T) = V0(T_{24}) + (-32-T) \cdot M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$ |
| -32℃ ≦ T ＜ -24℃ | $V0(T) = V0(T_{24}) + (-24-T) \cdot M1 + (M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$ |
| -24℃ ≦ T ＜ -16℃ | $V0(T) = V0(T_{24}) + (-16-T) \cdot M2 + (M3 + M4 + M5 + M6 + M7) \cdot 8$ |
| -16℃ ≦ T ＜ -8℃ | $V0(T) = V0(T_{24}) + (-8-T) \cdot M3 + (M4 + M5 + M6 + M7) \cdot 8$ |
| -8℃ ≦ T ＜ 0℃ | $V0(T) = V0(T_{24}) + (0-T) \cdot M4 + (M5 + M6 + M7) \cdot 8$ |
| 0℃ ≦ T ＜ 8℃ | $V0(T) = V0(T_{24}) + (8-T) \cdot M5 + (M6 + M7) \cdot 8$ |
| 8℃ ≦ T ＜ 16℃ | $V0(T) = V0(T_{24}) + (16-T) \cdot M6 + M7 \cdot 8$ |
| 16℃ ≦ T ＜ 24℃ | $V0(T) = V0(T_{24}) + (24-T) \cdot M7$ |
| 24℃ ≦ T ＜ 32℃ | $V0(T) = V0(T_{24}) - (T-24) \cdot M8$ |
| 32℃ ≦ T ＜ 40℃ | $V0(T) = V0(T_{24}) - (T-32) \cdot M9 - M8 \cdot 8$ |
| 40℃ ≦ T ＜ 48℃ | $V0(T) = V0(T_{24}) - (T-40) \cdot M10 - (M9 + M8) \cdot 8$ |
| 48℃ ≦ T ＜ 56℃ | $V0(T) = V0(T_{24}) - (T-48) \cdot M11 - (M10 + M9 + M8) \cdot 8$ |
| 56℃ ≦ T ＜ 64℃ | $V0(T) = V0(T_{24}) - (T-56) \cdot M12 - (M11 + M10 + M9 + M8) \cdot 8$ |
| 64℃ ≦ T ＜ 72℃ | $V0(T) = V0(T_{24}) - (T-64) \cdot M13 - (M12 + M11 + M10 + M9 + M8) \cdot 8$ |
| 72℃ ≦ T ＜ 80℃ | $V0(T) = V0(T_{24}) - (T-72) \cdot M14 - (M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$ |
| 80℃ ≦ T ＜ 88℃ | $V0(T) = V0(T_{24}) - (T-80) \cdot M15 - (M14 + M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$ |






**Note:**

**Please make sure to avoid any kind of heating source closing to ST7687s such as back light, to prevent Vop is not anticipatve because of temperature compensate circuit worked.**

#### 7.9.1.3. V0 fine tuning

ST7687S has 2 commands for fine tuning V0. These commands are VopOfsetInc (see section 8.1.43) and VopOfsetDec (see section 8.1.44). When writing VopOfsetInc into IC for each time, V0 would increase 40mV; when writing VopOfsetDec into IC for each time, V0 would decrease 40mV.

Example:

Vop[8:0]=011010010

EV[6:0]=0111111

VopOfsetInc x2

→ V0=3.6 + { 210 + (63-63) } x 0.04 + 0.04x2 =12.08 (V)

### 7.9.2. Voltage Follower Circuits

There is a build-in voltage follower circuits in ST7687S for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/6 to 1/12 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

| LCD bias | Vg | Vm |
|---|---|---|
| 1/N bias | (2/N) x V0 | (1/N) x V0 |

**N=6 to 12**



### 7.9.3. EEPROM Setting Flow

ST7687S provides the Write and Read function to write the electronic control value and built-in resistance ratio into built-in EEPROM, and then read them from it. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

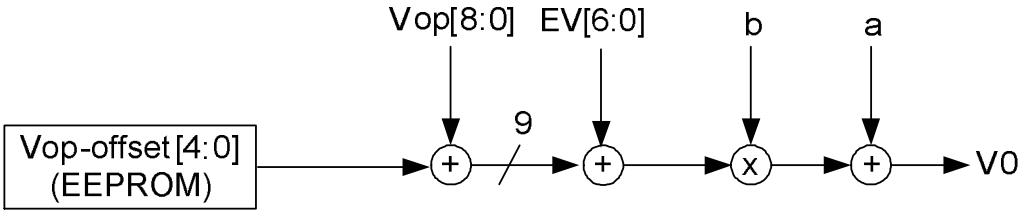



**Figure 7.9-5 V0 value control for different modules by loading EEPROM offset**

*Note1: This setting flow is used for LCM assembler.*

*Note2: EEPROM shouldn't be written without preceding loading correctly from EEPROM in order to avoid some errors during IC operation.*

*Note3: When writing value to EEPROM, the voltage of VPP must be more than 18V (18V~19.8V).*

*Note4: If the EEPROM is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90℃. The data retention guarantee period is specified including the retention period.*

## 7.10 Frquency Temperature Gradient Compensation Coefficient

ST7687S will auto-switch frame rate on different temperature such as Figure 7.10-1. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPRNG(see section 8.1.60). FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL (see section 8.1.57). The frame rate range is from 38.5Hz to 170Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH(℃). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example: TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please take Figure 7.10-1 for reference.



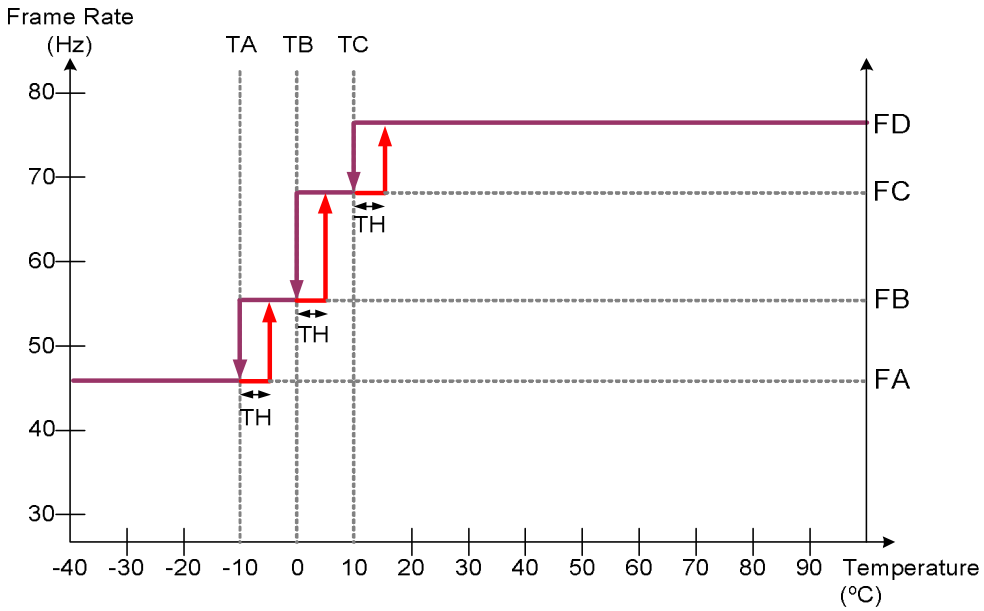



**Figure 7.10-1**

## 7.11 RESET CIRCUIT

The registers that are initialized are listed below.

| Item | After Power On | After Software Reset | After Hardware Reset |
|---|---|---|---|
| Frame memory (RAM data) | Random | No Change | No Change |
| RDDPM | 08h | 08h | 08h |
| RDDMADCTR | 00h | No Change | 00h |
| RDDCOLMOD | 05h (16-Bit/Pixel) | No Change | 05h (16-Bit/Pixel) |
| RDDIM | 00h | 00h | 00h |
| RDDSM | 00h | 00h | 00h |
| Sleep In/Out | In | In | In |
| Display mode (normal/partial) | Normal | Normal | Normal |
| Display Inversion On/Off | Off | Off | Off |
| All Pixel Off mode | Disable | Disable | Disable |
| All Pixel On mode | Disable | Disable | Disable |
| Contrast (EV) | 3Fh | 3Fh | 3Fh |
| Display On/Off | Display Off | Display Off | Display Off |
| Column: Start Address (XS) | 00h | 00h | 00h |
| Column: End Address (XE) | 7Fh | 7Fh (when MV=0/1) | 7Fh |
| Row: Start Address (YS) | 00h | 00h | 00h |
| Row: End Address (YE) | 7Fh | 7Fh (when MV=0/1) | 7Fh |
| Partial: Start Address (PS) | 00h | 00h | 00h |
| Partial: End Address (PE) | 7Fh | 7Fh | 7Fh |
| Scroll: Top Fixed Area (TFA) | 00h | 00h | 00h |
| Scroll: Scroll Area (VSA) | 80h | 80h | 80h |
| Scroll: Bottom Fixed Area | 00h | 00h | 00h |
| Memory Data Access Control MY/MX/MV/ML/RGB) | 0/0/0/0/0 | No Change | 0/0/0/0/0 |
| Scroll Start Address (SSA) | 00h | 00h | 00h |
| Idle Mode On/Off | Off | Off | Off |
| ID | Set by customer | Set by customer | Set by customer |
| Drive Duty | 7Fh | 7Fh | 7Fh |
| First Common | 00h | 00h | 00h |
| FOSC Divider | No division | No division | No division |
| Vop | 0D2h | 0D2h | 0D2h |
| Vop Offset increase/decrease | disable | disable | disable |
| Bias | 1/9 Bias | 1/9 Bias | 1/9 Bias |
| Booster setting | 8x | 8x | 8x |
| Booster Efficiency | 01 | 01 | 01 |
| EEPCIN | 0 | 0 | 0 |
| Frame Frequency in Normal Color (FA/FB/FC/FD) | 48.5Hz/64.6Hz/64.6Hz/77.6Hz | 48.5Hz/64.6Hz/64.6Hz/77.6Hz | 48.5Hz/64.6Hz/64.6Hz/77.6Hz |
| Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D) | 48.5Hz/64.6Hz/64.6Hz/77.6Hz | 48.5Hz/64.6Hz/64.6Hz/77.6Hz | 48.5Hz/64.6Hz/64.6Hz/77.6Hz |
| Temperature Range (TA/TB/TC) | -10℃/0℃/10℃ | -10℃/0℃/10℃ | -10℃/0℃/10℃ |
| Temperature Hysteresis (TH) | 4℃ | 4℃ | 4℃ |

# 8. INSTRUCTIONS

## 8.1 Instruction table

**Command Table**

| Hex | Command | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (00h) | NOP | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No Operation | 8.1.1 |
| (01h) | SWRESET | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Software reset | 8.1.2 |
| (09h) | RDDST | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Read Display Status | 8.1.3 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | ST31 | ST30 | ST29 | ST28 | ST27 | ST26 | ST25 | ST24 | (D31-D24) | |
| - | | 1 | 0 | 1 | ST23 | ST22 | ST21 | ST20 | ST19 | ST18 | ST17 | ST16 | (D23-D16) | |
| - | | 1 | 0 | 1 | ST15 | ST14 | ST13 | ST12 | ST11 | ST10 | ST9 | ST8 | (D15-D8) | |
| - | | 1 | 0 | 1 | ST7 | ST6 | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | (D7-D0) | |
| (0Ah) | RDDPM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Read Display Power Mode | 8.1.4 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | 0 | 0 | - | |
| (0Bh) | RDDMADCTR | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Read Display MADCTR | 8.1.5 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | 0 | 0 | 0 | - | |
| (0Ch) | RDDCOLMOD | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Read Display Pixel Format | 8.1.6 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 | - | |
| (0Dh) | RDDIM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | Read Display Image Mode | 8.1.7 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | D7 | 0 | D5 | D4 | D3 | 0 | 0 | 0 | - | |
| (0Eh) | RDDSM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Read Display signal Mode | 8.1.8 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| (10h) | SLPIN | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Sleep in & booster off | 8.1.9 |
| (11h) | SLPOUT | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Sleep out & booster on | 8.1.10 |
| (12h) | PTLON | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Partial mode on | 8.1.11 |
| (13h) | NORON | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Partial off (Normal) | 8.1.12 |
| (20h) | INVOFF | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Display inversion off (normal) | 8.1.13 |
| (21h) | INVON | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Display inversion on | 8.1.14 |
| (22h) | APOFF | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | All pixel off (Only for test purpose) | 8.1.15 |

## Command Table

| Hex | Command | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (23h) | APON | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | All pixel on (Only for test purpose) | 8.1.16 |
| (25h) | WRCNTR | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Write contrast | 8.1.17 |
| - | | 1 | 1 | 0 | 0 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | EV = 0 to 127 | |
| (28h) | DISPOFF | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Display off | 8.1.18 |
| (29h) | DISPON | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Display on | 8.1.19 |
| (2Ah) | CASET | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Column address set | 8.1.20 |
| | | 1 | 1 | 0 | 0 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 | X_ADR start: 0≦XS≦7Fh | |
| | | 1 | 1 | 0 | 0 | XE6 | XE5 | XE4 | XE3 | XE2 | XE1 | XE0 | X_ADR end: XS≦XE ≦7Fh | |
| (2Bh) | RASET | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Row address set | 8.1.21 |
| | | 1 | 1 | 0 | 0 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 | Y_ADR start: 0≦YS≦7Fh | |
| | | 1 | 1 | 0 | 0 | YE6 | YE5 | YE4 | YE3 | YE2 | YE1 | YE0 | Y_ADR end: YS≦YE≦7Fh | |
| (2Ch) | RAMWR | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Memory write | 8.1.22 |
| | | 1 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data | |
| (2Eh) | RAMRD | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Memory Read | 8.1.23 |
| | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| | | 1 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| (30h) | PTLAR | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Partial start/end address setting | 8.1.24 |
| - | | 1 | 1 | 0 | 0 | PS6 | PS5 | PS4 | PS3 | PS2 | PS1 | PS0 | Start address (0~127) | |
| - | | 1 | 1 | 0 | 0 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | End address (0~127) | |
| (33h) | SCRLAR | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Scroll Area | 8.1.25 |
| - | | 1 | 1 | 0 | 0 | TFA6 | TFA5 | TFA4 | TFA3 | TFA2 | TFA1 | TFA0 | TFA=0~128 | |
| - | | 1 | 1 | 0 | 0 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 | VSA=0~128 | |
| - | | 1 | 1 | 0 | 0 | BFA6 | BFA5 | BFA4 | BFA3 | BFA2 | BFA1 | BFA0 | BFA=0~128 | |
| (34h) | TEOFF | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Tearing effect line off | 8.1.26 |
| (35h) | TEON | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Tearing effect mode set & on | 8.1.27 |
| - | | 1 | 1 | 0 | - | - | - | - | - | - | - | M | “0”: mode1, “1”: mode2 | |
| (36h) | MADCTR | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Memory data access control | 8.1.28 |
| - | | 1 | 1 | 0 | MY | MX | MV | ML | RGB | - | - | - | - | |
| (37h) | VSCSAD | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Scroll start address of RAM | 8.1.29 |
| | | 1 | 1 | 0 | 0 | SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSA0 | SSA = 0~128 | |
| (38h) | IDMOFF | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | Idle mode off | 8.1.30 |
| (39h) | IDMON | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Idle mode on | 8.1.31 |

## Command Table

| Hex | Command | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **(3Ah)** | COLMOD | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Interface pixel format | 8.1.32 |
| - | | 1 | 1 | 0 | - | - | - | - | - | P2 | P1 | P0 | Interface format | |
| **(DAh)** | RDID | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Read ID | 8.1.33 |
| - | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy read | |
| - | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ID1 | ID0 | (D1-D0) | |
| **(B0h)** | DutySet | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Display Duty setting | 8.1.34 |
| | | 1 | 1 | 0 | Du7 | Du6 | Du5 | Du4 | Du3 | Du2 | Du1 | Du0 | | |
| **(B1h)** | FirstCom | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | First Com. Page address | 8.1.35 |
| | | 1 | 1 | 0 | -- | F6 | F5 | F4 | F3 | F2 | F1 | F0 | | |
| **(B3h)** | OscDiv | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | FOSC divider | 8.1.36 |
| | | 1 | 1 | 0 | - | - | - | - | - | - | CLD1 | CLD0 | | |
| **(B5h)** | NLInvSet | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | N-line control | 8.1.37 |
| | | 1 | 1 | 0 | M | 0 | 0 | N4 | N3 | N2 | N1 | N0 | | |
| **(B7h)** | ComScanDir | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Com/Seg Scan Direction for Glass layout | 8.1.38 |
| | | 1 | 1 | 0 | 0 | SMX | 0 | 0 | SBGR | 0 | 0 | 0 | | |
| **(B8h)** | RmwIn | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | read modify write control IN | 8.1.39 |
| **(B9h)** | RmwOut | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | read modify write control Out | 8.1.40 |
| **(BDh)** | DispCompStep | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | Display Compensation Step | 8.1.41 |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Step2 | Step1 | Step0 | | |
| **(C0h)** | VopSet | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Vop setting | 8.1.42 |
| | | 1 | 1 | 0 | Vop7 | Vop6 | Vop5 | Vop4 | Vop3 | Vop2 | Vop1 | Vop0 | | |
| | | 1 | 1 | 0 | - | - | - | - | - | - | - | Vop8 | | |
| **(C1h)** | VopOfsetInc | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | +40mv/setp | 8.1.43 |
| **(C2h)** | VopOfsetDec | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | -40mv/setp | 8.1.44 |
| **(C3h)** | BiasSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Bias selection | 8.1.45 |
| | | 1 | 1 | 0 | - | - | - | - | - | Bias2 | Bias1 | Bias0 | | |
| **(C4h)** | BstBmpXSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Booster setting | 8.1.46 |
| | | 1 | 1 | 0 | - | - | - | - | - | BST2 | BST 1 | BST0 | | |
| **(C5h)** | BstEffSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Booster efficiency selection | 8.1.47 |
| | | 1 | 1 | 0 | - | - | - | - | - | - | BTF1 | BTF0 | | |
| **(CBh)** | VgSorcSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | FV3 with Booster x2 control | 8.1.48 |
| | | 1 | 1 | 0 | - | - | - | - | - | - | - | 2BT0 | | |
| **(CCh)** | IDSet | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | ID setting | 8.1.49 |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ID1 | ID0 | | |

## Command Table

| Hex | Command | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (D0h) | ANASET | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Analog circuit setting | 8.1.50 |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | | |
| (D7h) | AutoLoadSet | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | EEPROM data auto re-load control | 8.1.51 |
| | | 1 | 1 | 0 | 1 | 0 | - | ARD | 1 | 1 | 1 | 1 | | |
| (DEh) | RDTstStatus | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | read IC status | 8.1.52 |
| | | 1 | 0 | 1 | - | - | - | - | - | - | - | - | Dummy Read | |
| | | 1 | 0 | 1 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | | |
| (E0h) | EEPCIN | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | EEPROM control in | 8.1.53 |
| | | 1 | 1 | 0 | 0 | 0 | 0 | WR/ERS/RD | 0 | 0 | 0 | 0 | | |
| (E1h) | EEPCOUT | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | EEPROM control out | 8.1.54 |
| (E2h) | EEPWR | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Write to EEPROM | 8.1.55 |
| (E3h) | EEPRD | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Read from EEPROM | 8.1.56 |
| (E5h) | ROMSET | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Programmable rom setting | 8.1.57 |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | | |
| (F0h) | FRMSEL | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Frame Freq. in Temp range A,B,C and D | 8.1.58 |
| | | 1 | 1 | 0 | - | - | - | DIVA | FA3 | FA2 | FA1 | FA0 | | |
| | | 1 | 1 | 0 | - | - | - | DIVB | FB3 | FB2 | FB1 | FB0 | | |
| | | 1 | 1 | 0 | - | - | - | DIVC | FC3 | FC2 | FC1 | FC0 | | |
| | | 1 | 1 | 0 | - | - | - | DIVD | FD3 | FD2 | FD1 | FD0 | | |
| (F1h) | FRM8SEL | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Frame Freq. in Temp range A,B,C and D (idle) | 8.1.59 |
| | | 1 | 1 | 0 | - | - | - | F8A4 | F8A3 | F8A2 | F8A1 | F8A0 | | |
| | | 1 | 1 | 0 | - | - | - | F8B4 | F8B3 | F8B2 | F8B1 | F8B0 | | |
| | | 1 | 1 | 0 | - | - | - | F8C4 | F8C3 | F8C2 | F8C1 | F8C0 | | |
| | | 1 | 1 | 0 | - | - | - | F8D4 | F8D3 | F8D2 | F8D1 | F8D0 | | |
| (F2h) | TMPRNG | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Temp range A,B and C | 8.1.60 |
| | | 1 | 1 | 0 | - | TA6 | TA5 | TA4 | TA3 | TA2 | TA1 | TA0 | | |
| | | 1 | 1 | 0 | - | TB6 | TB5 | TB4 | TB3 | TB2 | TB1 | TB0 | | |
| | | 1 | 1 | 0 | - | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 | | |
| (F3h) | TMPHYS | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | Hysteresis value set | 8.1.61 |
| | | 1 | 1 | 0 | - | - | - | - | TH3 | TH2 | TH1 | TH0 | | |
| (F4h) | TEMPSEL | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | TEMPSEL | 8.1.62 |

## Command Table

| Hex | Command | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 1 | 0 | MT13 | MT12 | MT11 | MT10 | MT03 | MT02 | MT01 | MT00 | | |
| | | 1 | 1 | 0 | MT33 | MT32 | MT31 | MT30 | MT23 | MT22 | MT21 | MT20 | | |
| | | 1 | 1 | 0 | MT53 | MT52 | MT51 | MT50 | MT43 | MT42 | MT41 | MT40 | | |
| | | 1 | 1 | 0 | MT73 | MT72 | MT71 | MT70 | MT63 | MT62 | MT61 | MT60 | | |
| | | 1 | 1 | 0 | MT93 | MT92 | MT91 | MT90 | MT83 | MT82 | MT81 | MT80 | | |
| | | 1 | 1 | 0 | MTB3 | MTB2 | MTB1 | MTB0 | MTA3 | MTA2 | MTA1 | MTA0 | | |
| | | 1 | 1 | 0 | MTD3 | MTD2 | MTD1 | MTD0 | MTC3 | MTC2 | MTC1 | MTC0 | | |
| | | 1 | 1 | 0 | MTF3 | MTF2 | MTF1 | MTF0 | MTE3 | MTE2 | MTE1 | MTE0 | | |
| **(F7h)** | THYS | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | Temperature detection threshold | 8.1.63 |
| | | 1 | 1 | 0 | THYS7 | THYS6 | THYS5 | THYS4 | THYS3 | THYS2 | THYS1 | THYS0 | | |
| **(F9h)** | Frame Set | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | Set Frame RGB value | 8.1.64 |
| | | 1 | 1 | 0 | - | - | - | P14 | P13 | P12 | P11 | P10 | | |
| | | 1 | 1 | 0 | - | - | - | P24 | P23 | P22 | P21 | P20 | | |
| | | : | : | : | : | : | : | : | : | : | : | : | | |
| | | 1 | 1 | 0 | - | - | - | P154 | P153 | P152 | P151 | P150 | | |
| | | 1 | 1 | 0 | - | - | - | P164 | P163 | P162 | P161 | P160 | | |
| **(FAh)** | EEPANFSEL | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | EEPROM function selection | 8.1.65 |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | - | ERAE | WRE | - | | |
| **(FBh)** | EEPERS | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | Erase EEPROM | 8.1.66 |



*Note:*

*During Sleep In mode, these commands are updated immediately.*

*Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode*

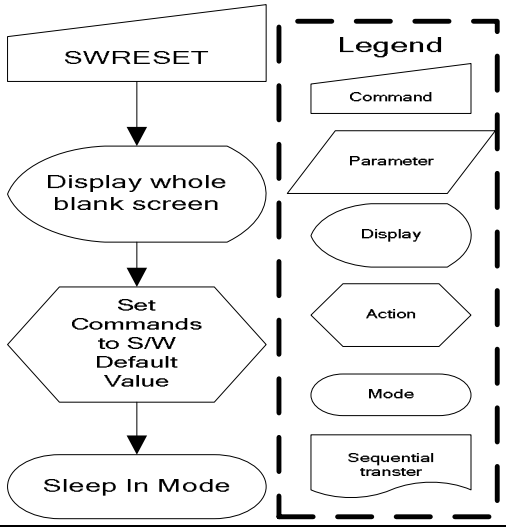
### 8.1.1. NOP (00h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NOP | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **(00h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command is an empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands. |
| Restriction | - |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / N/A<br>S/W Reset / N/A<br>H/W Reset / N/A |
| Flow Chart | - |

### 8.1.2. SWRESET: Software Reset (01h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SWRESET | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **(01h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to Vm (display off: blank display). (See default tables in each command description)<br>*Note: The Frame Memory contents are not affected by this command.* |
| Restriction | It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.<br>Software Reset command cannot be sent during Sleep Out sequence. |
| Register Availability | Status: Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status: Default Value<br>Power On Sequence: N/A<br>S/W Reset: N/A<br>H/W Reset: N/A |
| Flow Chart |  |

### 8.1.3. RDDST: Read Display Status (09h)

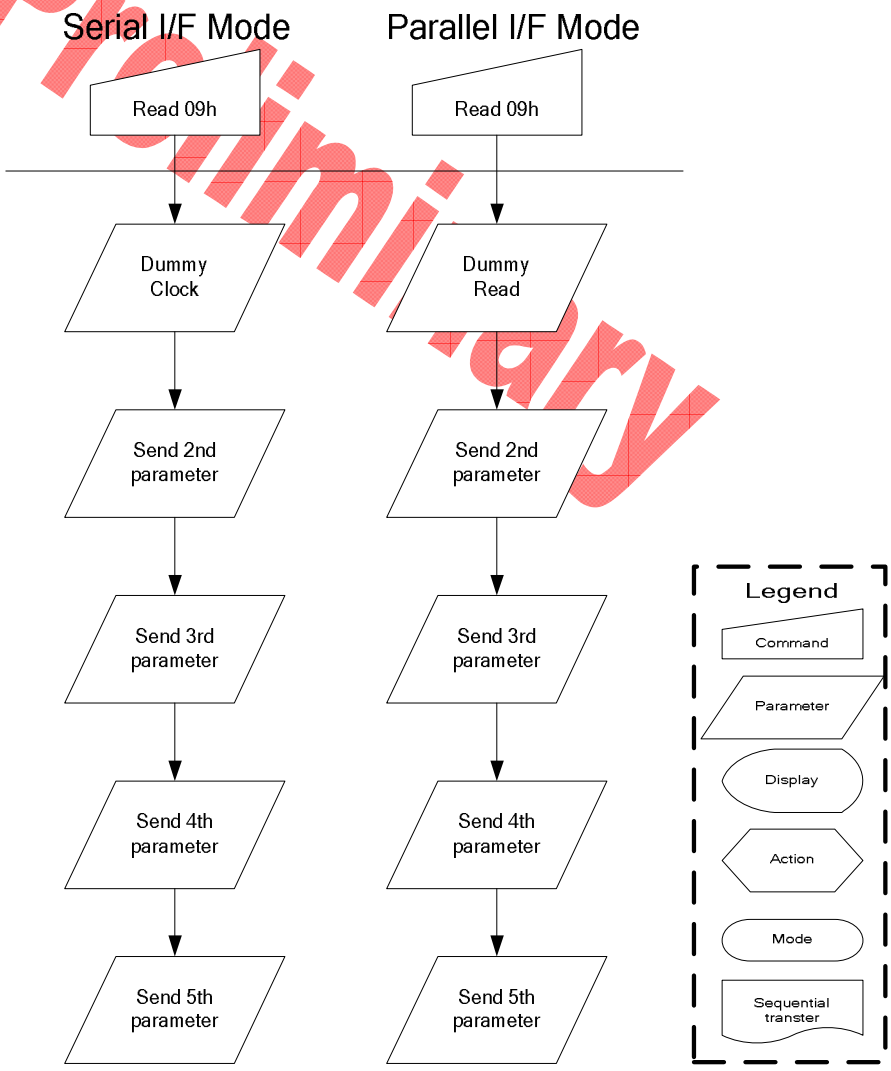
| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDDST | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | **(09h)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | ST31 | ST30 | ST29 | ST28 | ST27 | ST26 | ST25 | ST24 | - |
| 3rd parameter | 1 | 0 | 1 | ST23 | ST22 | ST21 | ST20 | ST19 | ST18 | ST17 | ST16 | - |
| 4th parameter | 1 | 0 | 1 | ST15 | ST14 | ST13 | ST12 | ST11 | ST10 | ST9 | ST8 | - |
| 5th parameter | 1 | 0 | 1 | ST7 | ST6 | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | - |

*NOTE: "-" Don't care*

Description

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| ST31 | Booster Voltage Status | "1"=Booster on, "0"=off |
| ST30 | Row Address Order (MY) | "1"=Decrement, "0"=Increment |
| ST29 | Column Address Order (MX) | "1"=Decrement, "0"=Increment |
| ST28 | Row/Column Order (MV) | "1"= Row/column exchange (MV=1)<br>"0"= Normal (MV=0) |
| ST27 | Scan Address Order (ML) | "1"=Decrement, "0"=Increment |
| ST26 | RGB/BGR Order (RGB) | "1"=BGR, "0"=RGB |
| ST25 | Not Used | "0" |
| ST24 | Not Used | "0" |
| ST23 | Not Used | "0" |
| ST22 | Interface Color Pixel Format Definition | "101" = 16-bit / pixel, |
| ST21 | | |
| ST20 | | |
| ST19 | Idle Mode On/Off | "1" = On, "0" = Off |
| ST18 | Partial Mode On/Off | "1" = On, "0" = Off |
| ST17 | Sleep In/Out | "1" = Out, "0" = In |
| ST16 | Display Normal Mode On/Off | "1" = Normal Display, "0" = Partial Display |
| ST15 | Vertical Scrolling Status | "1" = Scroll on, "0" = Scroll off |
| ST14 | Not Used | "0" |
| ST13 | Inversion Status | "1" = On, "0" = Off |
| ST12 | All Pixels On | "1" = all pixal on, "0" = normal display |
| ST11 | All Pixels Off | "1" = all pixal off, "0" = normal display |
| ST10 | Display On/Off | "1" = On, "0" = Off |
| ST9 | Tearing effect line on/off | "1" = On, "0" = Off |
| ST8 | Not Used | "0" |
| ST7 | Not Used | "0" |
| ST6 | Not Used | "0" |
| ST5 | Tearing effect line mode | "0" = mode1, "1" = mode2 |
| ST4 | Not Used | "0" |
| ST3 | Not Used | "0" |
| ST2 | Not Used | "0" |
| ST1 | Not Used | "0" |
| ST0 | Not Used | "0" |

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value (ST[31:0])</td></tr>
<tr><td>Power On Sequence</td><td>0000 0000_0101 0001_0000 0000_0000 0000</td></tr>
<tr><td>S/W Reset</td><td>0xxx xx00_0xxx 0001_0000 0000_0000 0000</td></tr>
<tr><td>H/W Reset</td><td>0000 0000_0101 0001_0000 0000_0000 0000</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

### 8.1.4. RDDPM: Read Display Power Mode (0Ah)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDDPM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | **(0Ah)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | 0 | 0 | - |

*NOTE: "-" Don't care*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| D7 | Booster Voltage Status | "1"=Booster on, "0"=Booster off |
| D6 | Idle Mode On/Off | "1" = Idle Mode On, "0" = Idle Mode Off |
| D5 | Partial Mode On/Off | "1" = Partial Mode On, "0" = Partial Mode |
| D4 | Sleep In/Out | "1" = Sleep Out, "0" = Sleep In |
| D3 | Display Normal Mode On/Off | "1" = Normal Display, "0" = Partial Display |
| D2 | Display On/Off | "1" = Display On, "0" = Display Off |
| D1 | Not Used | "0" |
| D0 | Not Used | "0" |

**Restriction**

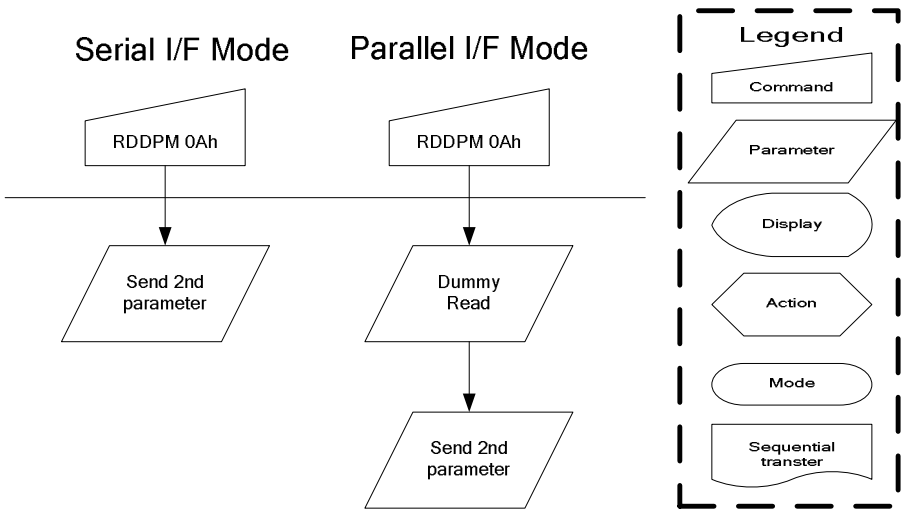
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D[7:0]) |
|---|---|
| Power On Sequence | 00001000b (08h) |
| S/W Reset | 00001000b (08h) |
| H/W Reset | 00001000b (08h) |

**Flow Chart**



### 8.1.5. RDDMADCTR: Read Display MADCTR (0Bh)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDDMADCTR | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | **(0Bh)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | 0 | 0 | 0 | - |

*NOTE: "-" Don't care*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| D7 | Row Address Order (MY) | "1"=Decrement, "0"=Increment |
| D6 | Column Address Order (MX) | "1"=Decrement, "0"=Increment |
| D5 | Row/Column Order (MV) | "1"= Row/column exchange (MV=1)<br>"0"= Normal (MV=0) |
| D4 | Scan Address Order (ML) | "1"=Decrement, "0"=Increment |
| D3 | RGB/BGR Order (RGB) | "1"=BGR, "0"=RGB |
| D2 | Not Used | "0" |
| D1 | Not Used | "0" |
| D0 | Not Used | "0" |

**Restriction**

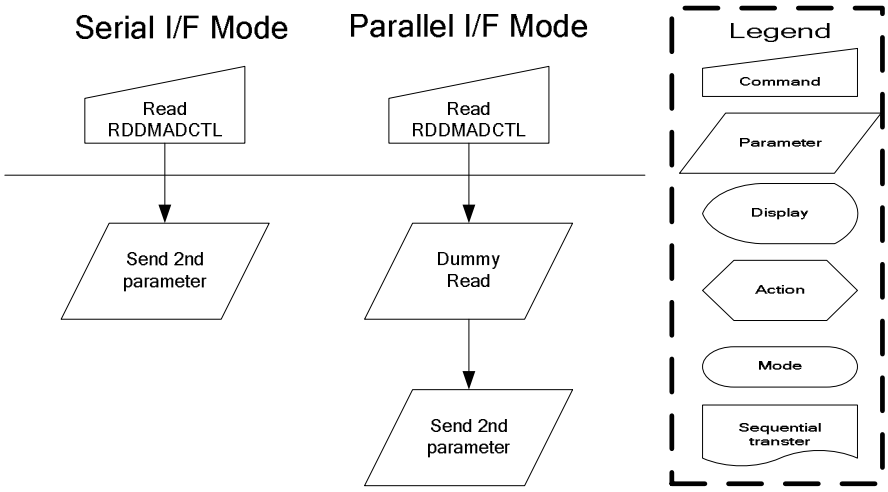
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D[7:0]) |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | No change |
| H/W Reset | 00h |

**Flow Chart**



### 8.1.6. RDDCOLMOD: Read Display Pixel Format (0Ch)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDDCOLMOD | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | **(0Ch)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 | - |

*NOTE: "-" Don't care*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| D7 | RGB Interface Color Format | "0" (Not Used) |
| D6 | | "0" (Not Used) |
| D5 | | "0" (Not Used) |
| D4 | | "0" (Not Used) |
| D3 | Control Interface Color Format | "0" |
| D2 | | "011"=12 bit/pixel (type A)<br>"100"=12 bit/pixel (type B)<br>"101"=16 bit/pixel |
| D1 | | |
| D0 | | |

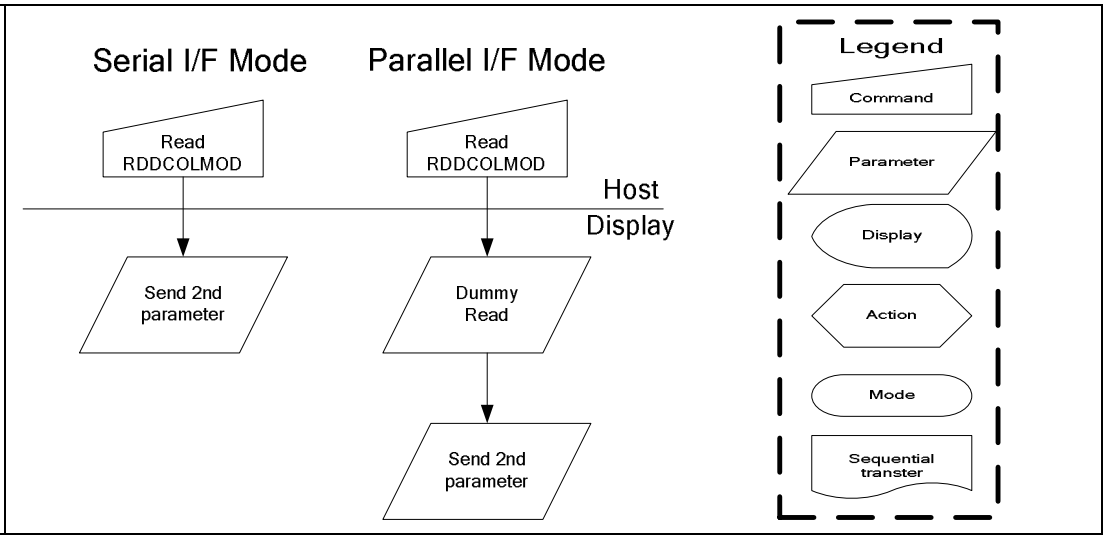
**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D[2:0]) |
|---|---|
| Power On Sequence | 16 bit/pixel |
| S/W Reset | No change |
| H/W Reset | 16 bit/pixel |

| | |
|---|---|
| Flow Chart |  |

### 8.1.7. RDDIM: Read Display Image Mode (0Dh)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDDIM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | **(0Dh)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | D7 | 0 | D5 | D4 | D3 | 0 | 0 | 0 | - |

*NOTE: "-" Don't care*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| D7 | Vertical Scrolling On/Off | "1" = Vertical scrolling is On,<br>"0" = Vertical scrolling is Off, |
| D6 | Not Used | "0" |
| D5 | Inversion On/Off | "1" = Inversion is On, "0" = Inversion is Off |
| D4 | All Pixels On | "1" = All Pixels On, "0" = Normal Mode |
| D3 | All Pixels Off | "1" = All Pixels Off, "0" = Normal Mode |
| D2 | Not Used | "0" |
| D1 | | "0" |
| D0 | | "0" |

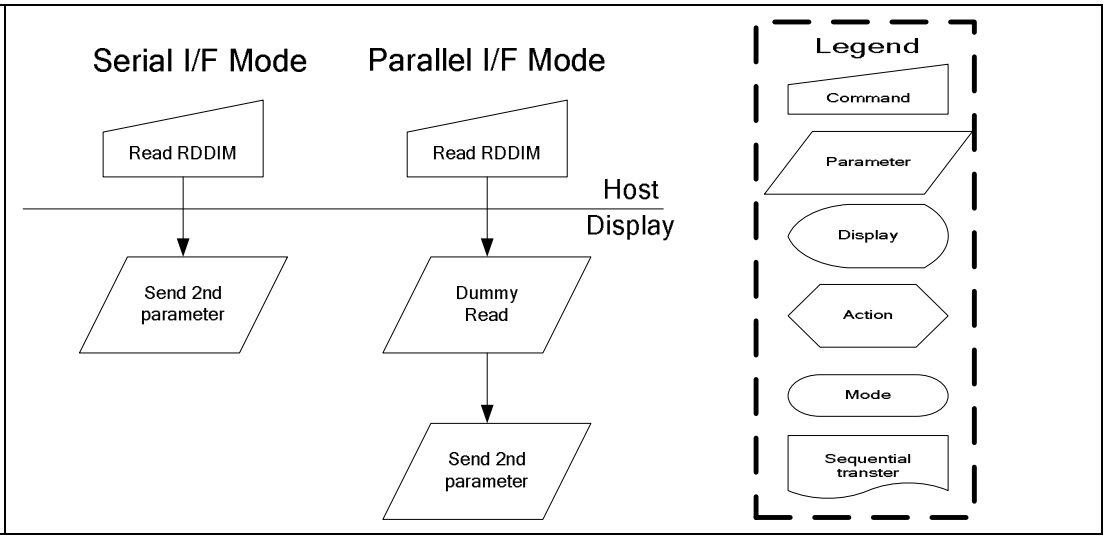
**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D[7:0]) |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

| | |
|---|---|
| Flow Chart |  |

### 8.1.8. RDDSM: Read Display Signal Mode (0Eh)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDDSM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | **(0Eh)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | - |

*NOTE: "-" Don't care*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| D7 | Tearing Effect Line On/Off | "1" = On, "0" = Off |
| D6 | Tearing effect line mode | "0" = mode1, "1" = mode2 |
| D5 | Not Used | "0" |
| D4 | Not Used | "0" |
| D3 | Not Used | "0" |
| D2 | Not Used | "0" |
| D1 | Not Used | "0" |
| D0 | Not Used | "0" |

**Restriction**

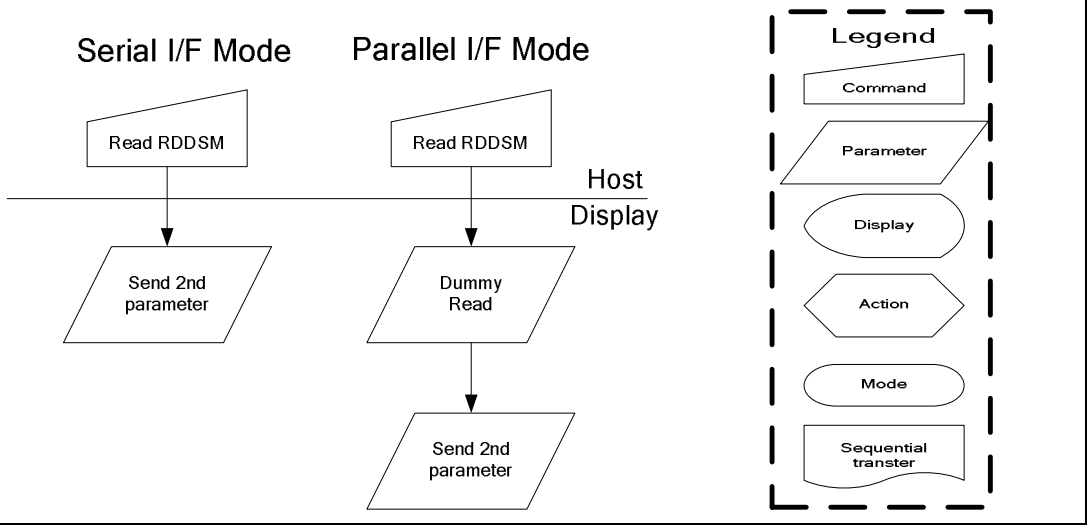
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

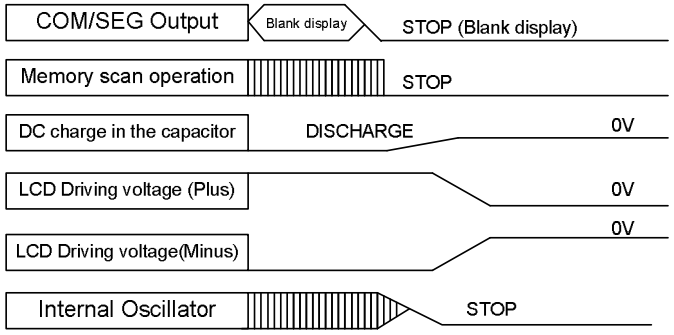
| Status | Default Value (D[7:0]) |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

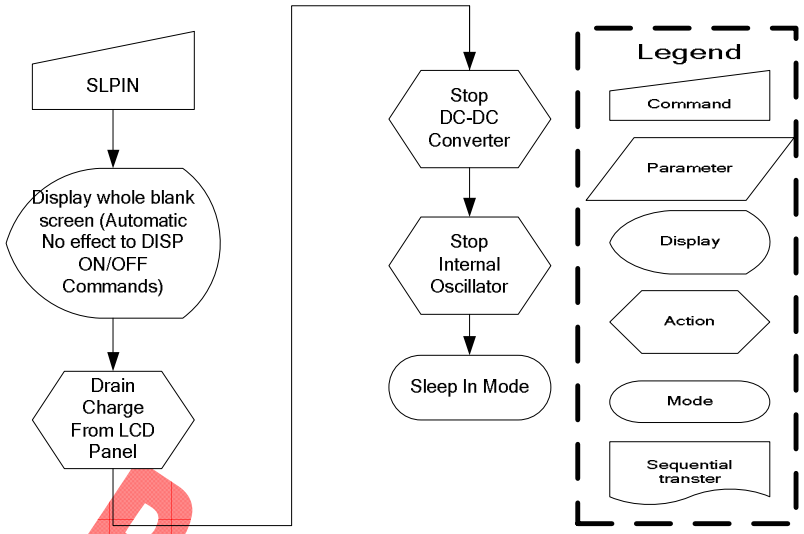


### 8.1.9. SLPIN: Sleep In (10h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SLPIN | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | **(10h)** |
| Parameter | No Parameter | | | | | | | | | | | |

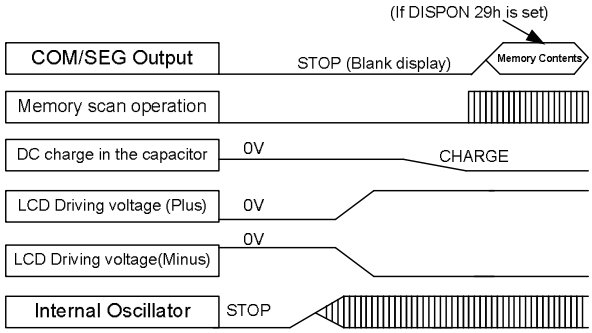
| | |
|---|---|
| Description | This command causes the LCD module to enter the minimum power consumption mode.<br>In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.<br>  <br><br>MCU interface and memory are still working and the memory keeps its contents |
| Restriction | This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).<br>It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. |
| Register Availability | Status: Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status: Default Value<br>Power On Sequence: Sleep in mode<br>S/W Reset: Sleep in mode<br>H/W Reset: Sleep in mode |

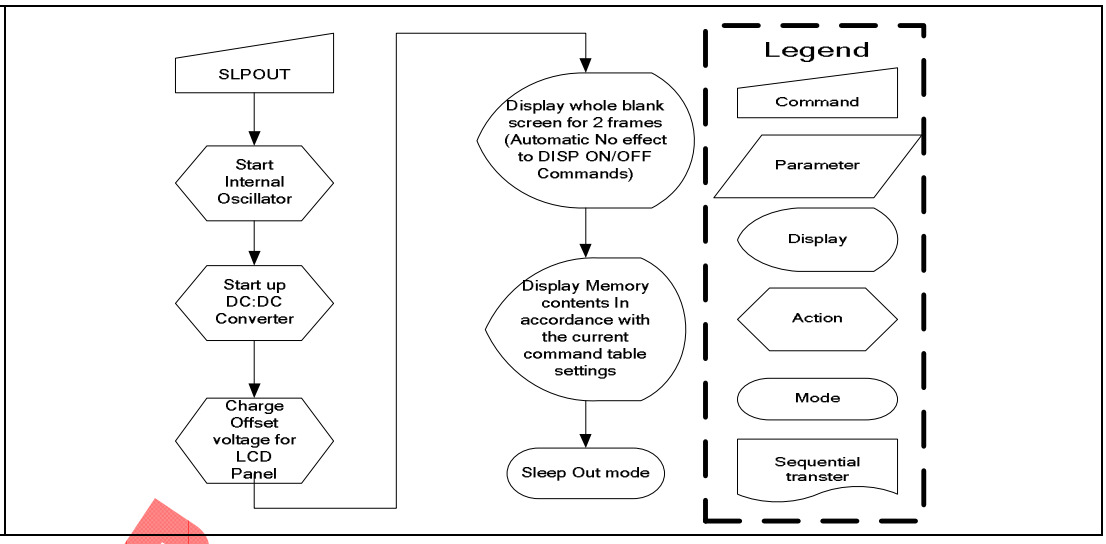
| Flow Chart | |
|---|---|



### 8.1.10. SLPOUT: Sleep Out (11h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SLPOUT | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | **(11h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.<br>  <br> |
| Restriction | This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).<br>It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize.<br>The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / Sleep in mode<br>S/W Reset / Sleep in mode<br>H/W Reset / Sleep in mode |

| Flow Chart |  |
|---|---|

### 8.1.11. PTLON: Partial Display Mode On (12h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLON | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | **(12h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H)<br>Exit from PTLON by Normal Display Mode On command (13H)<br>There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On. |
| Restriction | This command has no effect when Partial mode is active. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / Partial mode off<br>S/W Reset / Partial mode off<br>H/W Reset / Partial mode off |
| Flow Chart | See Partial Area (30h) |

### 8.1.12. NORON: Normal Display Mode On (13h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NORON | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | **(13h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command returns the display to normal mode.<br>Normal display mode on means Partial mode off, Scroll mode Off.<br>Exit from NORON by the Partial mode On command (12h)<br>There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On. |
| Restriction | This command has no effect when Normal Display mode is active. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / Normal Mode On<br>S/W Reset / Normal Mode On<br>H/W Reset / Normal Mode On |
| Flow Chart | See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command |

### 8.1.13. INVOFF: Display Inversion Off (20h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INVOFF | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **(20h)** |
| Parameter | No Parameter | | | | | | | | | | | |

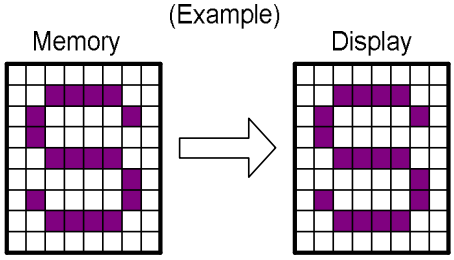
**Description**

This command is used to recover from display inversion mode.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)




**Restriction**

This command has no effect when module is already inversion off mode.

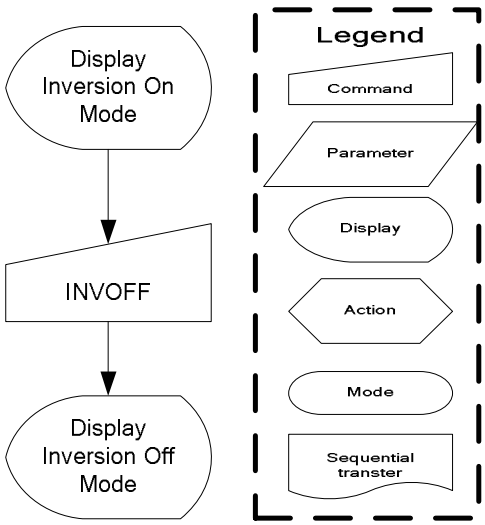
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| S/W Reset | Display Inversion off |
| H/W Reset | Display Inversion off |

**Flow Chart**



### 8.1.14. INVON: Display Inversion On (21h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INVON | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | **(21h)** |
| Parameter | No Parameter | | | | | | | | | | | |

**Description**

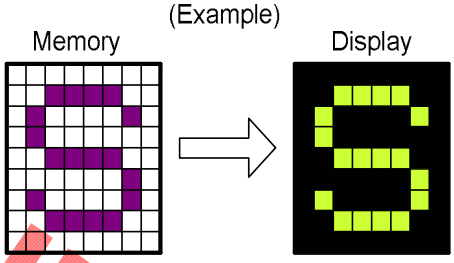
This command is used to enter into display inversion mode

This command makes no change of contents of frame memory.

This command does not change any other status.

To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)






**Restriction**

This command has no effect when module is already Inversion On mode.

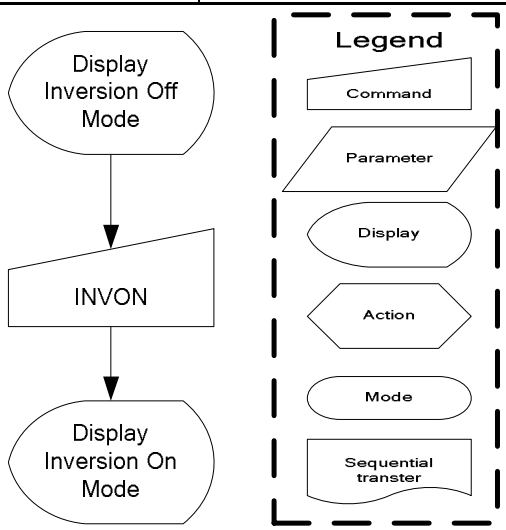
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

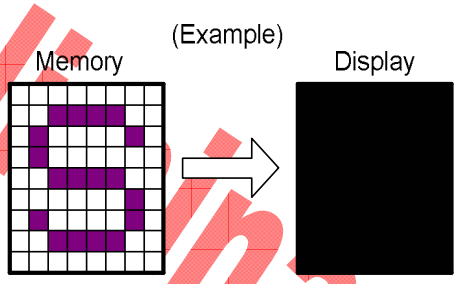
| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| S/W Reset | Display Inversion off |
| H/W Reset | Display Inversion off |

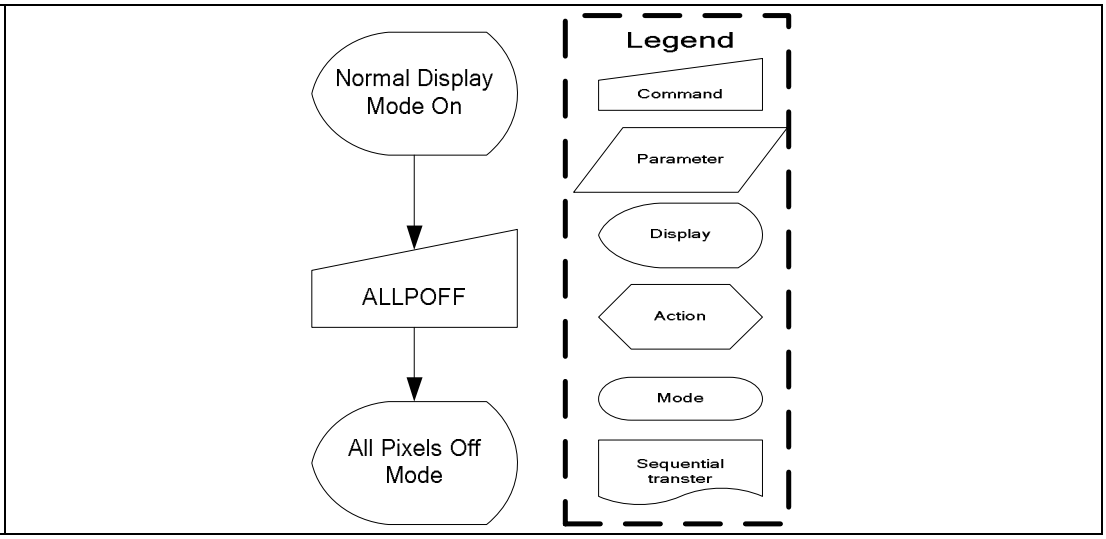
**Flow Chart**



### 8.1.15. APOFF: All Pixels Off (22h) (Only for Test Purposes)

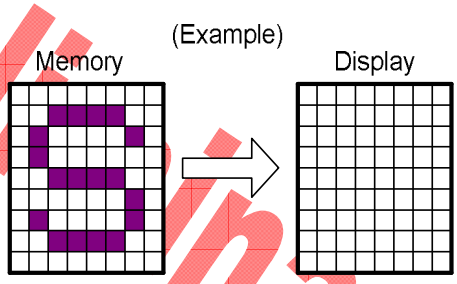
| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APOFF | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | **(22h)** |
| Parameter | No Parameter | | | | | | | | | | | |

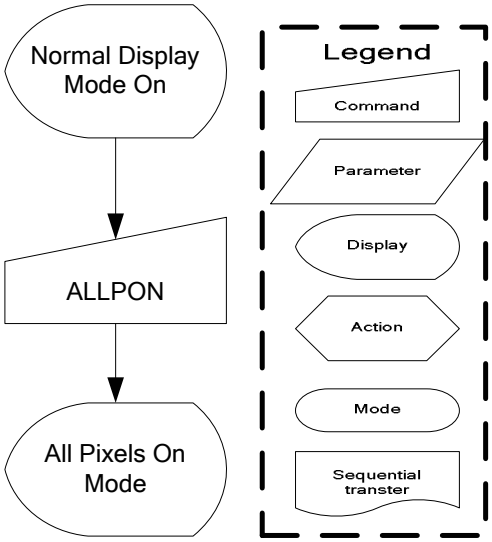
| | |
|---|---|
| Description | This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.<br>All driver outputs become “Low” data state and display becomes black.<br>This command makes no change of contents of display memory.<br>This command does not change any other status.<br>Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.<br>The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.<br>  |
| Restriction | This command has no effect when module is already All Pixel Off mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / All pixel off mode disable<br>S/W Reset / All pixel off mode disable<br>H/W Reset / All pixel off mode disable |

| | |
|---|---|
| Flow Chart |  |

### 8.1.16. APON: All Pixels On (23h) (Only for Test Purposes)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APON | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | **(23h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.<br>All driver outputs become “High” data state and display becomes white.<br>This command makes no change of contents of display memory.<br>This command does not change any other status.<br>Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.<br>The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.<br>  |
| Restriction | This command has no effect when module is already All Pixel On mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / All pixel on mode disable<br>S/W Reset / All pixel on mode disable<br>H/W Reset / All pixel on mode disable |

| | |
|---|---|
| Flow Chart |  |

### 8.1.17. WRCNTR: Write Contrast (25h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRCNTR | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | **(25h)** |
| Parameter | 1 | 1 | 0 | 0 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | |

| | |
|---|---|
| Description | This command is used to fine tuning the contrast of the display. Parameter range is 00~7Fh. The contrast is not linear but the contrast adjustment is linear. Luminance is increasing from 00h to 7Fh. 00h is presenting dark end and 7Fh is presenting bright end. |
| Restriction | - |

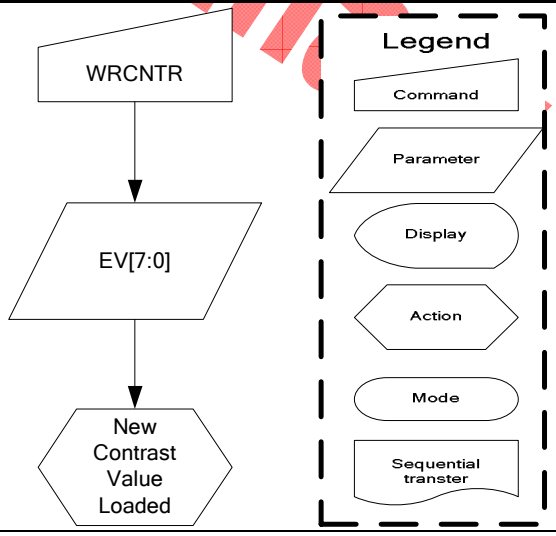
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

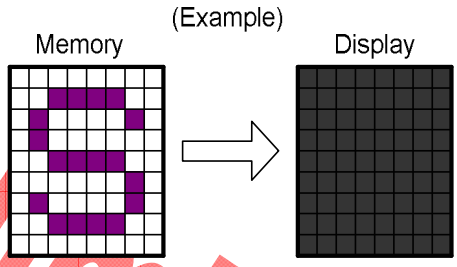
| Status | Default Value |
|---|---|
| Power On Sequence | 3Fh |
| S/W Reset | 3Fh |
| H/W Reset | 3Fh |

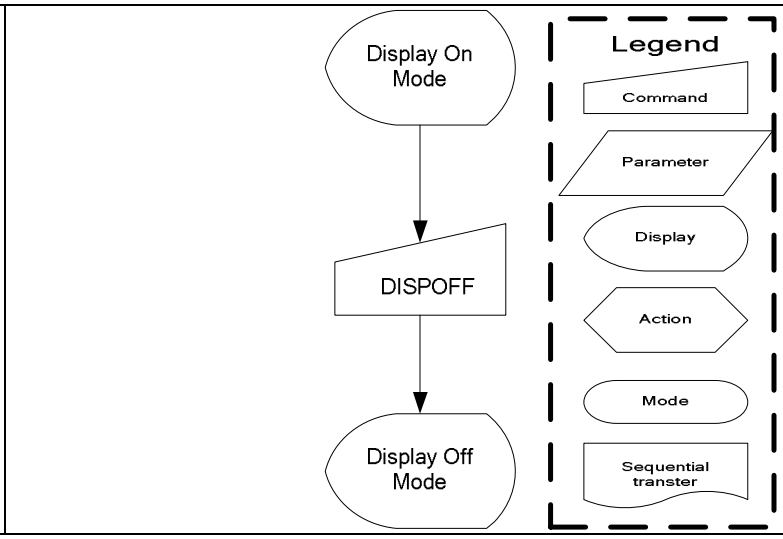
Flow Chart



### 8.1.18. DISPOFF: Display Off (28h)

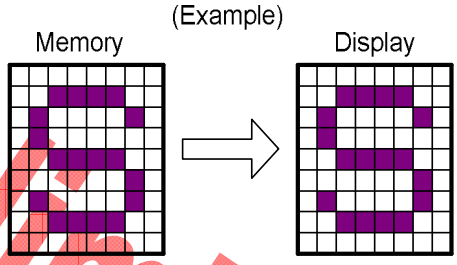
| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DISPOFF | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | **(28h)** |
| Parameter | No Parameter | | | | | | | | | | | |

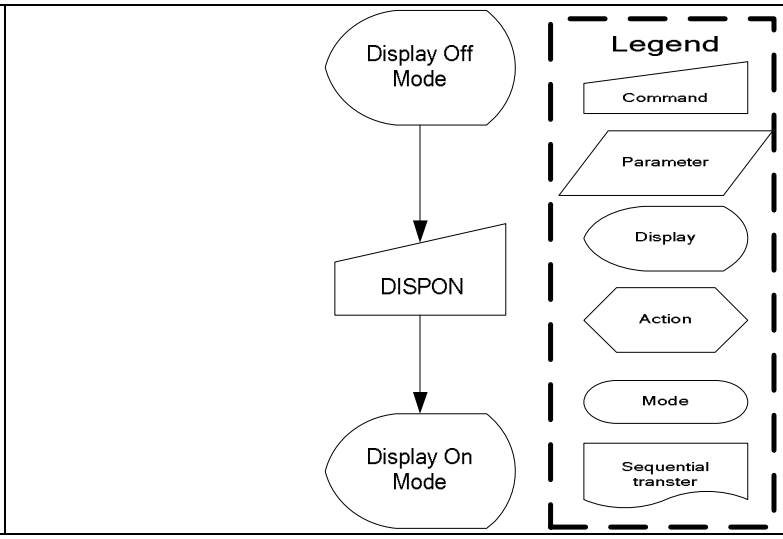
| | |
|---|---|
| Description | This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory disables and blank page inserted.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>There will be no abnormal visible effect on the display.<br>Exit from this command by Display On (29h)<br>  |
| Restriction | This command has no effect when module is already in Display Off mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / Display off<br>S/W Reset / Display off<br>H/W Reset / Display off |

| | |
|---|---|
| Flow Chart |  |

### 8.1.19. DISPON: Display On (29h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DISPON | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | **(29h)** |
| Parameter | No Parameter | | | | | | | | | | | |

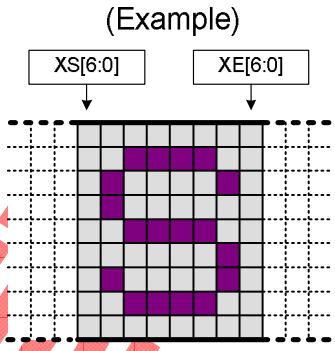
| | |
|---|---|
| Description | Turn on the display screen according to the current display data RAM content and the display timing and setting.<br>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>  |
| Restriction | This command has no effect when module is already in Display On mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / Display off<br>S/W Reset / Display off<br>H/W Reset / Display off |

| | |
|---|---|
| Flow Chart |  |

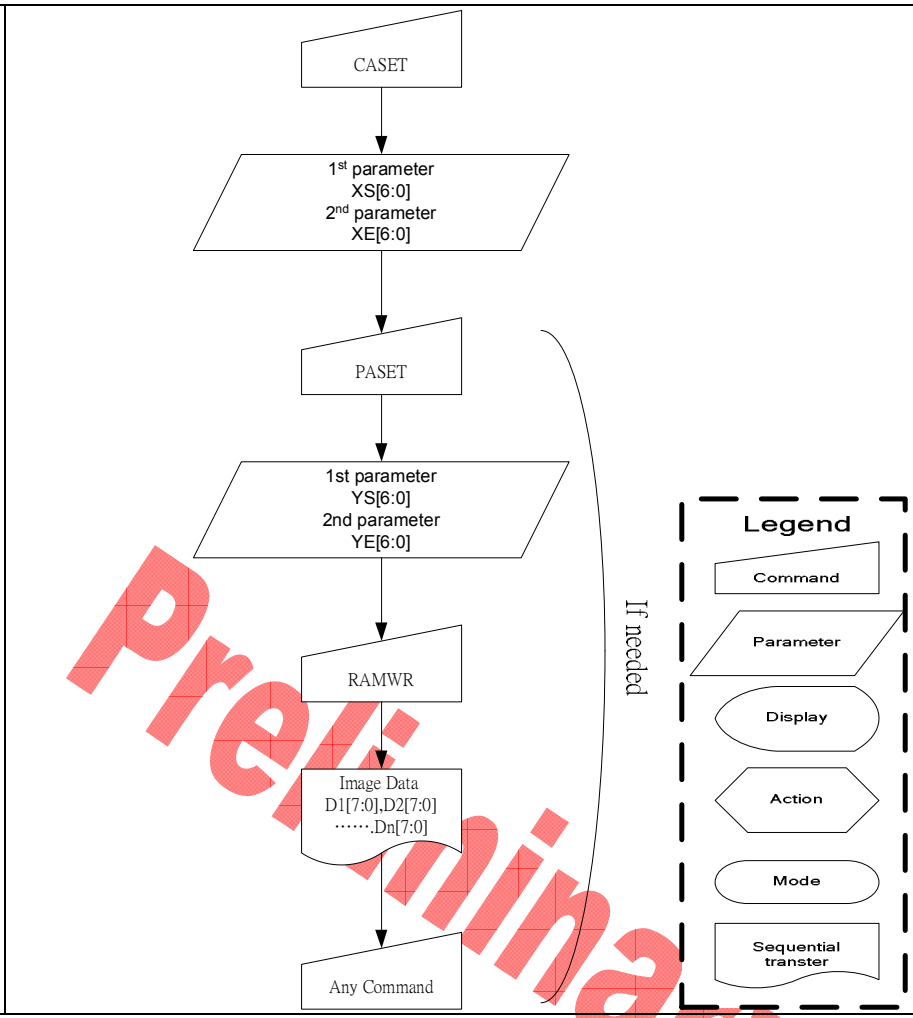
### 8.1.20. CASET: Column Address Set (2Ah)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CASET | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | **(2Ah)** |
| 1st Parameter | 1 | 1 | 0 | 0 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 | |
| 2nd Parameter | 1 | 1 | 0 | 0 | XE6 | XE5 | XE4 | XE3 | XE2 | XE1 | XE0 | |

*NOTE: "-" Don't care*

<table>
<tr><td>Description</td><td>This command is used to define area of frame memory where MCU can access.<br>This command makes no change on the other driver status.<br>The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.<br>Each value represents one column line in the Frame Memory.<br> 
</td></tr>
<tr><td>Restriction</td><td>XS [6:0] always must be equal to or less than XE [6:0]<br>When XS [6:0] or XE [6:0] is greater than 7Fh, data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td rowspan="2">Status</td><td colspan="2">Default Value</td></tr>
<tr><td>XS [6:0]</td><td>XE [6:0]</td></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>7Fh</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>7Fh</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>7Fh</td></tr>
</table>
</td></tr>
</table>

Flow Chart



### 8.1.21. RASET: Row Address Set (2Bh)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RASET | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | **(2Bh)** |
| 1st Parameter | 1 | 1 | 0 | 0 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 | |
| 2nd Parameter | 1 | 1 | 0 | 0 | YE6 | YE5 | YE4 | YE3 | YE2 | YE1 | YE0 | |

*NOTE: "-" Don't care*

**Description**

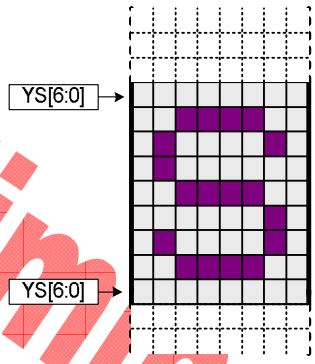
This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The value of YS [6:0] and YE [6:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.

(Example)






**Restriction**

YS [6:0] always must be equal to or less than YE [6:0]

When YS [6:0] or YE [6:0] is greater than 7Fh, data of out of range will be ignored.

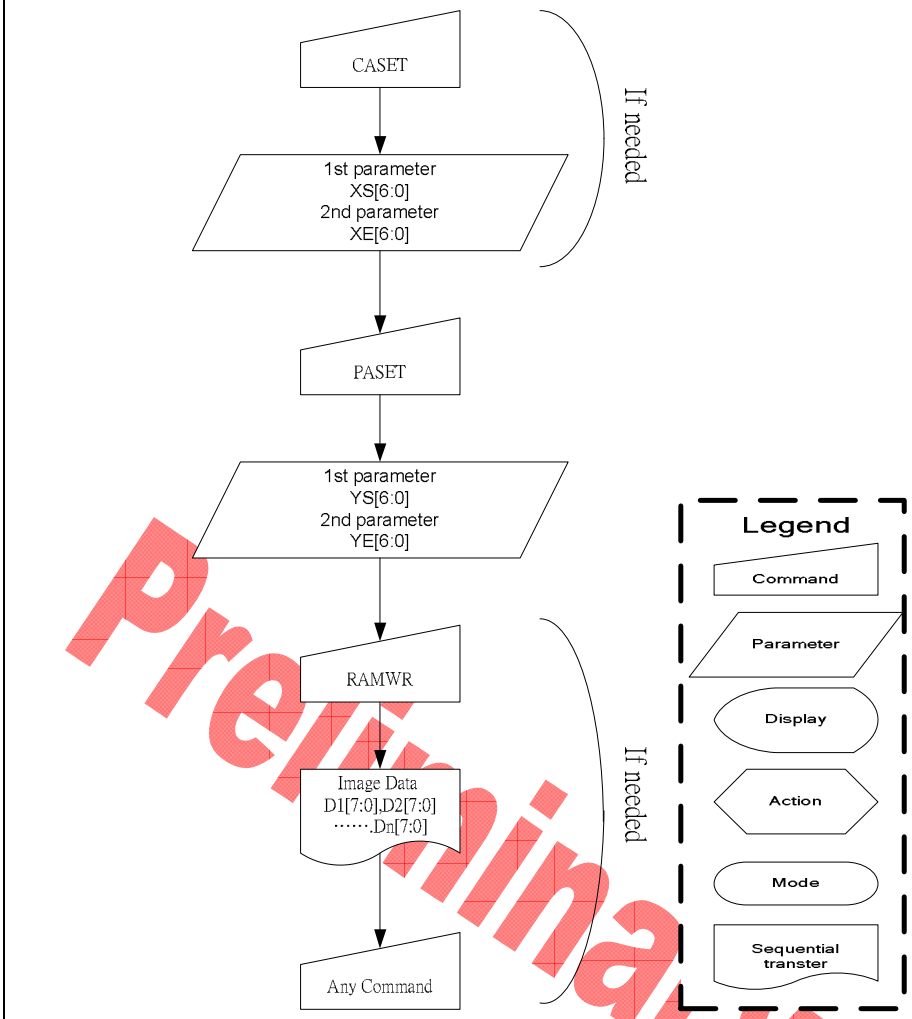
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | XS [6:0] | XE [6:0] |
| Power On Sequence | 00h | 7Fh |
| S/W Reset | 00h | 7Fh |
| H/W Reset | 00h | 7Fh |

Flow Chart



### 8.1.22. RAMWR: Memory Write (2Ch)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RAMWR | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **(2Ch)** |
| Write D1[7:0] | 1 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |
| : | 1 | 1 | 0 | : | : | : | : | : | : | : | : | - |
| Write Dn[7:0] | 1 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |

**Description**

This command is used to transfer data MCU to frame memory.

This command makes no change to the other driver status.

When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

The Start Column/Start Row positions are different in accordance with MADCTR setting. Then D [7:0] is stored in frame memory and the column register and the row register incremented.

Frame Write can be canceled by sending any other command.

**Restriction**

In all color modes, there is no restriction on length of parameters.

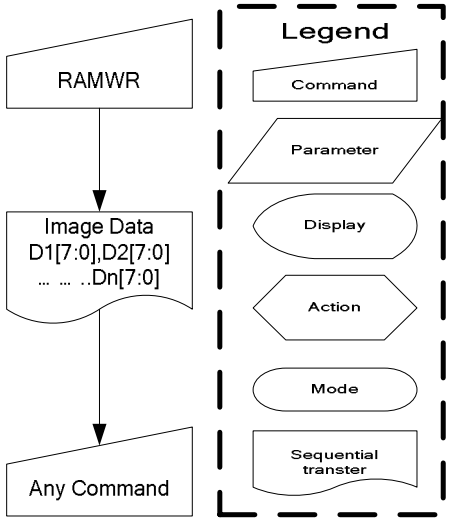
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is remained |
| H/W Reset | Contents of memory is remained |

**Flow Chart**



### 8.1.23. RAMRO : Memory Read (2EH)

| *Command* | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RAMRO | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **(2Eh)** |
| Dummy read | 1 | 0 | 1 | x | x | x | x | x | x | x | x | - |
| 2nd parameter | 1 | 0 | 1 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00H ~ FFH |
| … | 1 | 0 | 1 | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | 00H ~ FFH |
| (N+1)th parameter | 1 | 0 | 1 | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | 00H ~ FFH |

**Description**

This command is used to transfer data from frame memory to MCU. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTR setting. Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame Read can be stopped by sending any other command.

**Restriction**

In all color modes, the Frame Read is always 16bit so there is no restriction on length of parameters.

*Note: Memory Read is only possible via the Parallel Interface.*

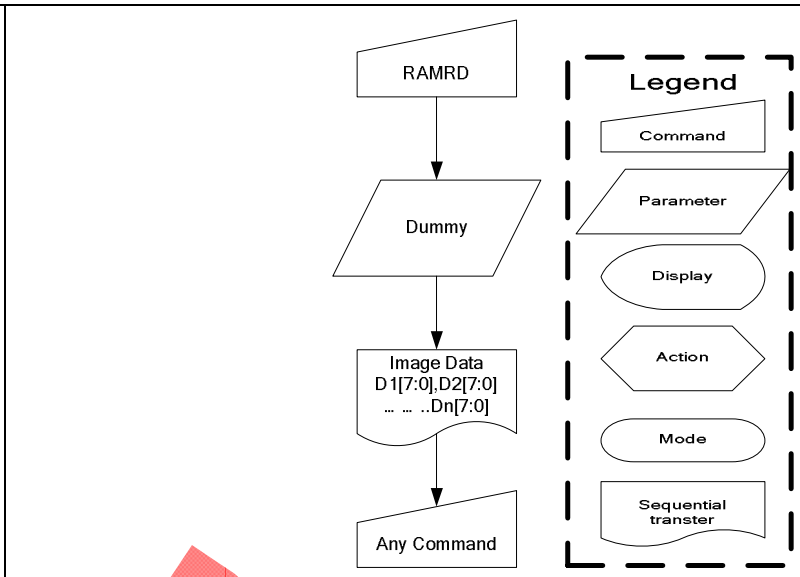
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |
| H/W Reset | Contents of memory is not cleared |

**Flow Chart**



### 8.1.24. PTLAR: Partial Area (30h)

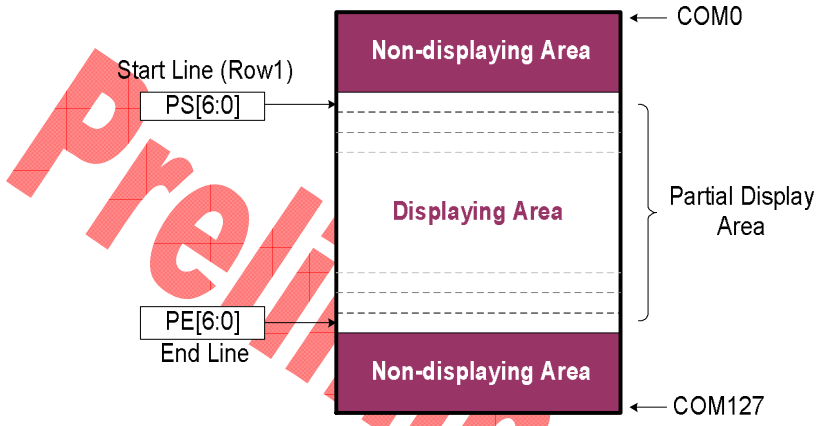
| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLAR | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | **(30h)** |
| 1st Parameter | 1 | 1 | 0 | 0 | PS6 | PS5 | PS4 | PS3 | PS2 | PS1 | PS0 | - |
| 2nd Parameter | 1 | 1 | 0 | 0 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | - |

*NOTE: "-" Don't care*

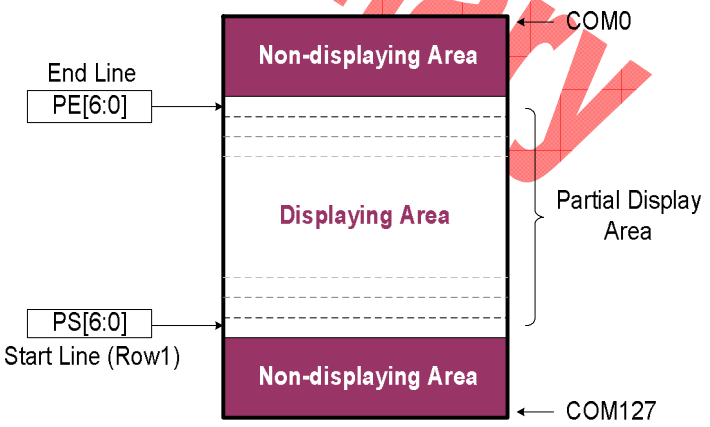
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Line (PS) and the second the End Line (PE), as illustrated in the figures below. PS and PE refer to the Frame Memory Line counter.

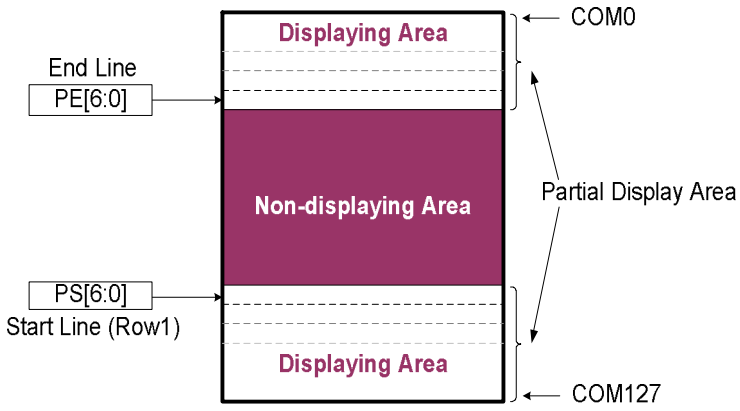
If End Line > Start Line when MADCTR ML=0:




If End Line > Start Line when MADCTR ML=1:




If End Line < Start Line when MADCTR ML=0:




* Row1: Frame memory row address 1.

If End Line = Start Line then the Partial Area will be one line deep.

Restriction

PS[6:0] and PE[6:0] are based on line unit.

PS[6:0]=00h, 01h, 02h, 03h, … , 7Fh

PE[6:0]= 00h, 01h, 02h, 03h, … , 7Fh

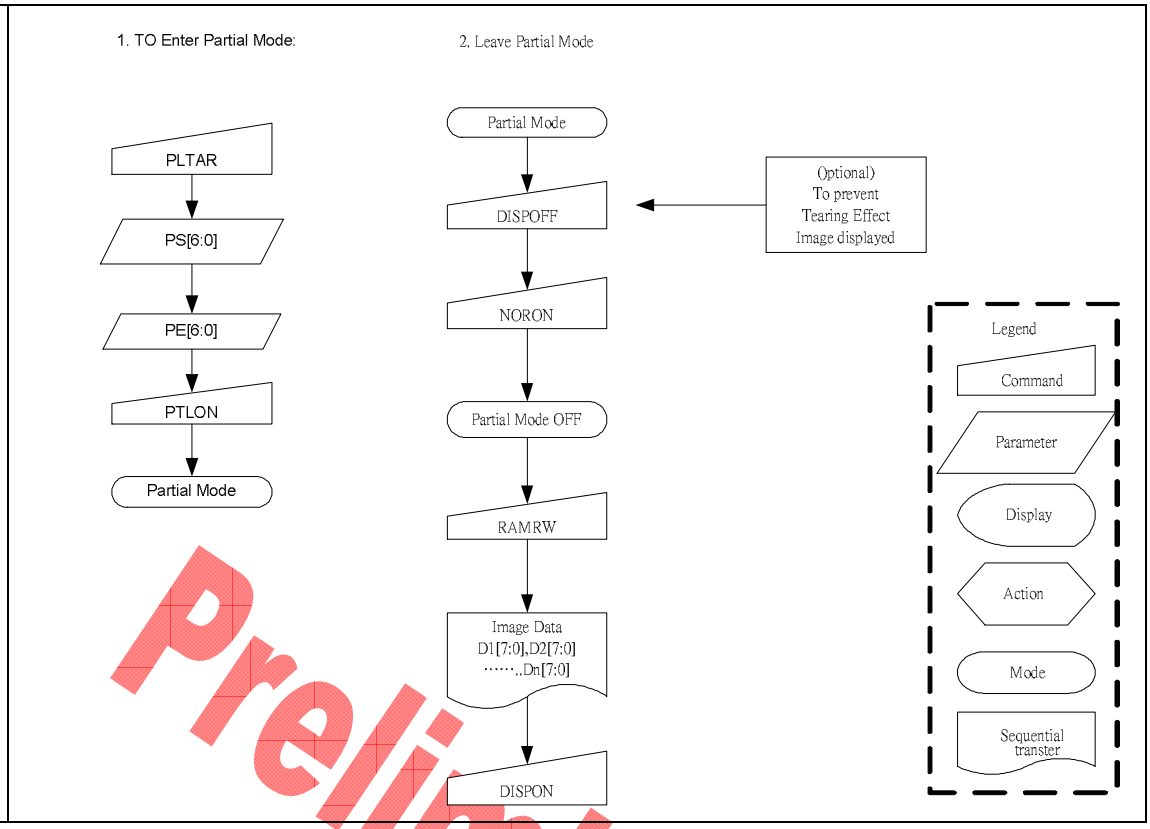
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | PS[6:0] | PE[6:0] |
| Power On Sequence | 00h | 7Fh |
| S/W Reset | 00h | 7Fh |
| H/W Reset | 00h | 7Fh |

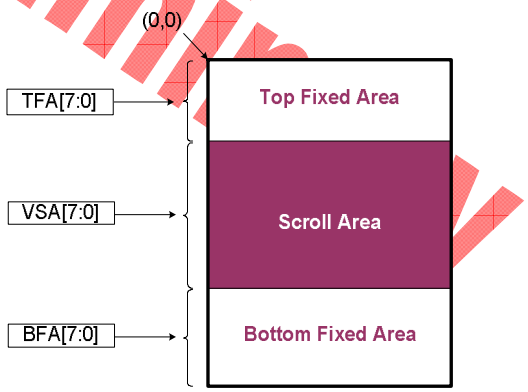
Flow Chart



### 8.1.25. SCRLAR: Scroll Area (33h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SCRLAR | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | **(33h)** |
| 1st parameter | 1 | 1 | 0 | TFA7 | TFA6 | TFA5 | TFA4 | TFA3 | TFA2 | TFA1 | TFA0 | - |
| 2nd parameter | 1 | 1 | 0 | VSA7 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 | - |
| 3rd parameter | 1 | 1 | 0 | BFA7 | BFA6 | BFA5 | BFA4 | BFA3 | BFA2 | BFA1 | BFA0 | - |

*NOTE: "-" Don't care*

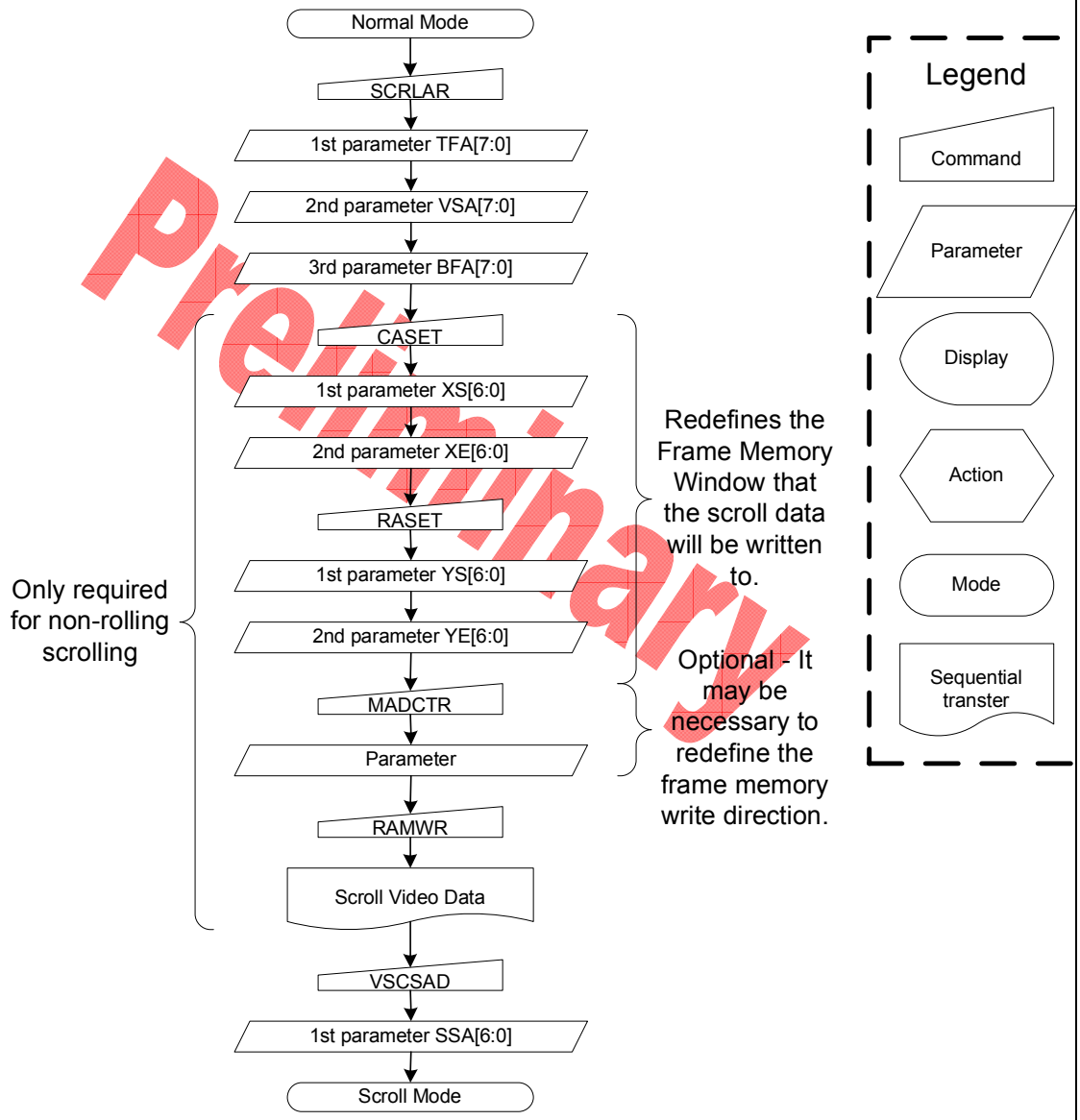
<table>
<tr><td>Description</td><td>This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll.<br>When MADCTR ML=0<br>The 1st parameter TFA [7:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).<br>The 2nd parameter VSA [7:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.<br>The 3rd parameter BFA [7:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).<br>TFA, VSA and BFA refer to the Frame Memory Line Pointer.<br> 
</td></tr>
<tr><td>Restriction</td><td>The condition is (TFA+VSA+BFA) = 128, otherwise Scrolling mode is undefined.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default

| Status | Default Value | | |
|---|---|---|---|
| | TFA [7:0] | VSA [7:0] | BFA [7:0] |
| Power On Sequence | 00h | 80h | 00h |
| S/W Reset | 00h | 80h | 00h |
| H/W Reset | 00h | 80h | 00h |

Flow Chart

1. TO Enter Vertical Scroll Mode:

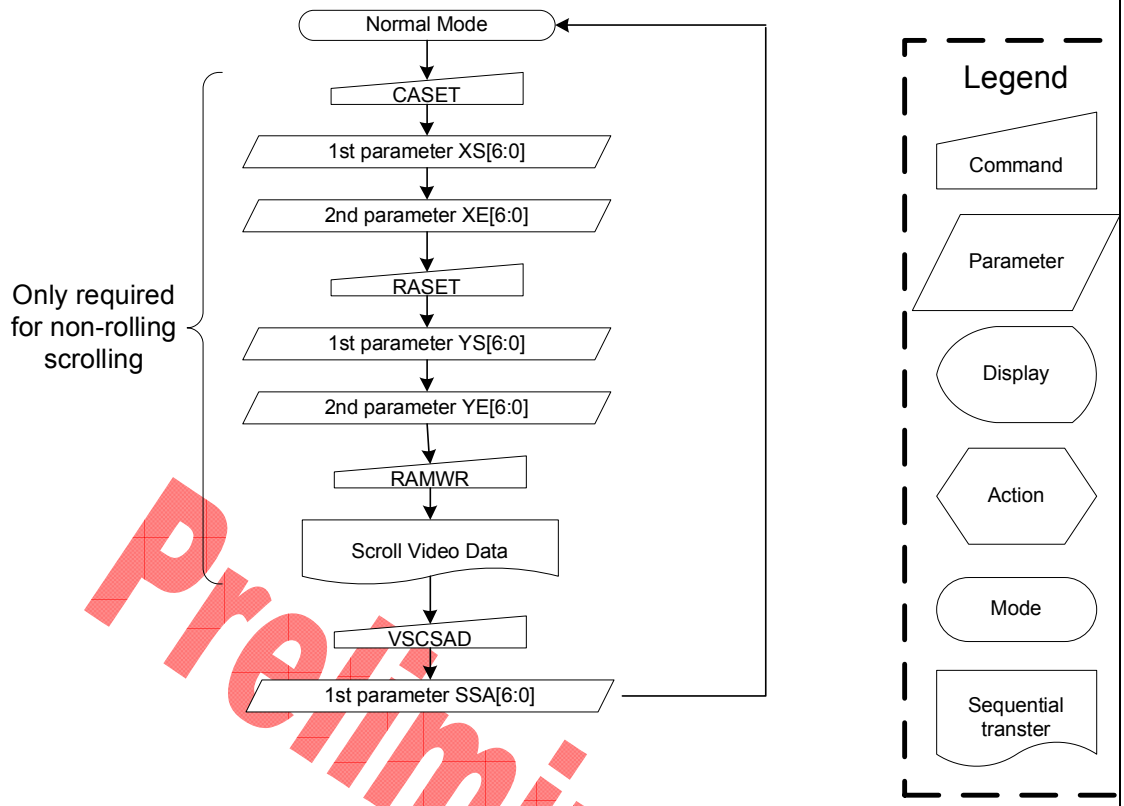





*NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.*

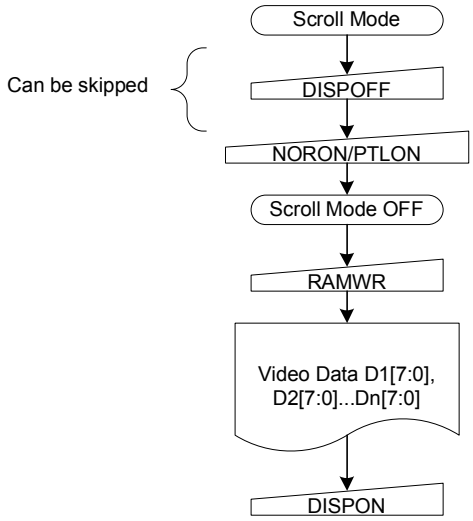
Flow Chart

2. Continuous Scroll:






3. To Exit Vertical Scroll Mode:




*NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.*

### 8.1.26. TEOFF: Tearing Effect Line OFF (34h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEOFF | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | **(34h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. |
| Restriction | This command has no effect when Tearing Effect output is already OFF. |

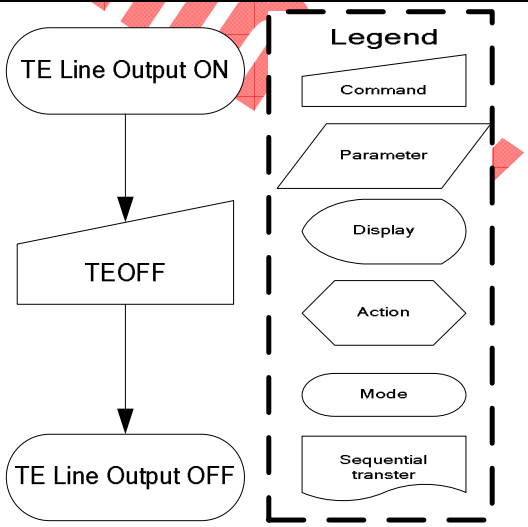
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Tearing effect off |
| S/W Reset | Tearing effect off |
| H/W Reset | Tearing effect off |

Flow Chart



### 8.1.27. TEON: Tearing Effect Line ON (35h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEON | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | **(35h)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | - | - | M | |

*NOTE: "-" Don't care*

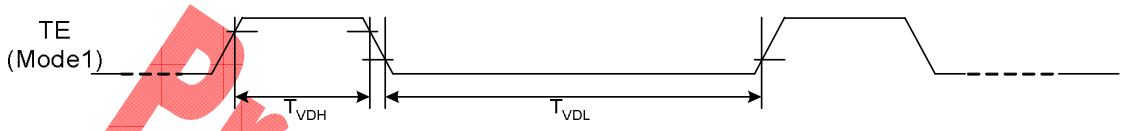
**Description**

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTR bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

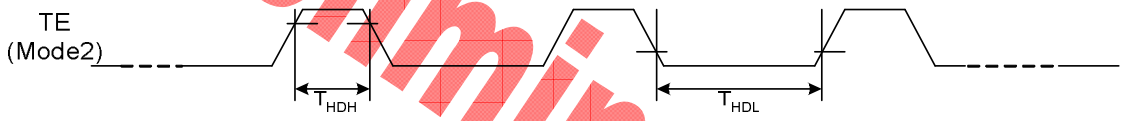
When M=0:

The Tearing Effect Output Line consists of V-Blanking information only:




When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:




See section 7.4.8 for more information.

*Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*

**Restriction**

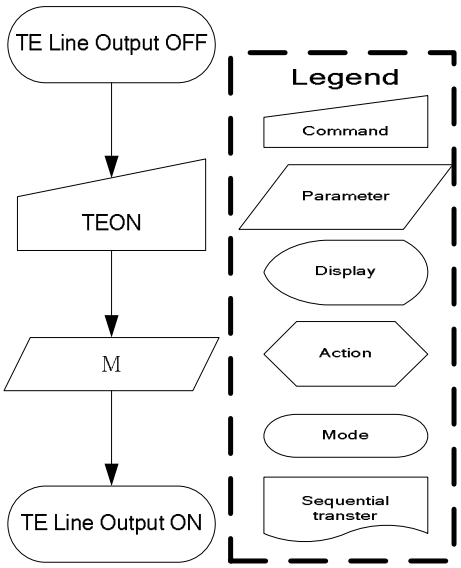
This command has no effect when Tearing Effect output is already OFF.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Tearing effect off & M=0 |
| S/W Reset | Tearing effect off & M=0 |
| H/W Reset | Tearing effect off & M=0 |

| Flow Chart |  |
|---|---|

### 8.1.28. MADCTR: Memory Data Access Control (36h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MADCTR | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | **(36h)** |
| Parameter | 1 | 1 | 0 | MY | MX | MV | ML | RGB | - | - | - | - |

*NOTE: "-" Don't care*

**Description**

This command defines read/write scanning direction of frame memory.

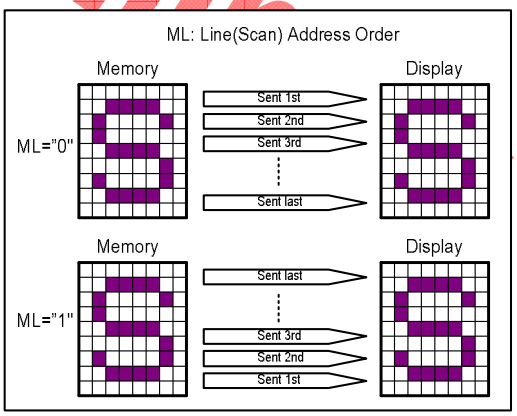
This command makes no change on the other driver status.

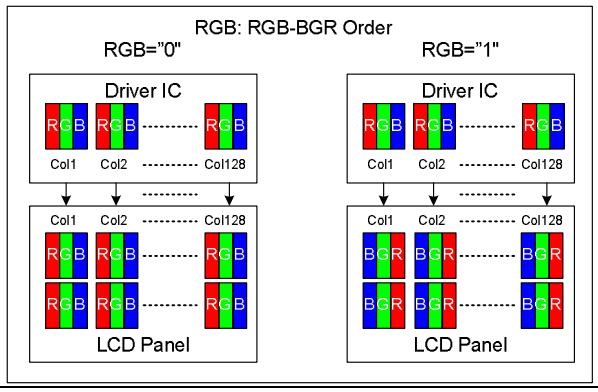
Note: ML affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands

Bit Assignment

| Bit | NAME | DESCRIPTION |
|---|---|---|
| MY | ROW ADDRESS ORDER | These 3bits controls MCU to memory write/read direction. |
| MX | COLUMN ADDRESS ORDER | |
| MV | ROW/COLUMN ORDER | |
| ML | LINE ADDRESS ORDER | LCD refresh direction control |
| RGB | RGB-BGR ORDER | Color selector switch control<br>0=RGB color filter panel, 1=BGR color filter panel)<br>The contents of the frame memory are not changed. |






**Restriction**

D2, D1 and D0 of the 1st parameter are set to '000'internally.

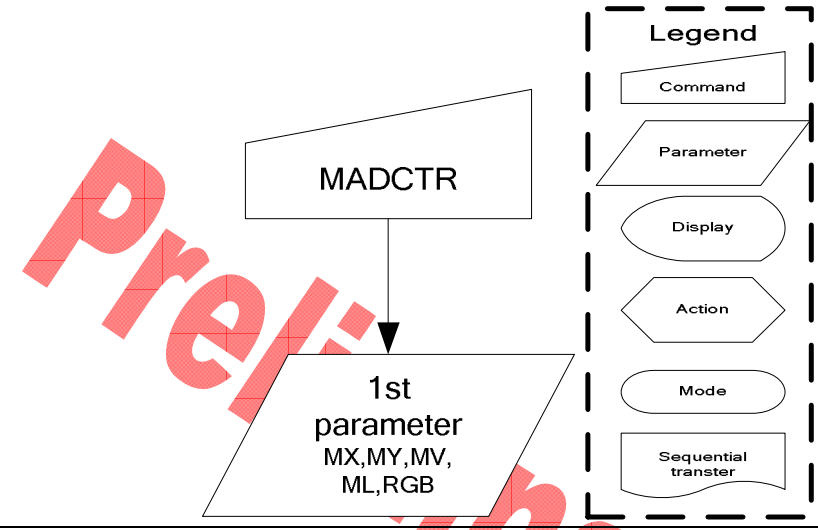
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |

| | | |
|---|---|---|
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In | Yes |

| | | |
|---|---|---|
| Default | Status | Default Value |
| | Power On Sequence | MY=0,MX=0,MV=0,ML=0,RGB=0 |
| | S/W Reset | Not changed |
| | H/W Reset | MY=0,MX=0,MV=0,ML=0,RGB=0 |

Flow Chart



### 8.1.29. VSCSAD: Vertical Scroll Start Address of RAM (37h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSCSAD | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | **(37h)** |
| Parameter | 1 | 1 | 0 | 0 | SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSA0 | |

**Description**

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

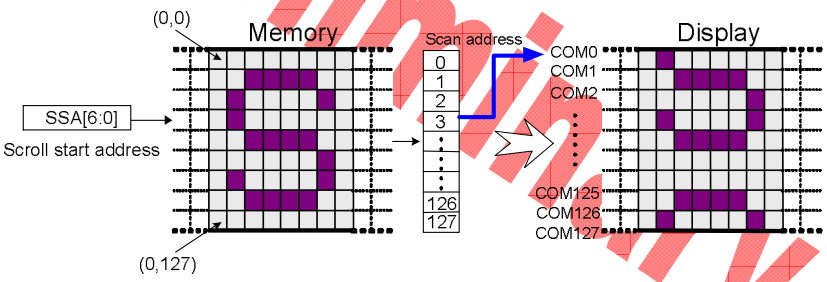
This command Start the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

**When MADCTR ML=0**

Example:

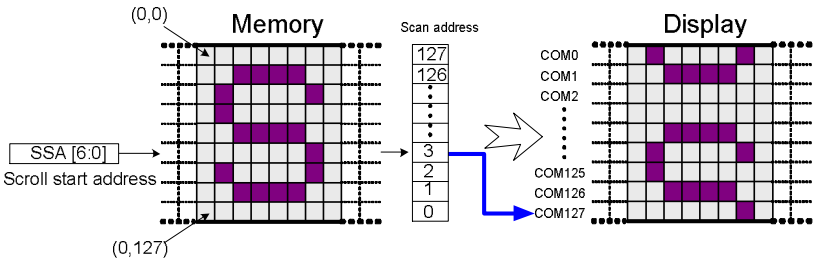
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=128 and Vertical Scrolling Pointer SSA='3'.




**When MADCTR ML=1**

Example:

When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=128 and Vertical Scrolling Pointer SSA='3'.



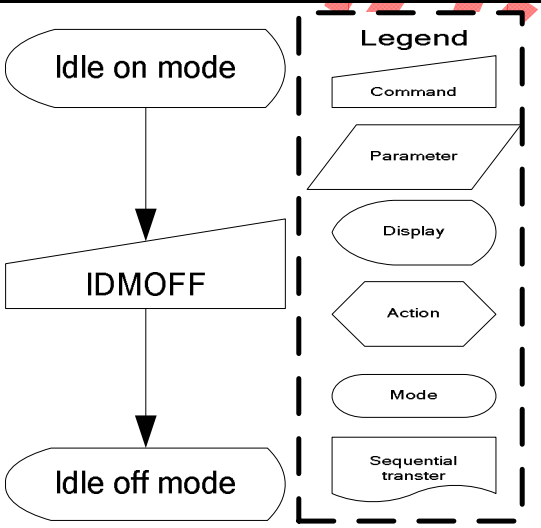

*NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.*

*SSA refers to the Frame Memory line Pointer.*

<table>
<tr><td>Restriction</td><td>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.<br>SSA [6:0] is based on line unit.<br>SSA [6:0] = 00h, 01h, 02h, 03h, … , 7Fh</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><td>Status</td><td>Default Value (SSA[6:0])</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

### 8.1.30. IDMOFF: Idle Mode Off (38h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IDMOFF | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | **(38h)** |
| Parameter | No Parameter | | | | | | | | | | | |

| | |
|---|---|
| Description | This command is used to recover from Idle mode on.<br>There will be no abnormal visible effect on the display mode change transition.<br>In the idle off mode,<br>1. LCD can display maximum 262,144 colors.<br>2. Normal frame frequency is applied. |
| Restriction | This command has no effect when module is already in idle off mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / Idle mode off<br>S/W Reset / Idle mode off<br>H/W Reset / Idle mode off |
| Flow Chart |  |

### 8.1.31. IDMON: Idle Mode On (39h)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IDMON | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | **(39h)** |
| Parameter | No Parameter | | | | | | | | | | | |

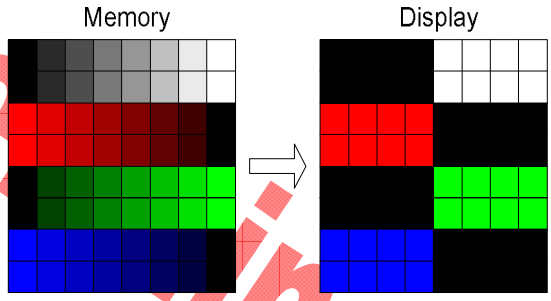
**Description**

This command is used to enter into Idle mode on.

There will be no abnormal visible effect on the display mode change transition. In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)




"X": don't care

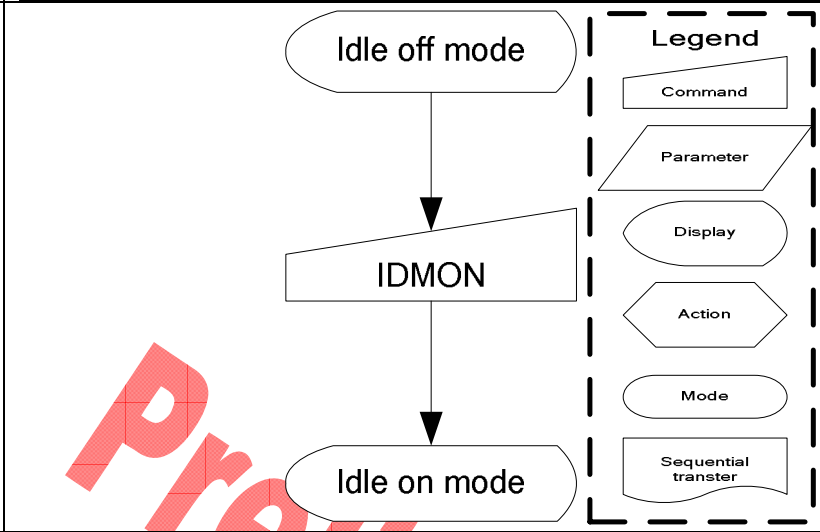
| Color | $R_5$ $R_4$ $R_3$ $R_2$ $R_1$ $R_0$ | $G_5$ $G_4$ $G_3$ $G_2$ $G_1$ $G_0$ | $B_5$ $B_4$ $B_3$ $B_2$ $B_1$ $B_0$ |
|---|---|---|---|
| Black | 0XXXXX | 0XXXXX | 0XXXXX |
| Blue | 0XXXXX | 0XXXXX | 1XXXXX |
| Red | 1XXXXX | 0XXXXX | 0XXXXX |
| Magenta | 1XXXXX | 0XXXXX | 1XXXXX |
| Green | 0XXXXX | 1XXXXX | 0XXXXX |
| Cyan | 0XXXXX | 1XXXXX | 1XXXXX |
| Yellow | 1XXXXX | 1XXXXX | 0XXXXX |
| White | 1XXXXX | 1XXXXX | 1XXXXX |

**Restriction**

This command has no effect when module is already in idle on mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

| | | |
|---|---|---|
| Default | Status | Default Value |
| | Power On Sequence | Idle mode off |
| | S/W Reset | Idle mode off |
| | H/W Reset | Idle mode off |
| Flow Chart |  | |

### 8.1.32. COLMOD: Interface Pixel Format (3Ah)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COLMOD | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | **(3Ah)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | P2 | P1 | P0 | - |

**Description**

This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:

| Interface Format | P2 | P1 | P0 |
|---|---|---|---|
| Not Defined | 0 | 0 | 0 |
| Not Defined | 0 | 0 | 1 |
| Not Defined | 0 | 1 | 0 |
| 12Bit/Pixel (Type A) | 0 | 1 | 1 |
| 12Bit/Pixel (Type B) | 1 | 0 | 0 |
| 16Bit/Pixel | 1 | 0 | 1 |
| Not Defined | 1 | 1 | 0 |
| Not Defined | 1 | 1 | 1 |

**Restriction**

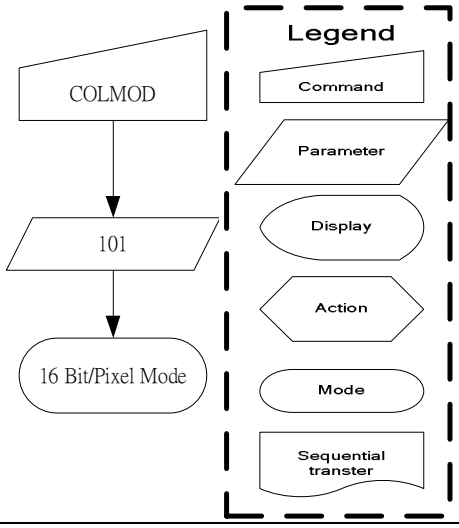
There is no visible effect until the Frame Memory is written to.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 05h (16Bit/Pixel) |
| S/W Reset | No Change |
| H/W Reset | 05h (16Bit/Pixel) |

| | |
|---|---|
| Flow Chart | Example:  |

### 8.1.33. RDID: Read ID Value (DAh)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDID1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | **(DAh)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ID1 | ID0 | - |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | This read byte returns 8-bit LCD module's manufacturer ID<br>D1-D0 (ID1 to ID0): LCD module's manufacturer ID. |
| Restriction | |

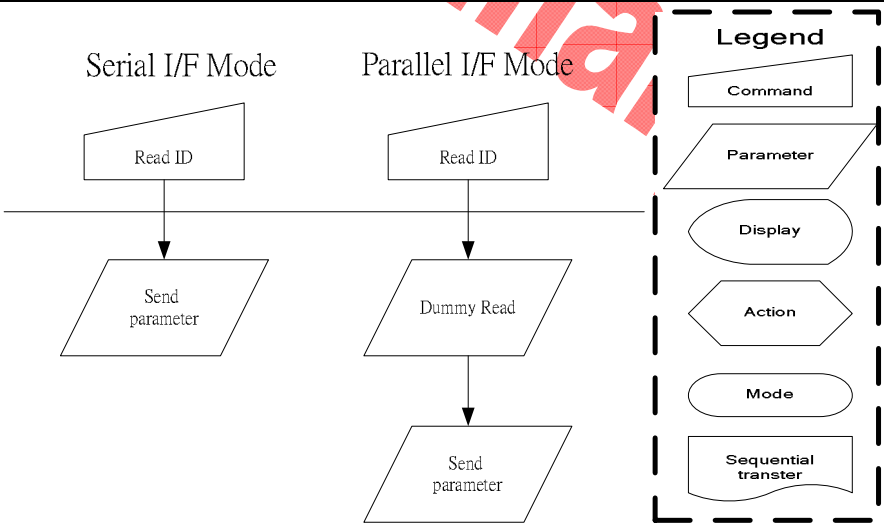
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart



### 8.1.34. DutySet: Display Duty setting (B0H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DutySet | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | **(B0h)** |
| Parameter | 1 | 1 | 0 | Du7 | Du6 | Du5 | Du4 | Du3 | Du2 | Du1 | Du0 | - |

*NOTE: "-" Don't care*

**Description**

This command is used to set display duty. Command set = display duty numbers - 1.

**Example:**

| Duty | Du7 | Du6 | Du5 | Du4 | Du3 | Du2 | Du1 | Du0 | Command set= Display duty numbers-1 |
|---|---|---|---|---|---|---|---|---|---|
| Example: 1/128 duty | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128-1=127 |

**Restriction**

Display duty must > 4 (1/4 duty)

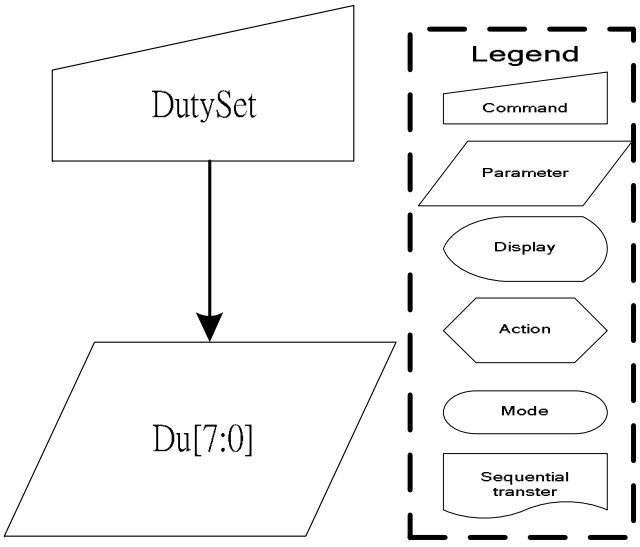
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (Du[6:0]) |
|---|---|
| Power On Sequence | 0111111b (7Fh) |
| S/W Reset | 0111111b (7Fh) |
| H/W Reset | 0111111b (7Fh) |

**Flow Chart**



### 8.1.35. FirstCom: First Com. Page address (B1H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FirstCom | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | **(B1h)** |
| Parameter | 1 | 1 | 0 | 0 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | - |

*NOTE: "-" Don't care*

**Description**

This command defines the first output COM number that mapping to the RAM page address 0. For detail setting value, please see the table as below.

| F6 | F5 | F4 | F3 | F2 | F1 | F0 | Line address |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | | 0 | 0 |
| 0 | 0 | 0 | 0 | | | 1 | 1 |
| 0 | 0 | 0 | 1 | | | 0 | 2 |
| 0 | 0 | 0 | 1 | | | 1 | 3 |
| : | : | : | : | | | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

Example:

If FirstCom=8, common 8 would output the data of RAM page address 0.

**Restriction**

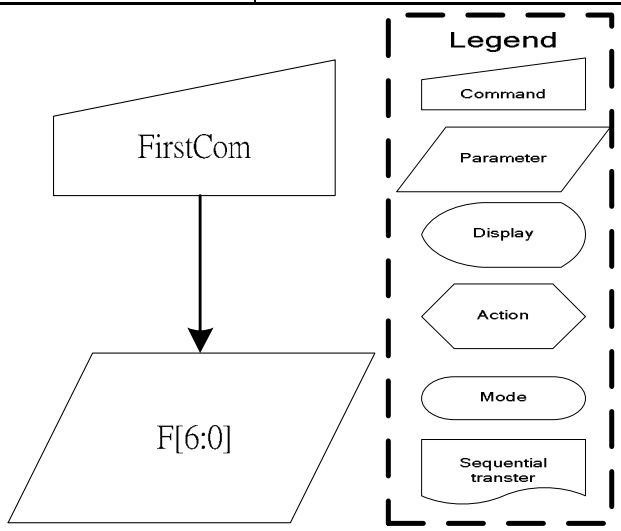
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (F[6:0]) |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**



### 8.1.36. OscDiv: FOSC Divider (B3H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OscDiv | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | **(B3h)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | - | CLD1 | CLD0 | - |

*NOTE: "-" Don't care*

**Description**

This command is used to specify the Fosc dividing ratio.

CLD1, CLD0: CL dividing ratio. They are used to change number of dividing stages of internal clock.

| CLD1 | CLD0 | Fosc dividing ratio |
|---|---|---|
| 0 | 0 | Not divide |
| 0 | 1 | 2 divisions |
| 1 | 0 | 4 divisions |
| 1 | 1 | 8 divisions |

**Restriction**

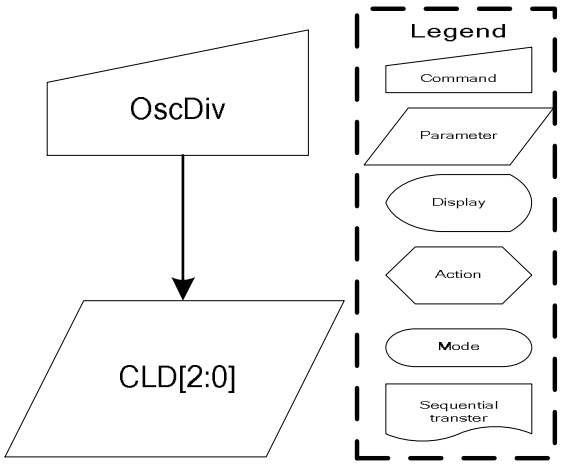
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (CLD[0:1]) |
|---|---|
| Power On Sequence | 00b |
| S/W Reset | 00b |
| H/W Reset | 00b |

**Flow Chart**



### 8.1.37. NLInvSet: N-Line control (B5H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NLInvSet | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | **(B5h)** |
| Parameter | 1 | 1 | 0 | M | 0 | 0 | N4 | N3 | N2 | N1 | N0 | - |

*NOTE: "-" Don't care*

**Description**

This command is used to set the inverted line number with range of 2 to (duty-1) to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frames. If N[6:0]=0, N-line inversion function is disable.

Line inversion numbers=N[6:0] +1.

Example:

If N[6:0]=7, inversion occurs per 8 line.

**Restriction**

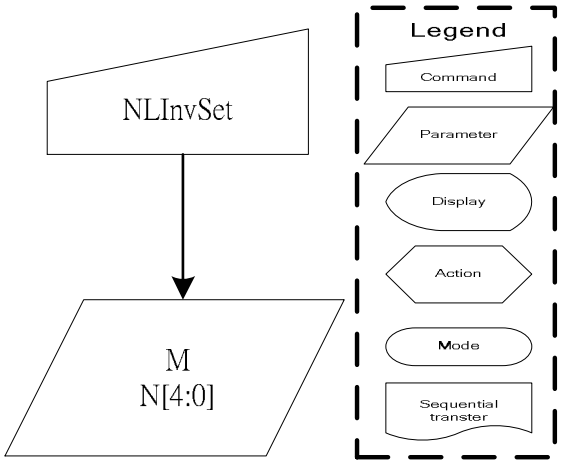
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | M | N[4:0] |
| Power On Sequence | 0b | 00000b |
| S/W Reset | 0b | 00000b |
| H/W Reset | 0b | 00000b |

**Flow Chart**



### 8.1.38. ComScanDir: Com/Seg Scan Direction for glass layout (B7H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ComScanDir | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | **(B7h)** |
| Parameter | 1 | 1 | 0 | 0 | SMX | 0 | 0 | SBGR | 0 | 0 | 0 | - |

*NOTE: "-" Don't care*

**Description**

| | Function | 0 | 1 |
|---|---|---|---|
| SMX | Inverse the MX setting | Keep MX | Inverse MX |
| SBGR | Inverse the BGR setting | Keep BGR | Inverse BGR |

**Restriction**

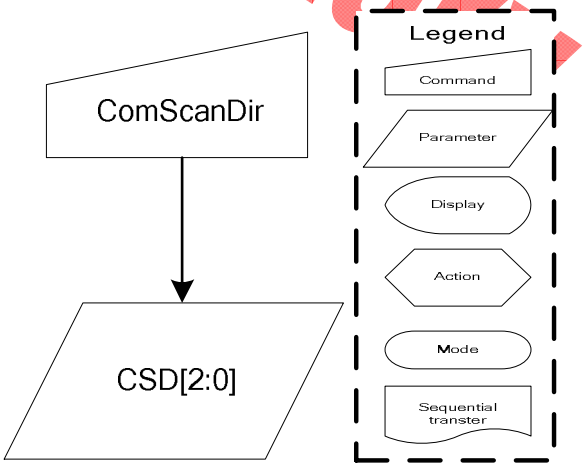
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 40h |
| S/W Reset | 40h |
| H/W Reset | 40h |

**Flow Chart**



### 8.1.39. RMWIN: Read Modify Write control in (B8H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RMWIN | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | **(B8h)** |
| Parameter | No Parameter | | | | | | | | | | | |

*NOTE: "-" Don't care*

| | | |
|---|---|---|
| Description | Read modify write control IN | |
| Restriction | | |
| Register Availability | Status | Availability |
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In | Yes |
| Default | Status | Default Value |
| | Power On Sequence | -- |
| | S/W Reset | -- |
| | H/W Reset | -- |

### 8.1.40. RMWOUT: Read Modify Write control out (B9H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RMWOUT | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | **(B9h)** |
| Parameter | No Parameter | | | | | | | | | | | |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | Read modify write control out |
| Restriction | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / --<br>S/W Reset / --<br>H/W Reset / -- |

### 8.1.41. DispCompStep: Display Compensation Step (BDH)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RMWOUT | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | **(BDh)** |
| Parameter | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Step2 | Step1 | Step0 | - |

*NOTE: "-" Don't care*

**Description**

The command is used to program the optimum LCD display quality.

**Restriction**

| Step2 | Step1 | Step0 | STEP |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 04h |
| S/W Reset | 04h |
| H/W Reset | 04h |

### 8.1.42. VopSet: Vop set (C0H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VopSet | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **(C0h)** |
| 1st parameter | 1 | 1 | 0 | Vop7 | Vop6 | Vop5 | Vop4 | Vop3 | Vop2 | Vop1 | Vop0 | - |
| 2nd parameter | 1 | 1 | 0 | - | - | - | - | - | - | - | Vop8 | |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | The command is used to program the optimum LCD supply voltage V0. Please see Section 7.9 for reference. |
| Restriction | |

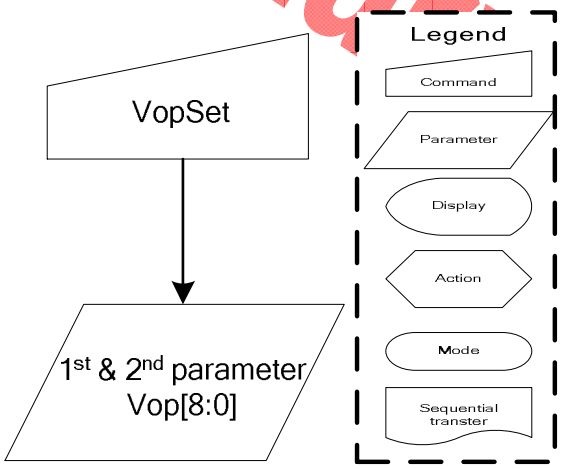
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value (Vop=12V) | |
|---|---|---|
| | Vop8 | Vop[7:0] |
| Power On Sequence | 0 | 11010010b (D2h) |
| S/W Reset | 0 | 11010010b (D2h) |
| H/W Reset | 0 | 11010010b (D2h) |

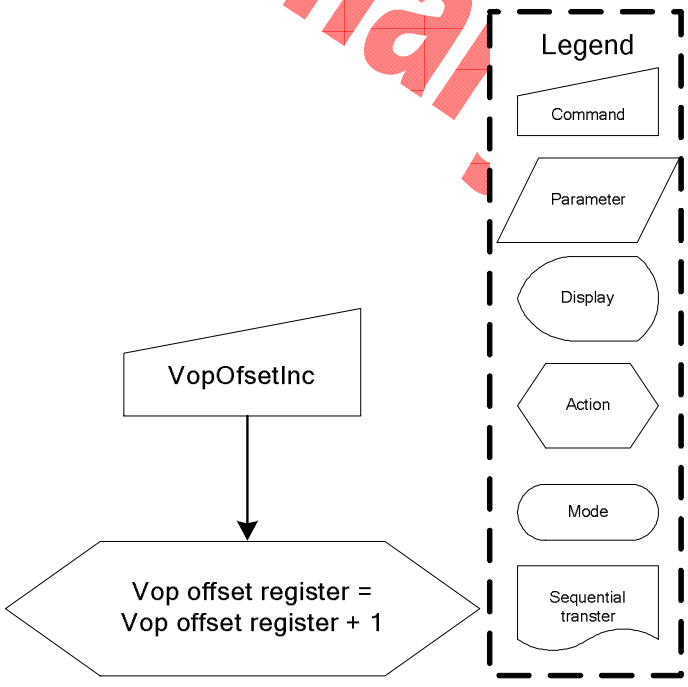
Flow Chart



### 8.1.43. VopOfsetInc: Vop Increase 1 (C1H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VopOfsetInc | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | **(C1h)** |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | With the VopOfsetInc and VopOfsetDec command the $V_{LCD}$ voltage and therewith the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1.<br>If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed. |
| Restriction | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status / Default Value<br>Power On Sequence: --<br>S/W Reset: --<br>H/W Reset: -- |
| Flow Chart |  |

### 8.1.44. VopOfsetDec: Vop Decrease 1 (C2H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VopOfsetDec | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | **(C2h)** |

*NOTE: "-" Don't care*

**Description**

With the VopOfsetInc and VopOfsetDec command the $V_{LCD}$ voltage and therewith the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1.

If you set the electronic control value to 00000, the control value is set to 11111 after this command has been executed.

| Electronic Control Value | Decimal Equivalent | V0 Offset |
|---|---|---|
| 11111 | 15 | +600 mV |
| 11110 | 14 | +560 mV |
| 11101 | 13 | +520 mV |
| … | … | … |
| 00010 | 2 | +80 mV |
| 00001 | 1 | +40 mV |
| 00000 | 0 | 0 mV |
| 11111 | -1 | -40 mV |
| 11110 | -2 | -80 mV |
| … | … | … |
| 00010 | -13 | -520 mV |
| 00001 | -14 | -560 mV |
| 00000 | -15 | -600 mV |

**Table 8.1-1 Possible Vop[4:0] values**



**Restriction**

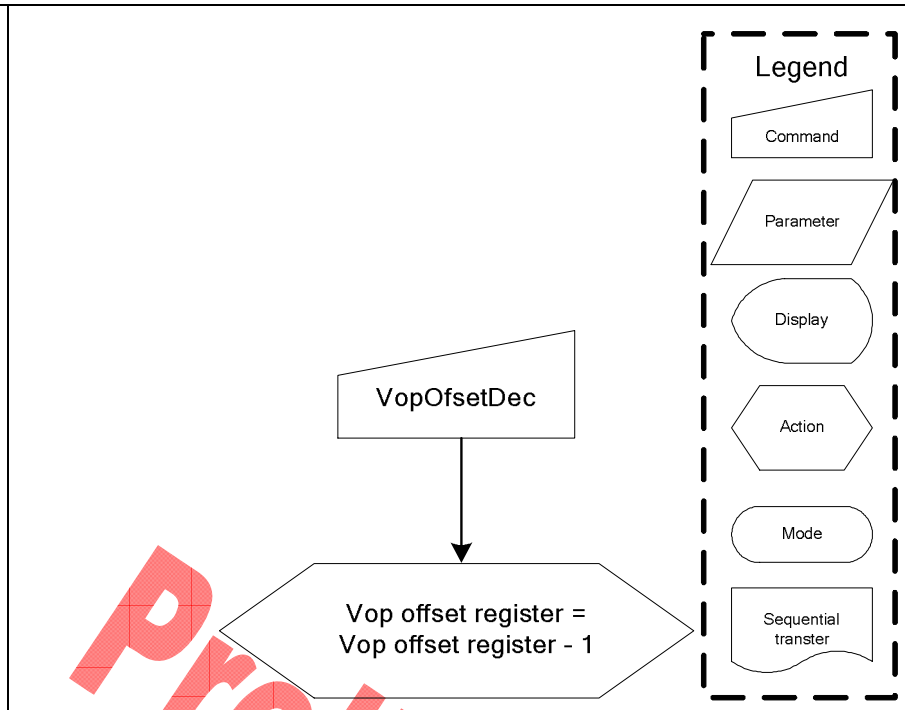
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | -- |
| S/W Reset | -- |
| H/W Reset | -- |

| Flow Chart | |
|---|---|



### 8.1.45. BiasSel: Bias Selection (C3H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BiasSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | **(C3h)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | Bias2 | Bias1 | Bias0 | - |

*NOTE: "-" Don't care*

**Description**

Select LCD bias ratio of the voltage required for driving the LCD.

| Bais2 | Bais1 | Bais0 | LCD bias |
|---|---|---|---|
| 0 | 0 | 0 | 1/12 |
| 0 | 0 | 1 | 1/11 |
| 0 | 1 | 0 | 1/10 |
| 0 | 1 | 1 | 1/9 |
| 1 | 0 | 0 | 1/8 |
| 1 | 0 | 1 | 1/7 |
| 1 | 1 | 0 | 1/6 |
| 1 | 1 | 1 | Reserved |

**Restriction**

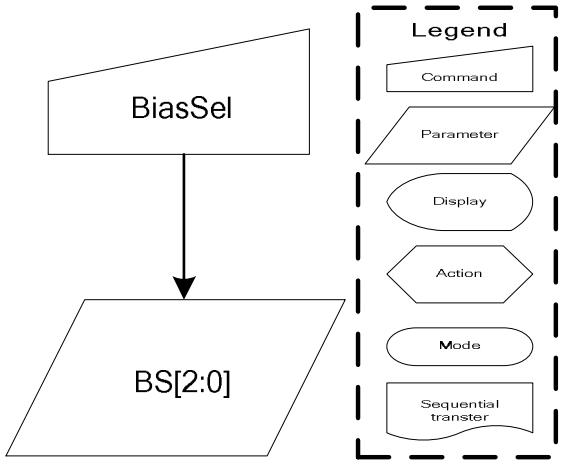
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (Bias[2:0]) |
|---|---|
| Power On Sequence | 011b |
| S/W Reset | 011b |
| H/W Reset | 011b |

**Flow Chart**



### 8.1.46. BstPmpXSel: Booster Setting (C4H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BstPmpXSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | **(C4h)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | BST2 | BST 1 | BST0 | - |

*NOTE: "-" Don't care*

**Description**

Booster setting

| BST2 | BST1 | BST0 | |
|---|---|---|---|
| 0 | 0 | 0 | x1 boosting circuit (Booster off) |
| 0 | 0 | 1 | x2 boosting circuit |
| 0 | 1 | 0 | x3 boosting circuit |
| 0 | 1 | 1 | x4 boosting circuit |
| 1 | 0 | 0 | x5 boosting circuit |
| 1 | 0 | 1 | x6 boosting circuit |
| 1 | 1 | 0 | x7 boosting circuit |
| 1 | 1 | 1 | x8 boosting circuit |

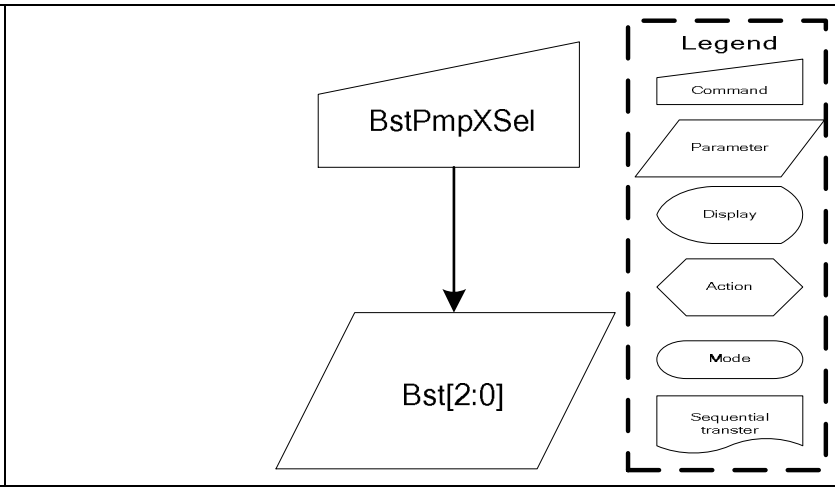
**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (BST[2:0]) |
|---|---|
| Power On Sequence | 111b |
| S/W Reset | 111b |
| H/W Reset | 111b |

| | |
|---|---|
| Flow Chart |  |

### 8.1.47. BstEffSel: Booster Efficiency selection (C5H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BstEffSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | **(C5h)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | - | BTF1 | BTF0 | - |

*NOTE: "-" Don't care*

**Description**

Booster Efficiency set

| BTF1 | BTF0 | Frequency ( Hz ) |
|---|---|---|
| 0 | 0 | Level 1 |
| 0 | 1 | Level 2 (default) |
| 1 | 0 | Level 3 |

By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~3) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level3 is higher than level1). The Boost Efficiency is better than lower level, and it just need few more power consumption current.

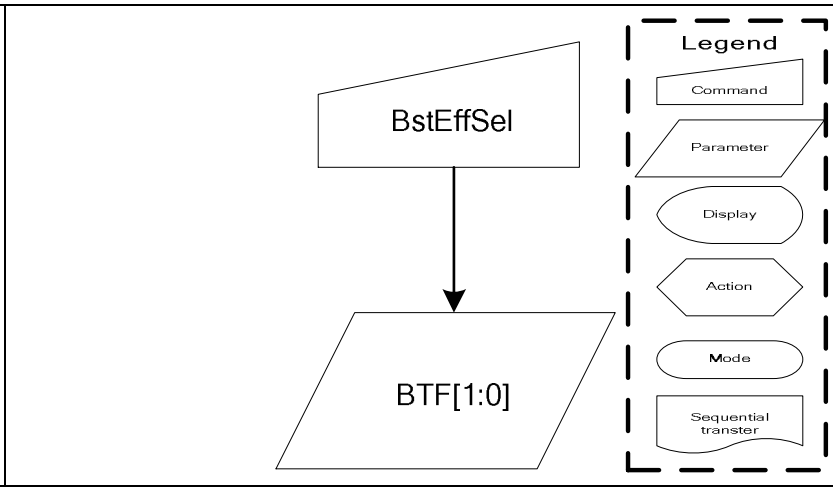
**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (BTF[1:0]) |
|---|---|
| Power On Sequence | 01b |
| S/W Reset | 01b |
| H/W Reset | 01b |

| | |
|---|---|
| Flow Chart |  |

### 8.1.48. VgSorcSel: Vg source control (CBH)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V3SorcSel | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | **(CBh)** |
| Parameter | 1 | 1 | 0 | - | - | - | - | - | - | - | 2BT0 | - |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | 2BT0=0: Vg source comes from VDD2 ;<br>2BT0=1: Vg source comes from 2-times charge pump. |
| Restriction | |

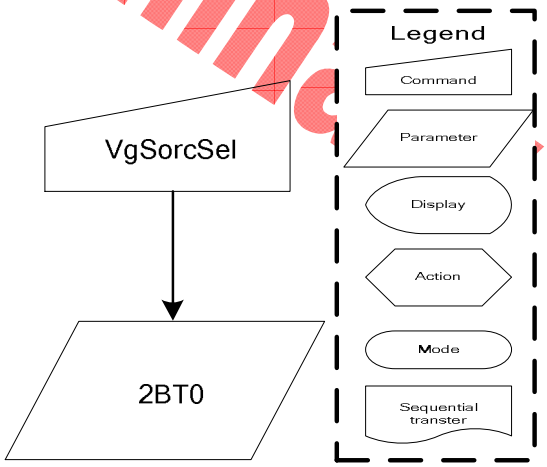
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value (2BT0) |
|---|---|
| Power On Sequence | 1 |
| S/W Reset | 1 |
| H/W Reset | 1 |

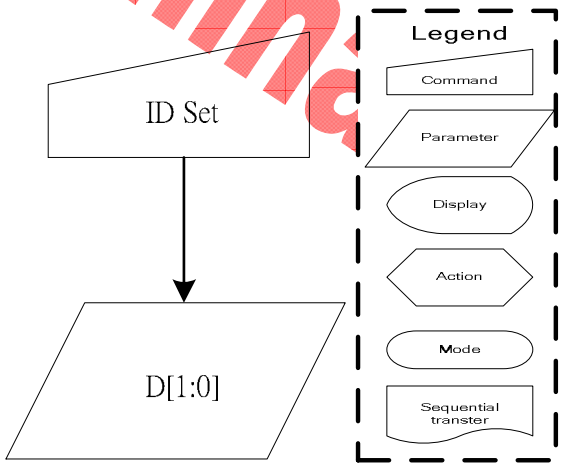
Flow Chart



### 8.1.49. IDSet : ID setting (CCH)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID1Set | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | **(CCh)** |
| Parameter | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ID1 | ID0 | - |

*NOTE: "-" Don't care*

<table>
<tr><td>Description</td><td>ID setting for request by customer</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

### 8.1.50. NASET: Analog circuit setting (D0H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AutoLoadSet | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | **(D0h)** |
| Parameter | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | **(1Dh)** |

*NOTE: "-" Don't care*

**Description**

Analog circuit setting. Such as follower selection, level shifter power mode selection.

**Restriction**

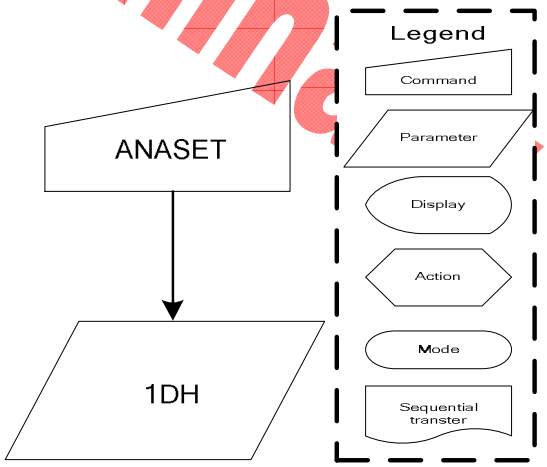
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value D[7:0] |
|---|---|
| Power On Sequence | 19h |
| S/W Reset | 19h |
| H/W Reset | 19h |

**Flow Chart**



### 8.1.51. AutoLoadSet: EEPROM data auto re-load control (D7H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AutoLoadSet | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | **(D7h)** |
| Parameter | 1 | 1 | 0 | 1 | 0 | 0 | ARD | 1 | 1 | 1 | 1 | - |

*NOTE: "-" Don't care*

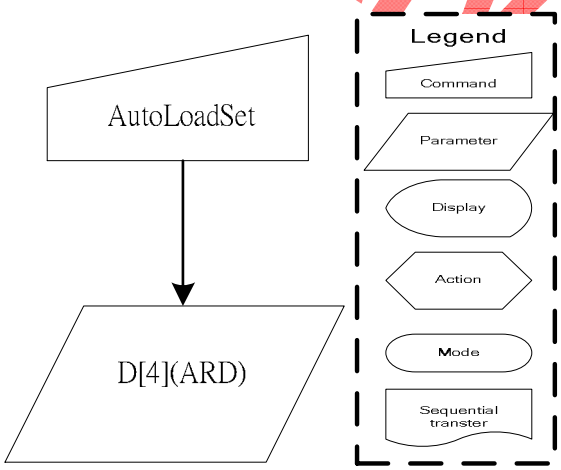
| | |
|---|---|
| Description | ARD : EEPROM auto read enable control, 1: Disable EEPROM auto read,<br>0: Enable EEPROM auto read |
| Restriction | |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default ValueD[7:0] |
|---|---|
| Power On Sequence | 1Fh |
| S/W Reset | 1Fh |
| H/W Reset | 1Fh |

Flow Chart



### 8.1.52. RDTstStatus: Read IC status (DEH)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDTstStatus | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | **(DEh)** |
| Dummy Read | 1 | 0 | 1 | - | - | - | - | - | - | - | - | |
| Parameter | 1 | 0 | 1 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | - |

*NOTE: "-" Don't care*

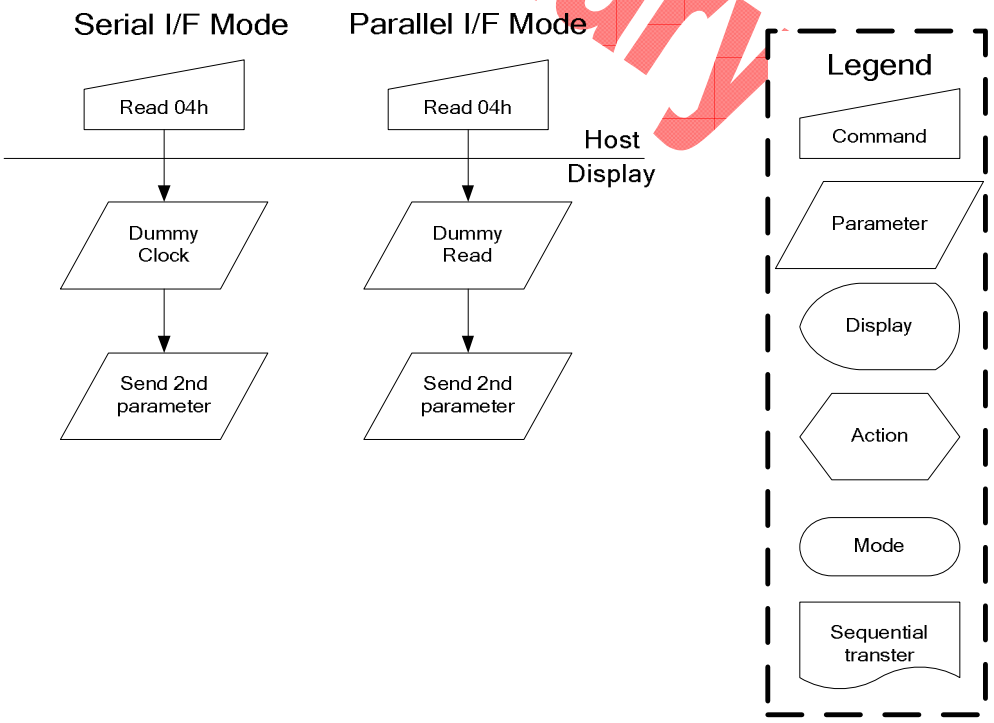
| | |
|---|---|
| Description | Read IC status.<br>Contect of EEPROM / RDA / PWR_VOP read control<br>(selection Byte by StusOutByteSel[3:0] control) |
| Restriction | |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | - |
| S/W Reset | - |
| H/W Reset | - |

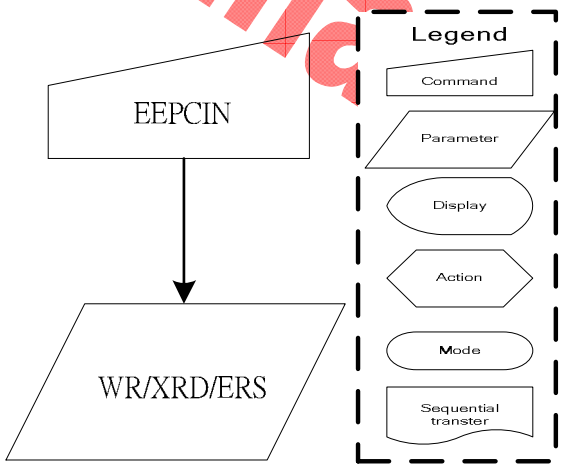
Flow Chart



### 8.1.53. EEPCIN: control EEPROM WR/ERS/RD (E0H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EEPCIN | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **(E0h)** |
| Parameter | 1 | 1 | 0 | 0 | 0 | WR/ERS/RD | 0 | 0 | 0 | 0 | 0 | - |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | WR/ERS/RD: when setting "1", the Write/Erase enable of EEPROM will be opened.<br>WR/ERS/RD: when setting "0", the Read enable of EEPROM will be opened. |
| Restriction | |
| Register Availability | Status: Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status: Default Value<br>Power On Sequence: 0<br>S/W Reset: 0<br>H/W Reset: 0 |
| Flow Chart |  |

### 8.1.54. EEPCOUT: EEPROM control out (E1H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EEPCOUT | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | **(E1h)** |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | IC exits the EEPROM control circuit when executing this command. |
| Restriction | |

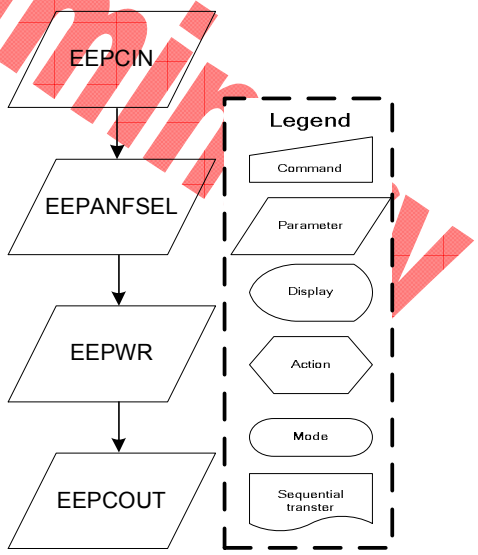
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | -- |
| S/W Reset | -- |
| H/W Reset | -- |

Flow Chart



### 8.1.55. EEPWR: Write to EEPROM (E2H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPCOUT | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | **(E2h)** |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | IC actives trigger to start EEPROM programming when executing this command. |
| Restriction | |

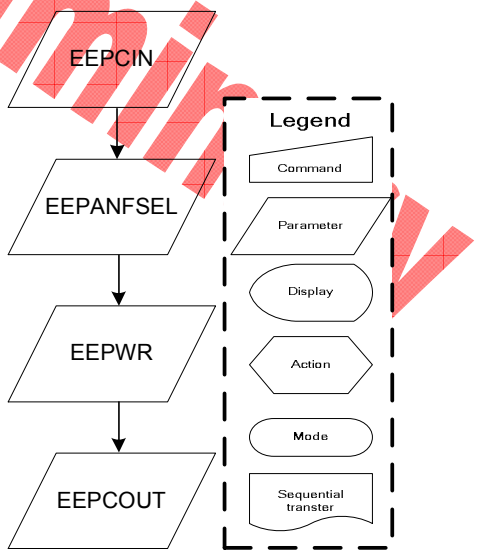
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | -- |
| S/W Reset | -- |
| H/W Reset | -- |

Flow Chart



### 8.1.56. EEPRD: Read from EEPROM (E3H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPMRD | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | **(E3h)** |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | IC actives trigger to start EEPROM data download to circuit when executing this command. |
| Restriction | |

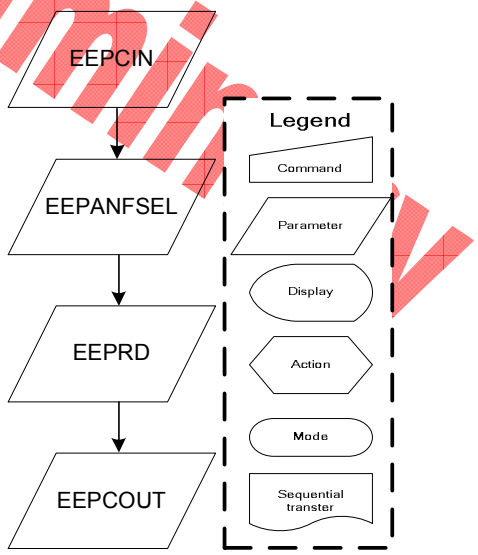
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | -- |
| S/W Reset | -- |
| H/W Reset | -- |

Flow Chart



### 8.1.57. ROMSET: Programmable rom setting (E5H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AutoLoadSet | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | **(E5h)** |
| Parameter | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | **(0Ch)** |

*NOTE: "-" Don't care*

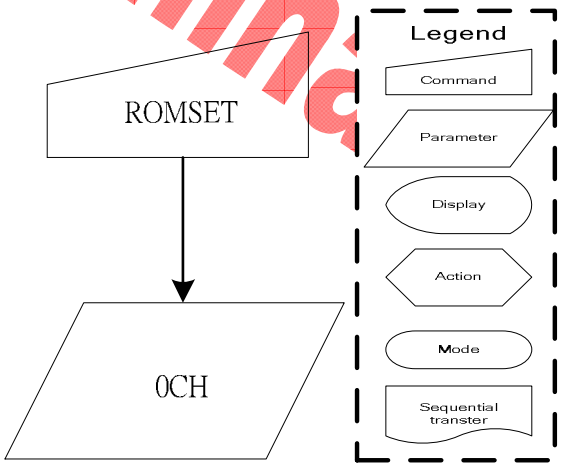
| | |
|---|---|
| Description | Set the EEPROM writing timing. Value 0x0C is the best value for ST7687S. |
| Restriction | |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value D[7:0] |
|---|---|
| Power On Sequence | 0Fh |
| S/W Reset | 0Fh |
| H/W Reset | 0Fh |

Flow Chart



### 8.1.58. FRMSEL: Frame Freq. in Temperature range (F0H)

| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Command** | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | **(F0H)** |
| **1st parameter** | 1 | 1 | 0 | - | - | - | DIVA | FA3 | FA2 | FA1 | FA0 | **Range A** |
| **2nd parameter** | 1 | 1 | 0 | - | - | - | DIVB | FB3 | FB2 | FB1 | FB0 | **Range B** |
| **3rd parameter** | 1 | 1 | 0 | - | - | - | DIVC | FC3 | FC2 | FC1 | FC0 | **Range C** |
| **4th parameter** | 1 | 1 | 0 | - | - | - | DIVD | FD3 | FD2 | FD1 | FD0 | **Range D** |

**Description**

Select Frame Freq. in normal display mode.

1st parameter : Frame freq. value set in temperature range 30(-30℃) to TA

2nd parameter : Frame freq. value set in temperature P range TA to TB

3rd parameter : Frame freq. value set in temperature range TB to TC

4th parameter : Frame freq. value set in temperature range TC to 145(90℃)

For command setting to frame rate value look-up-table, please see the following table:

| DIVx | 1 | | 0 | |
|---|---|---|---|---|
| | Fx[3:0] | Frame Rate (Hz) | Fx[3:0] | Frame Rate (Hz) |
| 1 | 0 | 77.6 | 0 | 38.8 |
| | 1 | 77.6 | 1 | 38.8 |
| | 2 | 77.6 | 2 | 38.8 |
| | 3 | 77.6 | 3 | 38.8 |
| | 4 | 77.6 | 4 | 38.8 |
| | 5 | 97 | 5 | 48.5 |
| | 6 | 97 | 6 | 48.5 |
| | 7 | 97 | 7 | 48.5 |
| | 8 | 97 | 8 | 48.5 |
| | 9 | 97 | 9 | 48.5 |
| | A | 129.3 | A | 64.6 |
| | B | 129.3 | B | 64.6 |
| | C | 129.3 | C | 64.6 |
| | D | 129.3 | D | 64.6 |
| | E | 129.3 | E | 64.6 |
| | F | 194 | F | 97 |

**Restriction**

**Register Availability**

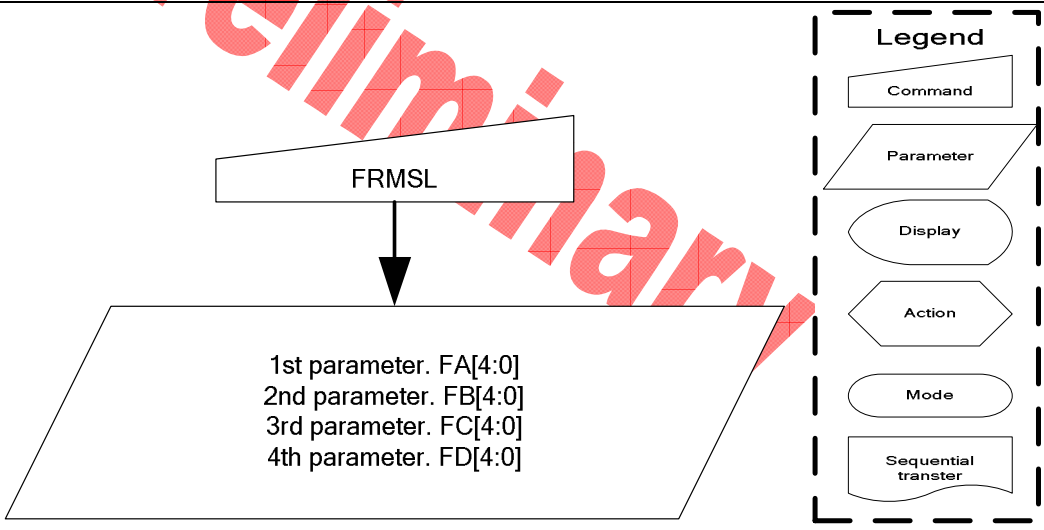
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | | |
|---|---|---|---|---|
| | FA[4:0] | FB[4:0] | FC[4:0] | FD[4:0] |
| Power On Sequence | 06h | 0Bh | 0Dh | 12h |
| S/W Reset | 06h | 0Bh | 0Dh | 12h |
| H/W Reset | 06h | 0Bh | 0Dh | 12h |



**Flow Chart**



### 8.1.59. FRM8SEL: Frame Freq. in Temperature range (idle-8 color) (F1H)

| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Command** | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | **(F1h)** |
| **1st parameter** | 1 | 1 | 0 | - | - | - | F8A4 | F8A3 | F8A2 | F8A1 | F8A0 | **Range A** |
| **2nd parameter** | 1 | 1 | 0 | - | - | - | F8B4 | F8B3 | F8B2 | F8B1 | F8B0 | **Range B** |
| **3rd parameter** | 1 | 1 | 0 | - | - | - | F8C4 | F8C3 | F8C2 | F8C1 | F8C0 | **Range C** |
| **4th parameter** | 1 | 1 | 0 | - | - | - | F8D4 | F8D3 | F8D2 | F8D1 | F8D0 | **Range D** |

**Description**

Select Frame Freq. in normal display mode.(idle;8 color mode)

1st parameter : Frame freq. value set in TEMP range 30(-30℃) to TA

2nd parameter : Frame freq. value set in TEMP range TA to TB

3rd parameter : Frame freq. value set in TEMP range TB to TC

4th parameter : Frame freq. value set in TEMP range TC to 145(90℃)

**Restriction**

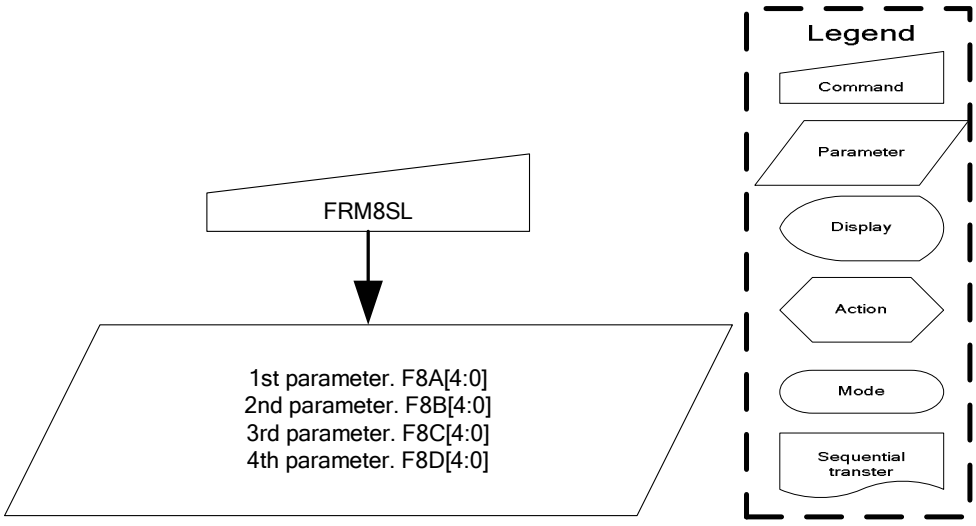
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | | |
|---|---|---|---|---|
| | FA[4:0] | FB[4:0] | FC[4:0] | FD[4:0] |
| Power On Sequence | 06h | 0Bh | 0Dh | 12h |
| S/W Reset | 06h | 0Bh | 0Dh | 12h |
| H/W Reset | 06h | 0Bh | 0Dh | 12h |

**Flow Chart**



### 8.1.60. TMPRNG: Temp. range set for Frame Freq. Adj. (F2H)

| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Command** | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | **(F2h)** |
| **1st parameter** | 1 | 1 | 0 | - | TA6 | TA5 | TA4 | TA3 | TA2 | TA1 | TA0 | **Range A** |
| **2nd parameter** | 1 | 1 | 0 | - | TB6 | TB5 | TB4 | TB3 | TB2 | TB1 | TB0 | **Range B** |
| **3rd parameter** | 1 | 1 | 0 | - | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 | **Range C** |

**Description**

Temp. range set for automatic frame freq. adj. operation according the current temp. value.

1st parameter: Temp. range A value set

2nd parameter: Temp. range B value set

3rd parameter: Temp. range C value set

**TA/TB/TC Temperature(℃) + 40 = TA/TB/TC[6 :0]**

Example:

If TA wants to be set at 24℃, TA[6:0]=24+40=64(40h),

**Restriction**

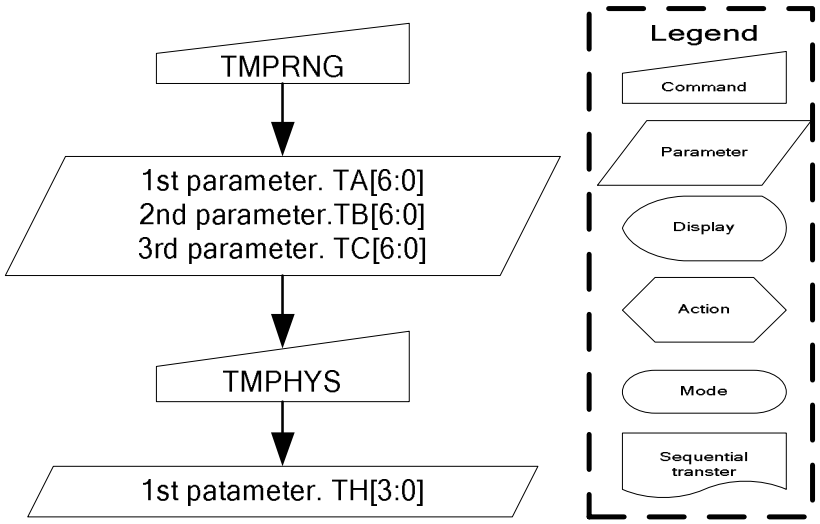
-40℃≦TA≦TA+TH≦TB≦TB+TH≦TC≦87℃

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | TA[6:0] | TB[6:0] | TC[6:0] |
| Power On Sequence | 1Eh | 28h | 32h |
| S/W Reset | 1Eh | 28h | 32h |
| H/W Reset | 1Eh | 28h | 32h |

| Flow Chart |  |
|---|---|

### 8.1.61. TMPHYS: Temp. Hysteresis Set for Frame Freq. Adj. (F3H)

| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Command** | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | **(F3h)** |
| **1st parameter** | 1 | 1 | 0 | - | - | - | - | TH3 | TH2 | TH1 | TH0 | |

**Description**

Temp. hysteresis range set for frame freq. adj.

Parameter TH[3:0] is used to set Temp. hysteresis range.

The relationship between temp. state and temp. range value is shown below.

| TEMP Range Value | TEMP Rising State | TEMP Falling State |
|---|---|---|
| Freq. changing point A | TA[6:0]+TH[3:0] | TA[6:0] |
| Freq. changing point B | TB[6:0]+TH[3:0] | TB[6:0] |
| Freq. changing point C | TC[6:0]+TH[3:0] | TC[6:0] |

**TH Temperature(℃) – 1 = TH[3:0]**

Example:

If TH wants to set 5℃, TH[3:0]=5-1=4.

**Restriction**

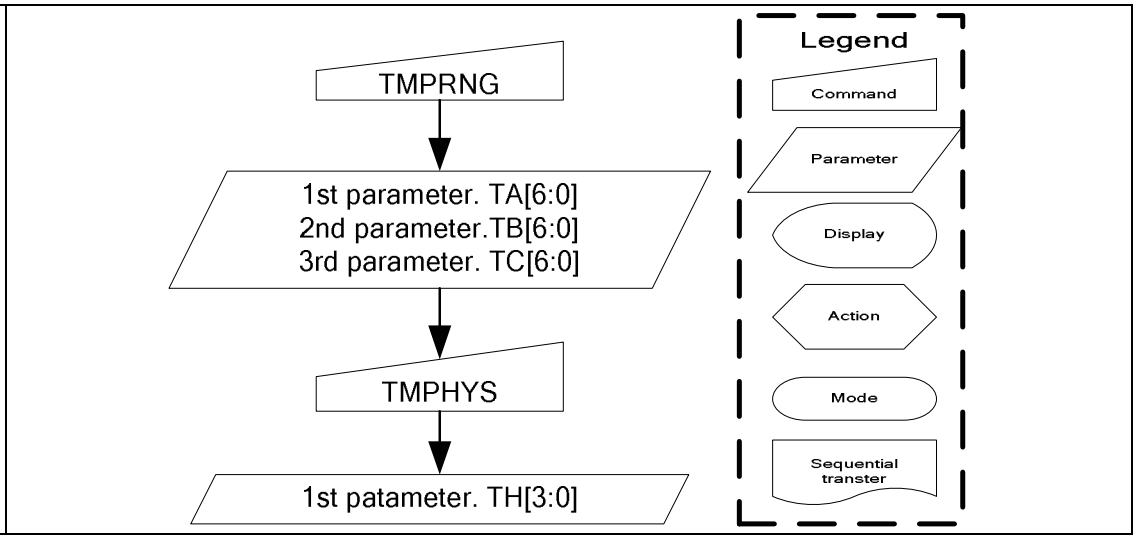
Temp. hysteresis value should be smaller than the gap of temp. range.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value(TH[3:0]) |
|---|---|
| Power On Sequence | 02h |
| S/W Reset | 02h |
| H/W Reset | 02h |

| Flow Chart |  |
|---|---|

### 8.1.62. TEMPSEL: Temperature Gradient Compensation Coefficient Set (F4H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEMPSEL | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | **(F4h)** |
| 1st parameter | 1 | 1 | 0 | MT13 | MT12 | MT11 | MT10 | MT03 | MT02 | MT01 | MT00 | MT1x: (-24 °C to -32 °C)<br>MT0x: (-32 °C to -40 °C) |
| 2nd parameter | 1 | 1 | 0 | MT33 | MT32 | MT31 | MT30 | MT23 | MT22 | MT21 | MT20 | MT3x: (-8 °C to -16 °C)<br>MT2x: (-16 °C to -24 °C) |
| 3rd parameter | 1 | 1 | 0 | MT53 | MT52 | MT51 | MT50 | MT43 | MT42 | MT41 | MT40 | MT5x: (8 °C to 0 °C)<br>MT4x: (0 °C to -8 °C) |
| 4th parameter | 1 | 1 | 0 | MT73 | MT72 | MT71 | MT70 | MT63 | MT62 | MT61 | MT60 | MT7x: (24 °C to16 °C)<br>MT6x: (16 °C to 8 °C) |
| 5th parameter | 1 | 1 | 0 | MT93 | MT92 | MT91 | MT90 | MT83 | MT82 | MT81 | MT80 | MT9x: (40 °C to 32 °C)<br>MT8x: (32 °C to 24 °C) |
| 6th parameter | 1 | 1 | 0 | MTB3 | MTB2 | MTB1 | MTB0 | MTA3 | MTA2 | MTA1 | MTA0 | MTBx: (56 °C to 48 °C)<br>MTAx: (48 °C to 40 °C) |
| 7th parameter | 1 | 1 | 0 | MTD3 | MTD2 | MTD1 | MTD0 | MTC3 | MTC2 | MTC1 | MTC0 | MTDx: (72 °C to 64 °C)<br>MTCx: (64 °C to 56 °C) |
| 8th parameter | 1 | 1 | 0 | MTF3 | MTF2 | MTF1 | MTF0 | MTE3 | MTE2 | MTE1 | MTE0 | MTFx: (87 °C to 80 °C)<br>MTEx: (80 °C to 72 °C) |

*NOTE: "-" Don't care*



**Description**

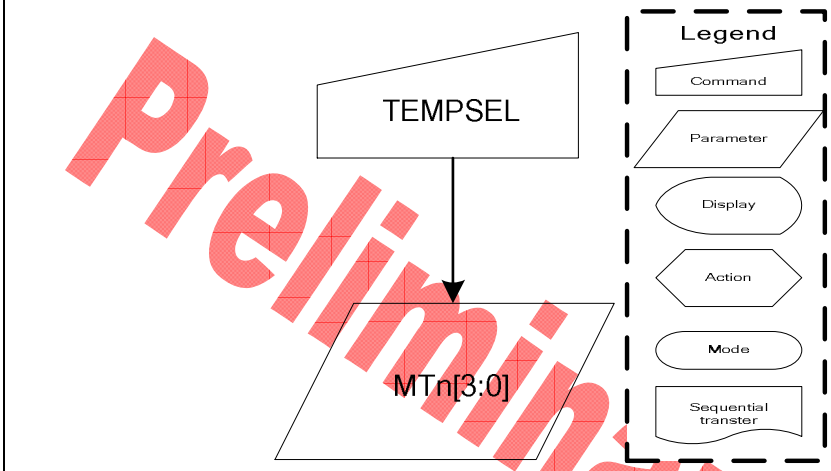
This command defines temperature gradient compensation coefficient. For this command detail description and opearation, please see Section 7.10.

| Parameter n | MT n 3 | MT n 2 | MT n 1 | MT n 0 | Voltage / °C |
|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **+5 mv / °C** |
| **1** | **0** | **0** | **0** | **1** | **0 mv / °C** |
| **2** | **0** | **0** | **1** | **0** | **-5 mv / °C** |
| **3** | **0** | **0** | **1** | **1** | **-10 mv / °C** |
| : | : | : | : | : | : |
| : | : | : | : | : | : |
| : | : | : | : | : | : |
| **12** | **1** | **1** | **0** | **0** | **-55 mv / °C** |
| **13** | **1** | **1** | **0** | **1** | **-60 mv / °C** |
| **14** | **1** | **1** | **1** | **0** | **-65 mv / °C** |
| **15** | **1** | **1** | **1** | **1** | **-70 mv / °C** |

**Voltage / °C (+/- 3mv tolerance)**

**Restriction**

Please refer to the specification in absolute maximum ratings for operating voltage range.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value (MTn[3:0])</td></tr>
<tr><td>Power On Sequence</td><td>--</td></tr>
<tr><td>S/W Reset</td><td>--</td></tr>
<tr><td>H/W Reset</td><td>--</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>



*NOTE:*

**The default value of temperature gradient compensation coefficient Set**

| | |
|---|---|
| **1st parameter** | 0xFF |
| **2nd parameter** | 0x36 |
| **3rd parameter** | 0x04 |
| **4th parameter** | 0x00 |
| **5th parameter** | 0x33 |
| **6th parameter** | 0x42 |
| **7th parameter** | 0xC4 |
| **8th parameter** | 0x59 |

### 8.1.63. THYS : Temperature detection threshold(F7H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THYS | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | **(F7h)** |
| Parameter | 1 | 1 | 0 | THYS7 | THYS6 | THYS5 | THYS4 | THYS3 | THYS2 | THYS1 | THYS0 | - |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | Temperature detection threshold setting. |
| Restriction | |

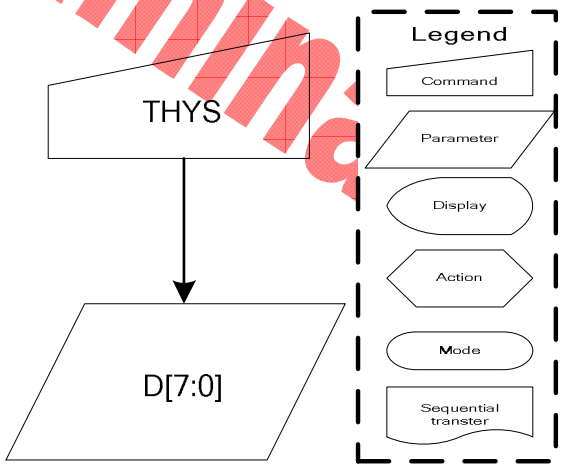
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value D[7:0] |
|---|---|
| Power On Sequence | 08h |
| S/W Reset | 08h |
| H/W Reset | 08h |

Flow Chart



### 8.1.64. Frame Set: Frame PWM Set (F9H)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Frame1 Set | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | **(F9h)** |
| 1st parameter | 1 | 1 | 0 | - | - | - | P14 | P13 | P12 | P11 | P10 | - |
| 2nd parameter | 1 | 1 | 0 | - | - | - | P24 | P23 | P22 | P21 | P20 | - |
| : | : | : | : | : | : | : | : | : | : | : | : | - |
| 15th parameter | 1 | 1 | 0 | - | - | - | P154 | P153 | P152 | P151 | P150 | - |
| 16th parameter | 1 | 1 | 0 | - | - | - | P164 | P163 | P162 | P161 | P160 | - |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | This command is used to set frame PWM. |
| Restriction | |

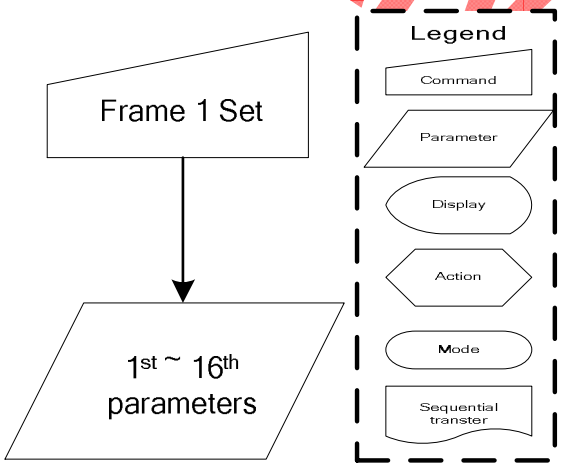
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | -- |
| S/W Reset | -- |
| H/W Reset | -- |

Flow Chart



*NOTE:*

**The default value of RGB level set**

| | |
|---|---|
| **RGB level0** | 00 |
| **RGB level1** | 02 |
| **RGB level2** | 04 |
| **RGB level3** | 06 |
| **RGB level4** | 08 |
| **RGB level5** | 0A |
| **RGB level6** | 0C |
| **RGB level7** | 0E |
| **RGB level8** | 10 |
| **RGB level9** | 12 |
| **RGB level10** | 14 |
| **RGB level11** | 16 |
| **RGB level12** | 18 |
| **RGB level13** | 1A |
| **RGB level14** | 1C |
| **RGB level15** | 1E |

All the modulation range of each level for each frame is from 00'H to 1F'H.

### 8.1.65. EEPANFSEL: EEPROM Function Selection (FAH)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THYS | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | **(FAh)** |
| Parameter | 1 | 1 | 0 | 0 | 0 | 0 | 0 | - | ERAE | WRE | - | **-** |

*NOTE: "-" Don't care*

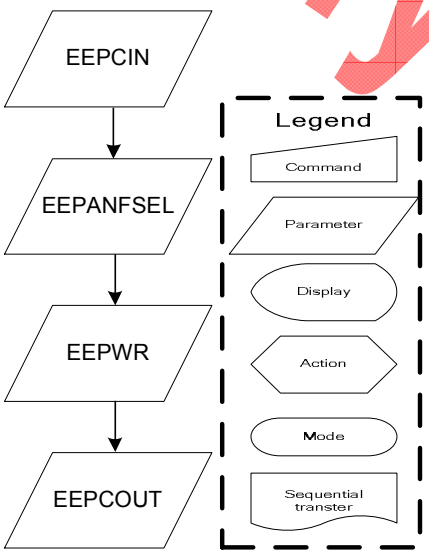
| | |
|---|---|
| Description | ERAE : EEPROM erase enable control, 1: EEPROM erase enable, 0 : EEPROM erase disable<br>WRE : EEPROM write enable control, 1: EEPROM write enable, 0 : EEPROM write disable |
| Restriction | |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default ValueD[7:0] |
|---|---|
| Power On Sequence | 08h |
| S/W Reset | 08h |
| H/W Reset | 08h |

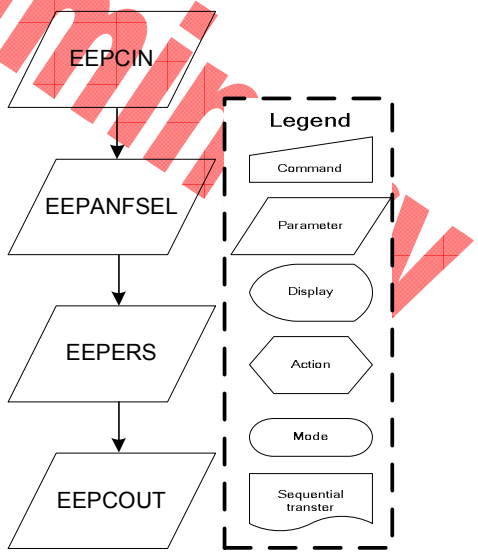
Flow Chart



### 8.1.66. EEPERS: Erase EEPROM (FBH)

| *Command* | *A0* | */RD* | */WR* | *D7* | *D6* | *D5* | *D4* | *D3* | *D2* | *D1* | *D0* | *Hex* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EEPCOUT | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | **(FBh)** |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | Erase EEPROM |
| Restriction | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / --<br>S/W Reset / --<br>H/W Reset / -- |
| Flow Chart |  |

# 9. SPECIFICATIONS

## 9.1 ABSOLUTE MAXIMUM RATINGS

(VSS = 0V)

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage 1 | $V_{DD}$ | - 0.3 ~ + 3.6 | V |
| Supply voltage 2 | $V_{DD2,VDD3,VDD4,VDD5}$ | - 0.3 ~ + 3.6 | V |
| Supply voltage 3 | $V_{LCD}$ (V0- XV0) | - 0.3 ~ + 18.0 | V |
| Input voltage range | $V_{IN}$ | - 0.3 ~ $V_{DD}$ + 0.3 | V |
| Operating temperature range | $T_{OPR}$ | - 30 ~ + 85 | ℃ |
| Storage temperature range | $T_{STG}$ | - 40 ~ + 125 | ℃ |

*NOTE:*

*(1). Voltages are all based on VSS = 0V.*

*(2). Voltage relationship: V0 > Vg > Vm > VSS > XV0 must always be satisfied.*

## 9.2 DC CHARACTERISTICS

### 9.2.1. Basic Characteristics

($V_{SS}$=0V , Ta = -30 to 85℃)

| Parameter | Symbol | Conditions | Related Pins | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Logic Operating voltage | $V_{DDI}$ | - | *2)VDD | 1.65 | 1.8 | 3.3 | V |
| Analog Operating voltage | $V_{DDA}$ | - | *2)VDD2,3,4,5 | 2.4 | 2.8 | 3.3 | |
| Voltage Regulator input voltage | $VD1_{in}$ | Regulator off | $VD1_{in}$ | 1.65 | - | 2.8 | |
| Driving voltage input | $V_{LCD}$ | V0 – XV0 | *3)V0, XV0 | - | - | 18.0 | |
| High level input voltage | $V_{IH}$ | | *1) *2) | 0.7$V_{DD}$ | - | $V_{DD}$ | |
| Low level input voltage | $V_{IL}$ | - | *1) *2) | $V_{SS}$ | - | 0.3$V_{DD}$ | |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA | *2) SI, TE | 0.8$V_{DD}$ | - | $V_{DD}$ | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = +1.0mA | | $V_{SS}$ | - | 0.2$V_{DD}$ | |
| Input leakage current | $I_{IL}$ | $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | *1) *2) | -1.0 | - | +1.0 | μA |
| Driver on resistance (SEG) | $R_{ONSEG}$ | Vg = 2.8V, Ta=25℃ | S0 to S383 | - | 1 | - | KΩ |
| Driver on resistance (COM) | $R_{ONCOM}$ | V0 = 14.0V, Ta=25℃ | C0 to C127 | - | 0.8 | - | |
| Frame rate | FR | Ta=25℃, n-line=0x00, Duty=128, FR=0x12 | - | - | 77 | - | kHz |
| Voltage follower output range | Vm | | - | 0.7 | Vg/2 | VDDA-0.7 | V |
| Booster2 output voltage range | Vg | | - | 1.8 | - | VDDAX2 | V |

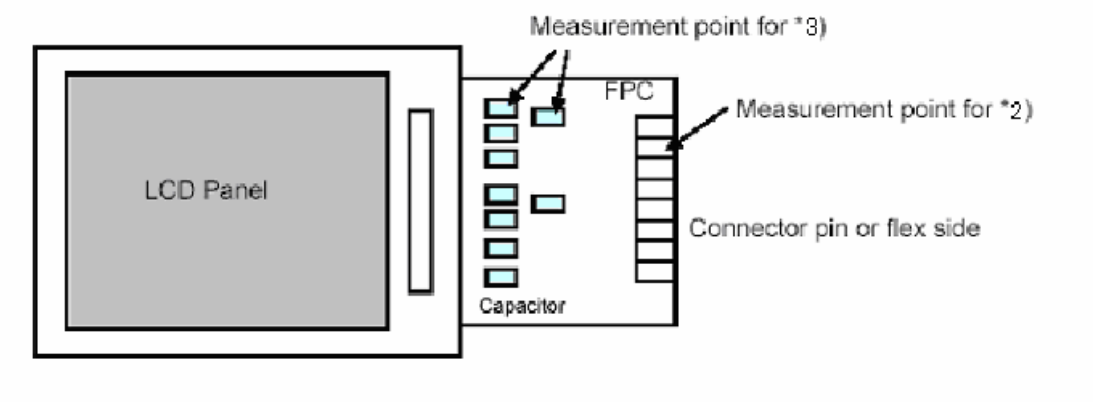




*NOTE:*

**1) Applies to IF1, IF2, IF3, /CS, /RST, /WR, /RD, A0(SCL) and D7-D2, D1 (A0) ,D0(SI) pins*

**2) *3) When the measurements are performed with LCD module, Measurement Points are like below.*



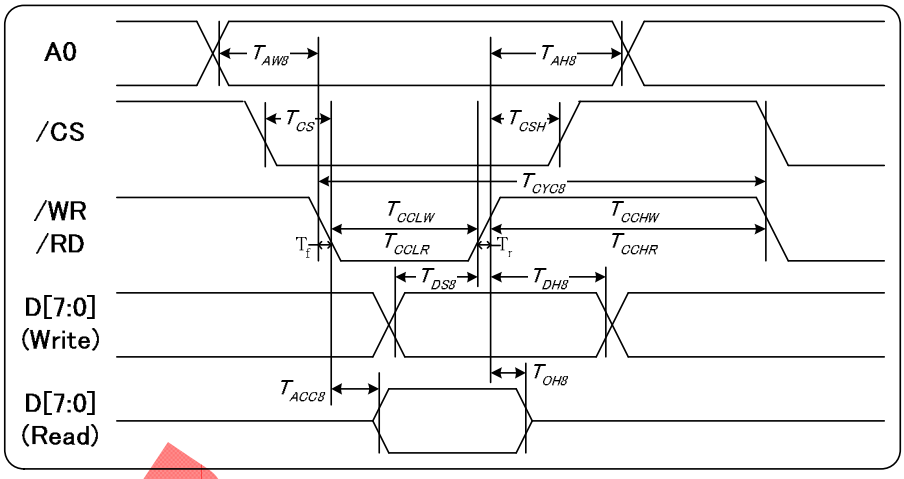
### 9.2.2. Current Consumption (Bare die)

| Operation mode | Condition | Current consumption | |
|---|---|---|---|
| | | Typical | Maximum |
| | | IDD (mA) | IDD (mA) |
| - Normal Mode | 1. 1/2 gray pattern<br>2. Vddi=1.8V, Vdda=2.8V<br>3. Vop=14V, bias=1/9, n-line=0x00,<br>FR=77Hz, x8 booster, Ta=25℃ | 0.6 | 0.9 |
| - Sleep In Mode | Vddi=1.8V, Vdda=2.8V, Ta=25℃ | 0.01 | 0.02 |

*Note:*
*The current consumption is DC characteristic.*

# 10. TIMING CHARACTERISTICS

## 10.1 Parallel Interface Characteristics bus (8080-series MCU)




($V_{DDA}$=2.4 to 3.3V, $V_{DDi}$=1.65 to 3.3V, Ta= 25℃, die)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0 | $T_{AH8}$ | | 0 | — | ns |
| Address setup time | | $T_{AW8}$ | | 0 | — | |
| Chip select setup time | /CS | $T_{CS}$ | | 10 | — | |
| Chip select hold time | | $T_{CSH}$ | | 10 | — | |
| System cycle time (WRITE) | WR | $T_{CYC8}$ | | 200 | — | |
| /WR L pulse width (WRITE) | | $T_{CCLW}$ | | 80 | — | |
| /WR H pulse width (WRITE) | | $T_{CCHW}$ | | 80 | — | |
| System cycle time (READ) | RD (ID) | $T_{CYC8}$ | When read ID data | 200 | — | |
| /RD L pulse width (READ) | | $T_{CCLR}$ | | 80 | — | |
| /RD H pulse width (READ) | | $T_{CCHR}$ | | 80 | — | |
| System cycle time (READ) | RD (FM) | $T_{CYC8}$ | When read from frame memory | 400 | — | |
| /RD L pulse width (READ) | | $T_{CCLR}$ | | 200 | — | |
| /RD H pulse width (READ) | | $T_{CCHR}$ | | 140 | — | |
| WRITE data setup time | D0 to D7 | $T_{DS8}$ | | 15 | — | |
| WRITE data hold time | | $T_{DH8}$ | | 15 | — | |
| READ access time (ID) | | $T_{ACC8}$ (ID) | | — | 60 | |
| READ access time (FM) | | $T_{ACC8}$ (FM) | CL = 30 pF | — | 90 | |
| READ Output disable time | | $T_{OH8}$ | CL = 30 pF | — | 80 | |

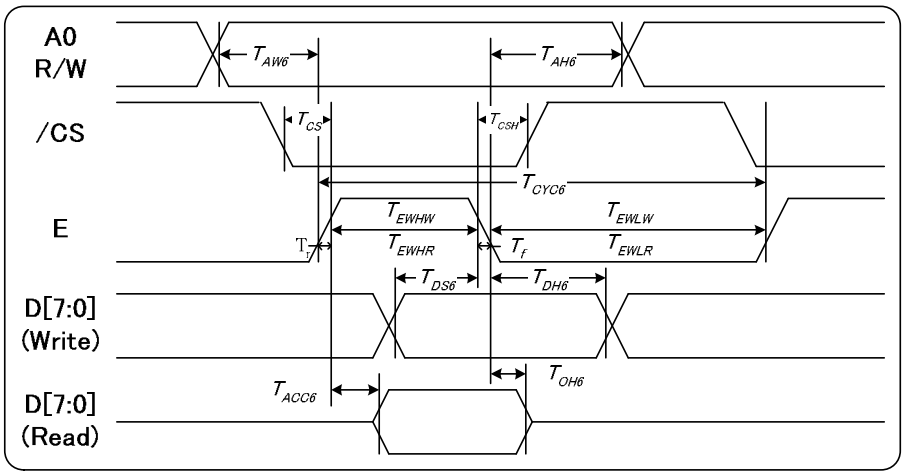


*1 The input signal rise time and fall time ($T_r$, $T_f$) is specified at 15 ns or less. When the system cycle time is extremely fast, ($T_r + T_f$) ≦ ($T_{CYC8} - T_{CCLW} - T_{CCHW}$) for ($T_r + T_f$) ≦ ($T_{CYC8} - T_{CCLR} - T_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 $T_{CCLW}$ and $T_{CCLR}$ are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

## 10.2 Parallel Interface Characteristics bus (6800-series MCU)




($V_{DDA}$=2.4 to 3.3V, $V_{DDi}$=1.65 to 3.3V, Ta= 25℃, die)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0 | $T_{AH6}$ | | 0 | — | ns |
| Address setup time | | $T_{AW6}$ | | 0 | — | |
| Chip select setup time | /CS | $T_{CS}$ | | 10 | — | |
| Chip select hold time | | $T_{CSH}$ | | 10 | — | |
| System cycle time (WRITE) | E | $T_{CYC6}$ | | 200 | — | |
| Low pulse width (WRITE) | | $T_{EWLW}$ | | 60 | — | |
| High pulse width (WRITE) | | $T_{EWHW}$ | | 80 | — | |
| System cycle time (READ) | RW (ID) | $T_{CYC6}$ | When read ID data | 200 | — | |
| Low pulse width (READ) | | $T_{EWLR}$ | | 70 | — | |
| High pulse width (READ) | | $T_{EWHR}$ | | 80 | — | |
| System cycle time (READ) | RW (FM) | $T_{CYC8}$ | When read from frame memory | 400 | — | |
| Low pulse width (READ) | | $T_{CCLR}$ | | 200 | — | |
| High pulse width (READ) | | $T_{CCHR}$ | | 140 | — | |
| WRITE data setup time | D0 to D7 | $T_{DS6}$ | | 15 | — | |
| WRITE data hold time | | $T_{DH6}$ | | 15 | — | |
| READ access time (ID) | | $T_{ACC6}$ (ID) | | — | 60 | |
| READ access time (FM) | | $T_{ACC6}$ (FM) | CL = 30 pF | — | 90 | |
| READ Output disable time | | $T_{OH6}$ | CL = 30 pF | — | 80 | |

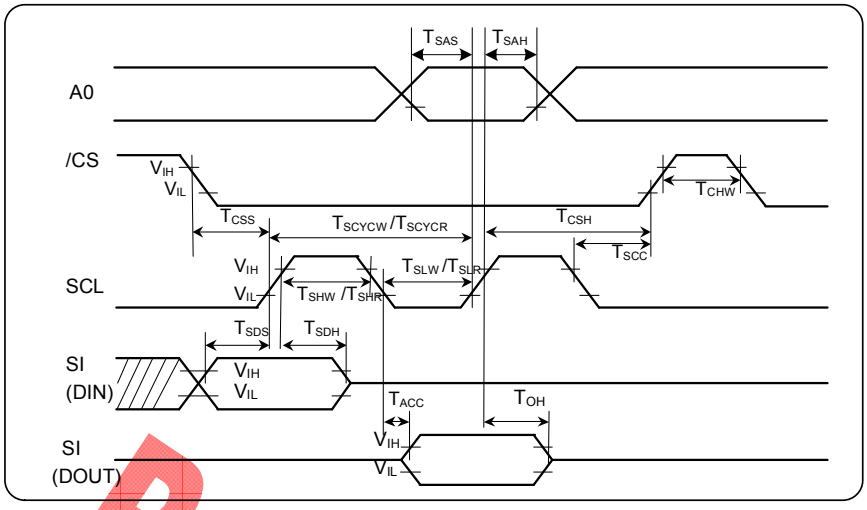


*1 The input signal rise time and fall time ($T_r$, $T_f$) is specified at 15 ns or less. When the system cycle time is extremely fast, ($T_r + T_f$) ≦ ($T_{CYC6} - T_{EWLW} - T_{EWHW}$) for ($T_r + T_f$) ≦ ($T_{CYC6} - T_{EWLR} - T_{EWHR}$) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 $t_{EWLW}$ and $t_{EWLR}$ are specified as the overlap between /CS being “L” and E.

## 10.3 Serial Interface Characteristics (4-pin Serial)





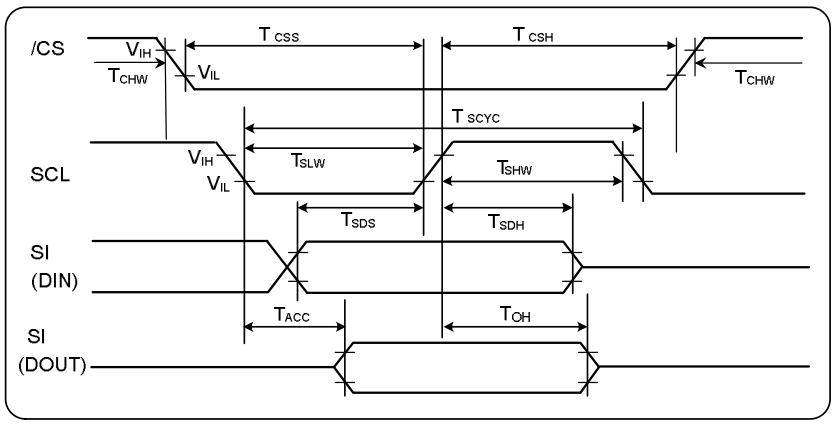

($V_{DDA}$=2.4 to 3.3V, $V_{DDI}$=1.65 to 3.3V, Ta= 25℃, die)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Serial clock period (write) | SCL | $T_{SCYCW}$ | | 70 | — | ns |
| SCL “H” pulse width (write) | | $T_{SHW}$ | | 35 | — | |
| SCL “L” pulse width (write) | | $T_{SLW}$ | | 35 | — | |
| Serial clock period (read) | | $T_{SCYCR}$ | | 150 | — | |
| SCL “H” pulse width (read) | | $T_{SHR}$ | | 70 | — | |
| SCL “L” pulse width (read) | | $T_{SLR}$ | | 70 | — | |
| Address setup time | A0 | $T_{SAS}$ | | 10 | — | |
| Address hold time | | $T_{SAH}$ | | 10 | — | |
| Data setup time | SI | $T_{SDS}$ | | 10 | — | |
| Data hold time | | $T_{SDH}$ | | 10 | — | |
| Data access time | | $T_{ACC}$ | CL = 30 pF | — | 60 | |
| Output disable time | | $T_{OH}$ | CL = 30 pF | — | 60 | |
| Chip select setup time | /CS | $T_{CSS}$ | | 35 | — | |
| Chip select hold time | | $T_{CSH}$ | | 35 | — | |
| Chip select “H” pulse width | | $T_{CHW}$ | | 0 | — | |

*1 The input signal rise and fall time ($T_r$, $T_f$) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

## 10.4 Serial Interface Characteristics (3-pin Serial)





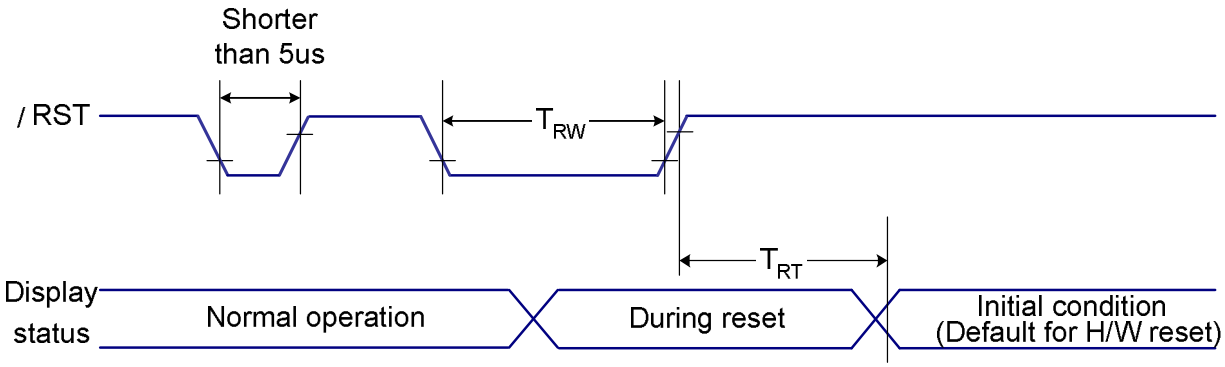

($V_{DDA}$=2.4 to 3.3V, $V_{DDI}$=1.65 to 3.3V, Ta= 25℃, die)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Serial clock period (write) | SCL | $T_{SCYC}$ | | 70 | — | ns |
| SCL “H” pulse width (write) | | $T_{SHW}$ | | 35 | — | |
| SCL “L” pulse width (write) | | $T_{SLW}$ | | 35 | — | |
| Serial clock period (read) | | $T_{SCYC}$ | | 150 | — | |
| SCL “H” pulse width (read) | | $T_{SHW}$ | | 70 | — | |
| SCL “L” pulse width (read) | | $T_{SLW}$ | | 70 | — | |
| Data setup time | SI | $T_{SDS}$ | | 10 | — | |
| Data hold time | | $T_{SDH}$ | | 10 | — | |
| Access time | | $T_{ACC}$ | CL = 30 pF | — | 60 | |
| Output disable time | | $T_{OH}$ | CL = 30 pF | — | 60 | |
| Chip select setup time | /CS | $T_{CSS}$ | | 35 | — | |
| Chip select hold time | | $T_{CSH}$ | | 35 | — | |
| Chip select “H” pulse width | | $T_{CHW}$ | | 0 | — | |

*1 The input signal rise and fall time ($T_r$, $T_f$) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

## 11. RESET TIMING




($V_{DDA}$=2.4 to 3.3V, $V_{DDI}$=1.65 to 3.3V, Ta = 25℃)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Reset “L” pulse width | /RST | $T_{RW}$ | | 10us | — | us |
| Reset time | | $T_{RT}$ | | 5 (*note 5) | — | ms |
| Reset time | | $T_{RT}$ | | 120 (*note 6,7) | — | ms |



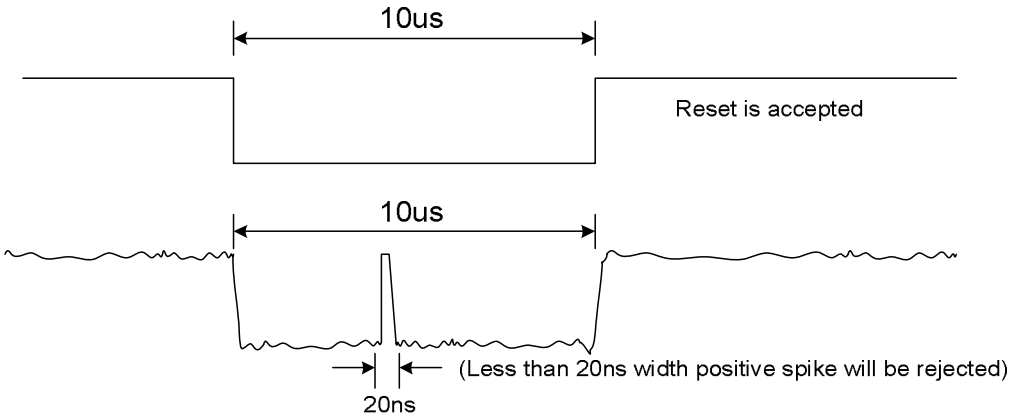
*Notes:*

*1. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below:*

| RST Pulse | Action |
|---|---|
| Shorter than 3μs | Reset Rejected |
| Longer than 9μs | Reset |
| Between 3μs and 9μs | Reset starts |

*2. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.*

*3. Spike Rejection also applies during a valid reset pulse as shown below:*




*5. When Reset applied during Sleep In Mode.*

*6. When Reset applied during Sleep Out Mode.*

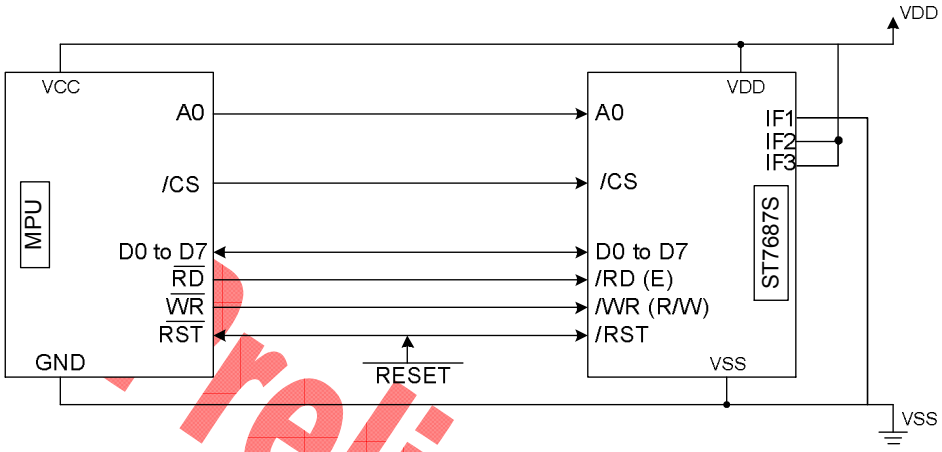
*7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.*

# 12. THE MPU INTERFACE (REFERENCE EXAMPLES)

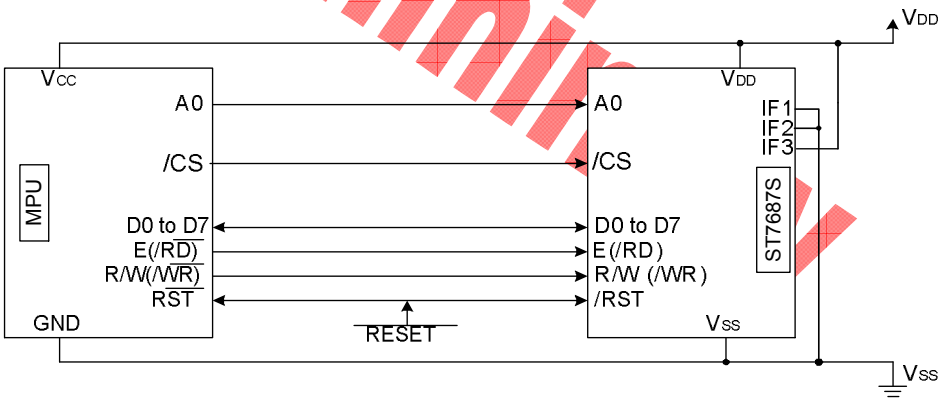
The ST7687S Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7687S series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7687S Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

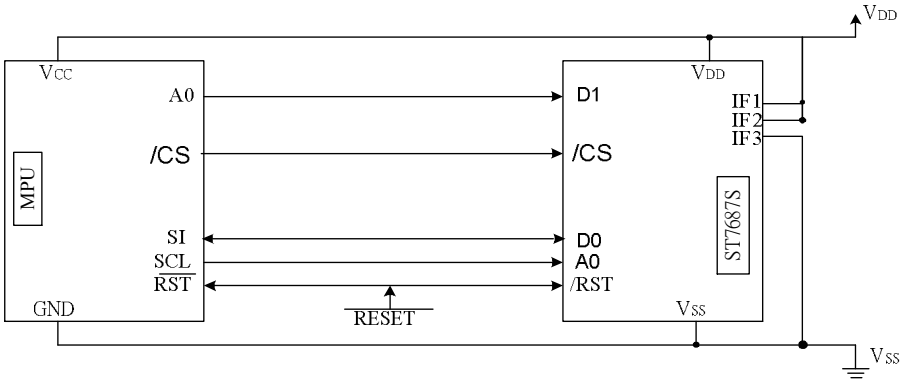
(1) 8080 Series MPUs



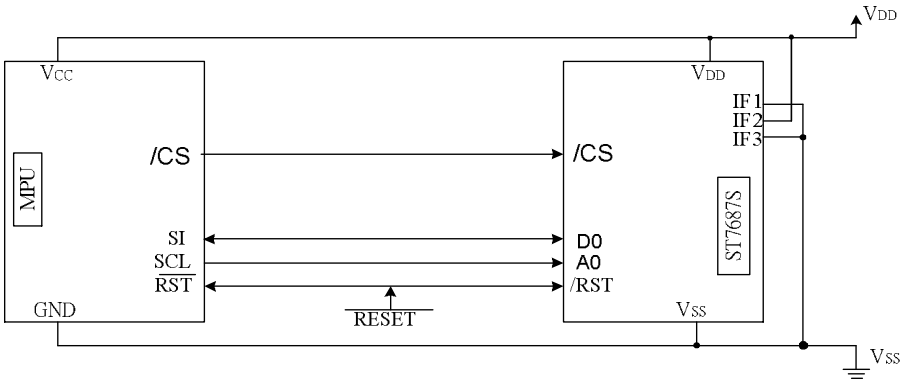

(2) 6800 Series MPUs




(3) Using the Serial Interface (4-line interface)



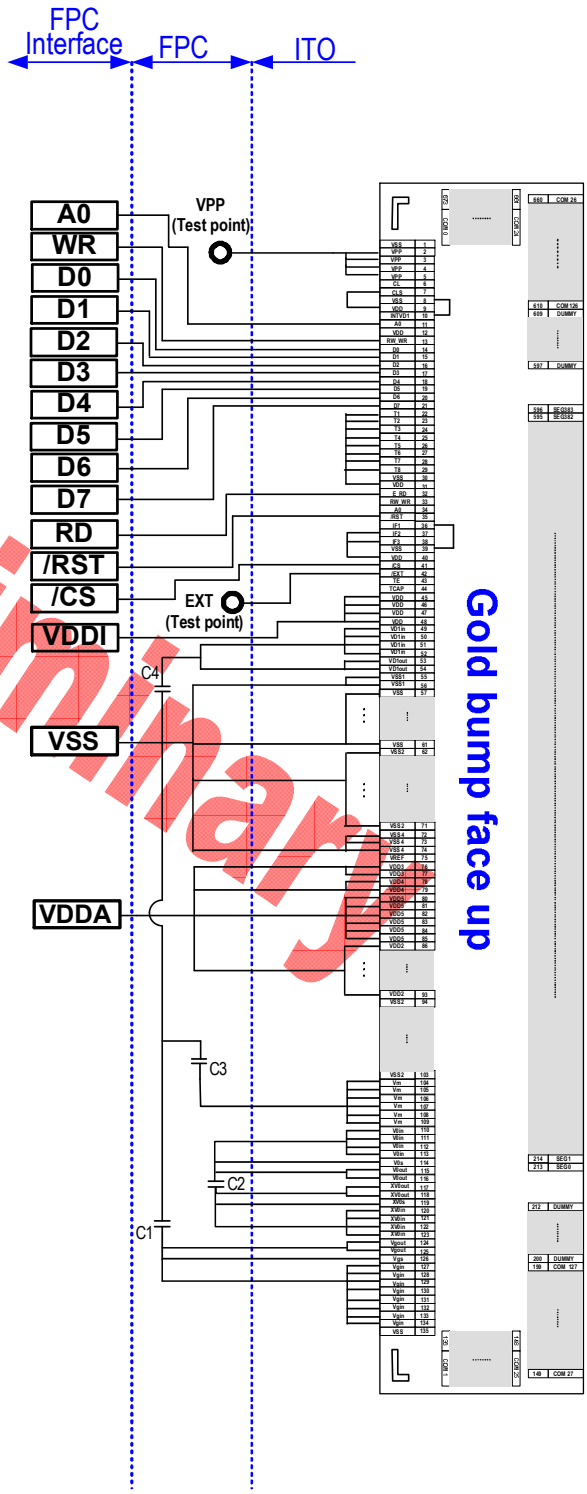
(4) Using the Serial Interface (3-line interface)



# A – Application Note

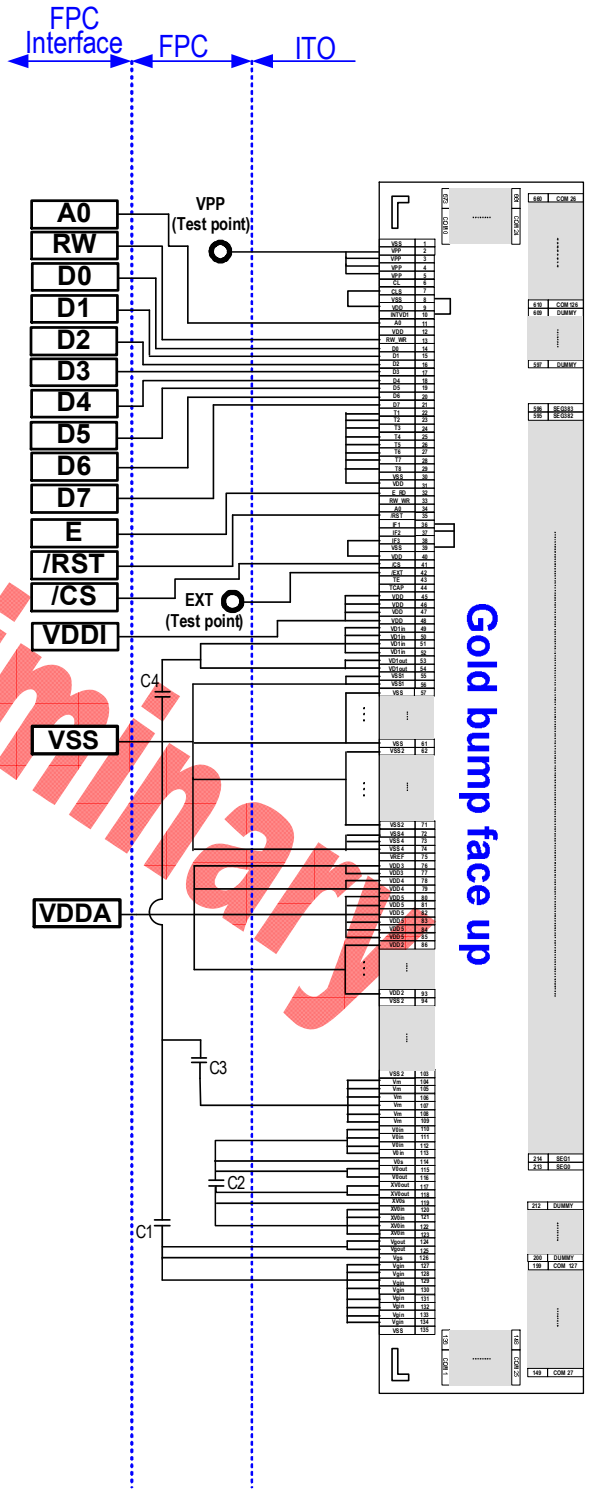
## A1a – 80-8bit parallel interlace Mode

| | |
|---|---|
| **Typical VDDI** | 1.8V/2.8V |
| **VDDA** | 2.4V≦VDDA≦3.3V |
| **IF[3:1]** | HHL |
| **CLS** | H (internal OSC) |
| **INTVD1** | L |
| **C1** | 1uF/16V |
| **C2** | 1uF/25V |
| **C3** | 1uF/16V |
| **C4** | 1uF/16V (optional) |



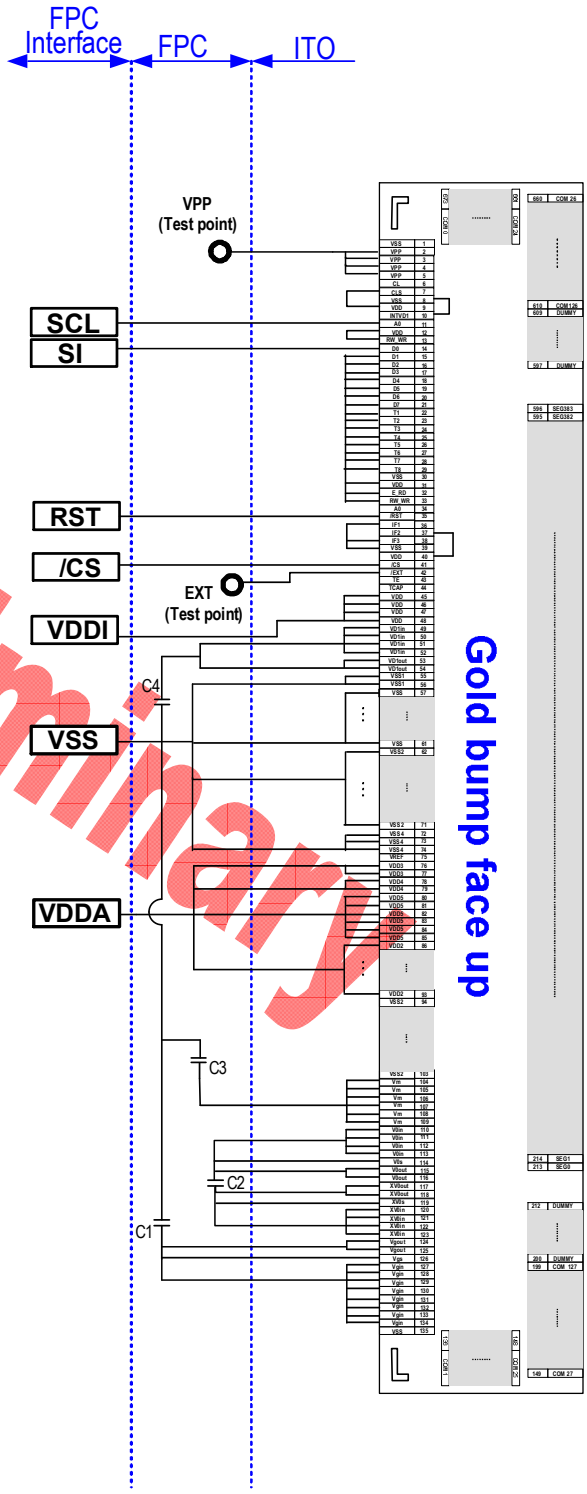
### A1c –68-8bit parallel interlace Mode

| | |
|---|---|
| **Typical VDDI** | 1.8V/2.8V |
| **VDDA** | 2.4V≦VDDA≦3.3V |
| **IF[3:1]** | HLL |
| **CLS** | H (internal OSC) |
| **INTVD1** | L |
| **C1** | 1uF/16V |
| **C2** | 1uF/25V |
| **C3** | 1uF/16V |
| **C4** | 1uF/16V (optional) |



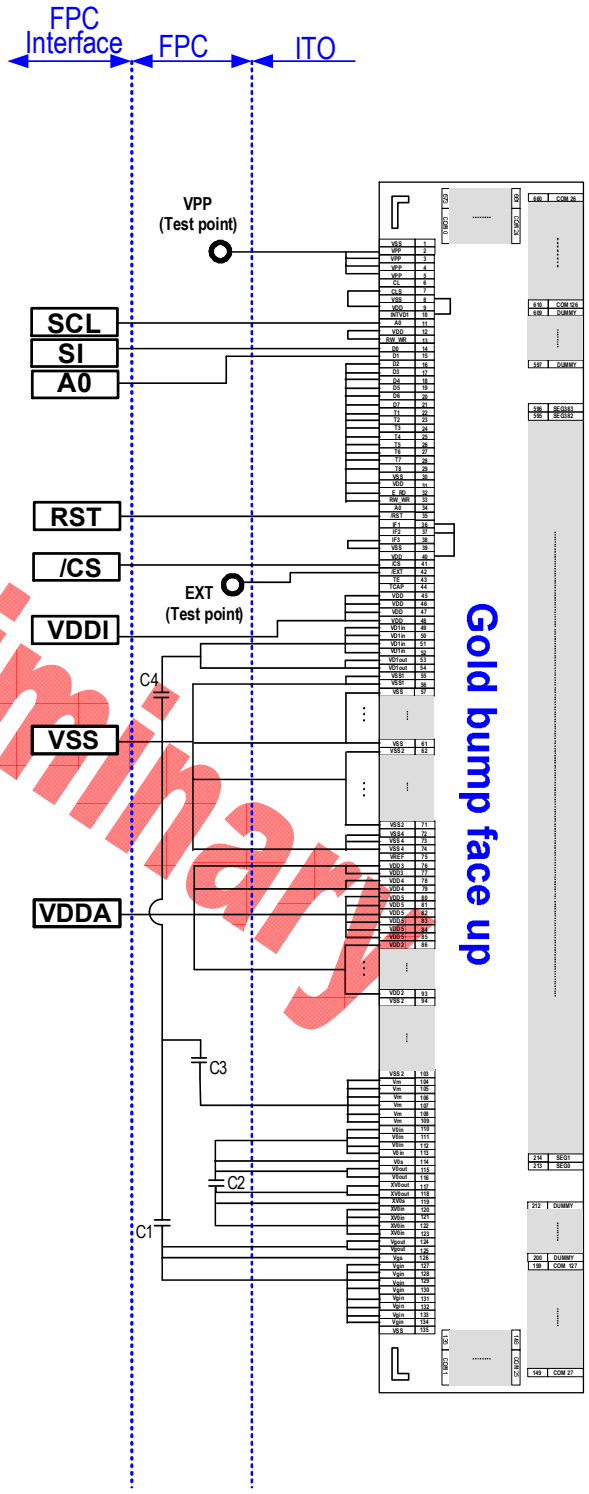
### A1e –3-line serial interlace Mode

| | |
|---|---|
| **Typical VDDI** | 1.8V/2.8V |
| **VDDA** | 2.4V≦VDDA≦3.3V |
| **IF[3:1]** | LHL |
| **CLS** | H (internal OSC) |
| **INTVD1** | L |
| **C1** | 1uF/16V |
| **C2** | 1uF/25V |
| **C3** | 1uF/16V |
| **C4** | 1uF/16V (optional) |



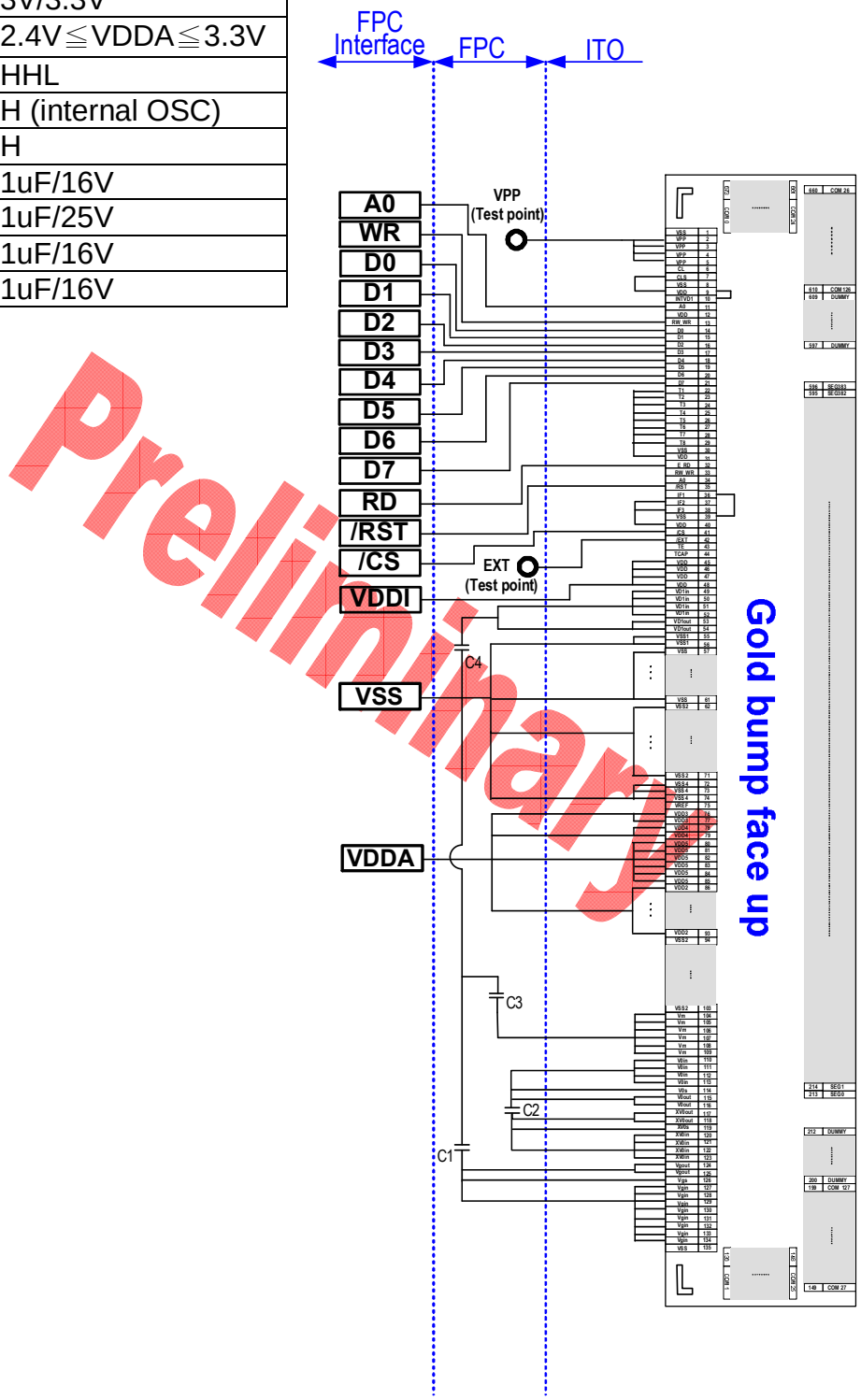
### A1f – 4-line serial interlace Mode

| | |
|---|---|
| **Typical VDDI** | 1.8V/2.8V |
| **VDDA** | 2.4V≦VDDA≦3.3V |
| **IF[3:1]** | LHH |
| **CLS** | H (internal OSC) |
| **INTVD1** | L |
| **C1** | 1uF/16V |
| **C2** | 1uF/25V |
| **C3** | 1uF/16V |
| **C4** | 1uF/16V (optional) |



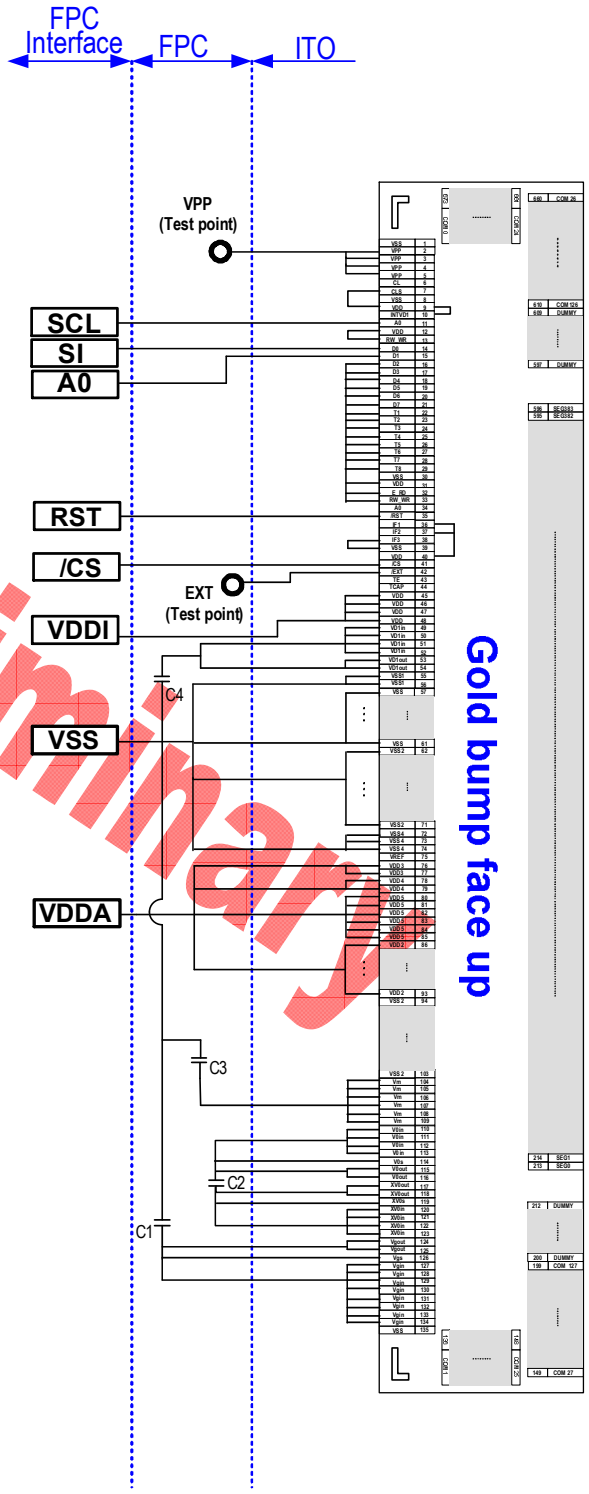
### A1g –80-8bit parallel interlace Mode while typical Vddi=3V/3.3V

| | |
|---|---|
| **Typical VDDI** | 3V/3.3V |
| **VDDA** | 2.4V≦VDDA≦3.3V |
| **IF[3:1]** | HHL |
| **CLS** | H (internal OSC) |
| **INTVD1** | H |
| **C1** | 1uF/16V |
| **C2** | 1uF/25V |
| **C3** | 1uF/16V |
| **C4** | 1uF/16V |



### A1h – 4-line serial interlace Mode while typical Vddi=3V/3.3V

| | |
|---|---|
| **Typical VDDI** | 3V/3.3V |
| **VDDA** | 2.4V≦VDDA≦3.3V |
| **IF[3:1]** | LHH |
| **CLS** | H (internal OSC) |
| **INTVD1** | H |
| **C1** | 1uF/16V |
| **C2** | 1uF/25V |
| **C3** | 1uF/16V |
| **C4** | 1uF/16V |



| ST7687S Serial Specification Revision History | | |
|---|---|---|
| **Version** | **Date** | **Description** |
| 0.0 | | Preliminary version |
| 0.1 | 2007/12 | 1. Add pad arrangement.<br>2. Add pad center coordinates.<br>3. Add application note-80-8bit parallel interface and 4 line serial interface. |
| 0.2 | 2008/01 | 1. Modify location of common pad.<br>2. Modify bump size of pad 58 and bump pitch between pad 57 and 59.<br>3. Add application not- 80-16bit, 68-8bit, 68-16bit, 3line interface.<br>4. Fix some type error. |
| 0.3 | 2008/03 | 1. Fix type error.<br>2. Modify pin description.<br>3. Add application note for INTVD1= level high. |
| 0.4 | 2008/07 | 1. Add timing characteristic value.(p.152~156)<br>2. Add current consumption value.(p.151)<br>3. Remove external clock function.(p.15,37)<br>3. Remove 16bit mode.(p.16,20~22)<br>4. Remove 1/5 bias.(p.14)<br>5. Modify command 0xE0 and 0xFA.(p.51~52,129,147) |