

TECHNICAL BRIEF

IEEE 1284 compliant printer/scanner
interfacing

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Todd Andersen, Alan Light
Logic Products Group

The well known parallel interfacing for printers has been upgraded with the new standard IEEE 1284 which describes several protocols: ECP, EEP, bi-directional and Centronics compatible. Two electrical interfaces, Level One and Level Two, are also described in the 1284 specification. Level One electrical interfacing is the historical implementation of the uni-directional parallel port. However, Level Two electrical interfacing is recommended for the newer high speed bi-directional protocols. Hardware implementation of the Level Two electrical interface allows all these protocols to operate at peak performance level, yet is backward compatible with the older Level One interface. Level One interfaces using symmetrical voltages whereas Level Two interfaces using symmetrical impedances and balanced currents.

The newer protocol standards broaden the traditional applications of the parallel interface beyond standard printers to scanners,

CD-ROM players, hard disks and feature rich bi-directional printers. The more sophisticated protocols are also much faster--over two megabytes/second.

A typical interface between a driver and receiver is shown in Figure 1. $Z_o = 50$ ohms and $R_o = R_s \approx 90\% Z_o$, but $R_{in} \gg Z_o$. (R_o is the driver impedance as seen by the cable. Z_o is the input impedance of the cable. R_d is the B/Y side output resistance, R_s is an added series resistance and R_{in} is the input impedance of the receiver.) These impedance relationships cause half the source voltage to be injected into the cable which generates essentially double the voltage feeding the receiver due to reflection from the selected mismatch. This causes the input voltage at the receiver to be close to the value of the source voltage. A corresponding transceiver interface is shown in Figure 2.

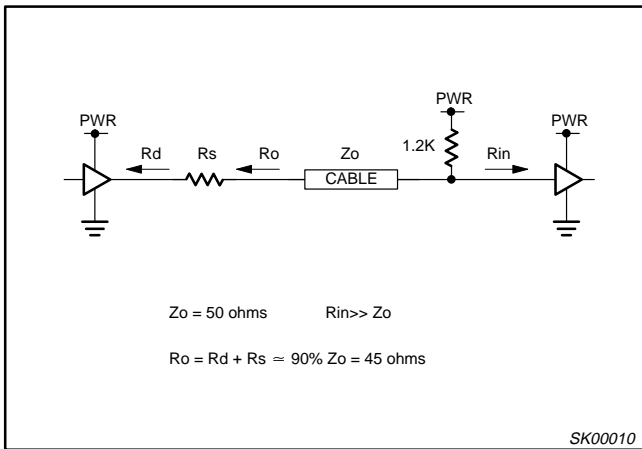


Figure 1. Driver/Receiver

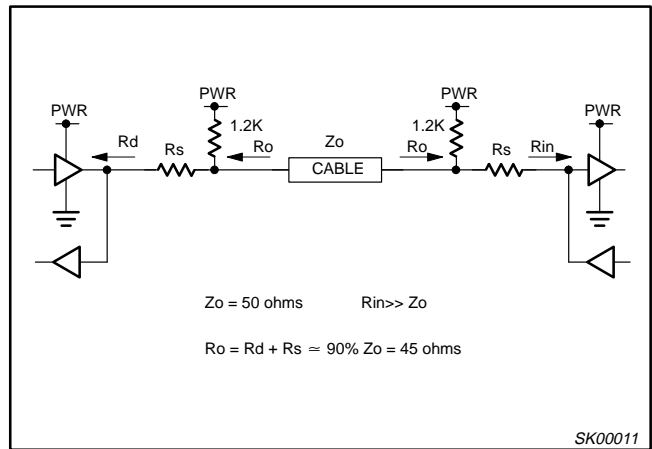


Figure 2. Transceiver

The Philips 74HCT1284 and 74LVC1284 Parallel interface transceiver/buffers are ideal components to implement a Level Two electrical interface. The HCT1284 uses a V_{cc} of 5 volts with a typical R_d of 15 ohms, requiring an external R_s of about 30 ohms; the second uses a V_{cc} of 3.3 volts with a typical R_d of 45 ohms, which is adequate without an external R_s . An R_o of about 90% of Z_o is needed for proper system performance. Each interface integrated circuit (IC) as shown in Figure 3, incorporates four data transceivers with data direction and high drive enable pins as well as three control/status drivers. Each IC has TTL compatible inputs and operates asynchronously with low noise. Also overvoltage protection has been designed in the B side of the IC's. The LVC1284 was designed with 3.3V systems in mind. This component can be used to allow 3.3V hosts or peripherals to interface either 5.0V or 3.3V agents on the other side of the cable.

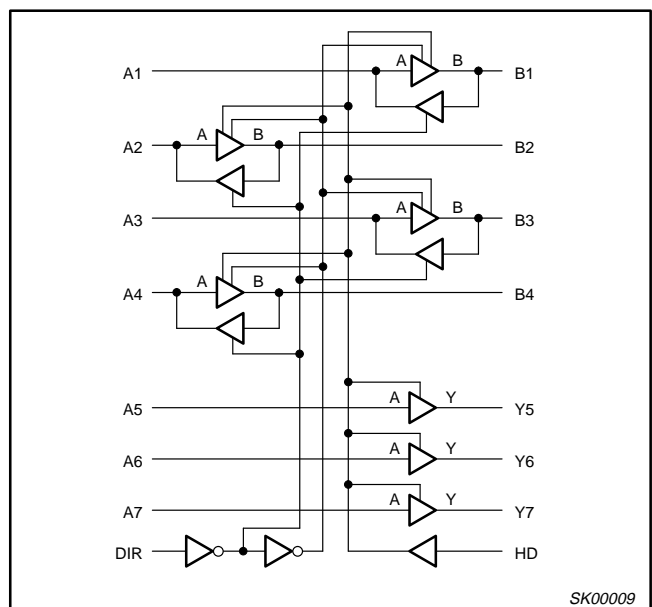


Figure 3. Logic Diagram of 74HCT1284 and LVC1284

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Figure 4. shows an IEEE 1284 Interface System utilizing 74HCT1284's. This diagram shows two IC's on the host side and two IC's on the peripheral side with bidirectional data transfer between the computer host and its peripheral. In this electrical implementation, the control signals required by the IEEE 1284 are generated by the host and sent to the peripheral and the status signals generated by the peripheral are sent back to the host. However, the control signals and status signals could have opposite source and destination depending on the protocol implemented. Also receivers for control and status are needed.

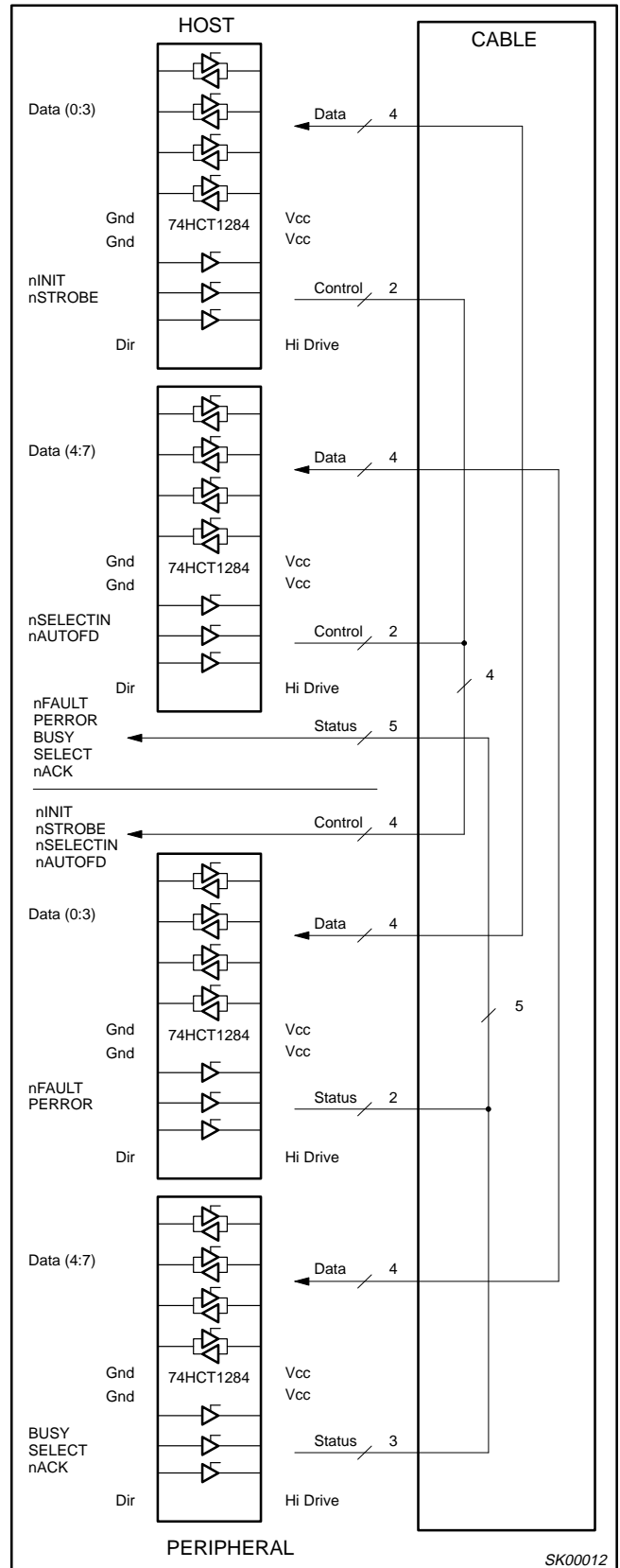


Figure 4. IEEE 1284 Interface System

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811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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