

# TPIC6595 POWER LOGIC 8-BIT SHIFT REGISTER

SLIS010A – APRIL 1992 – REVISED OCTOBER 1995

- Low  $r_{DS(on)}$  . . . 1.3  $\Omega$  Typical
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage at 45 V
- Devices Are Cascadable
- Low Power Consumption

## description

The TPIC6595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

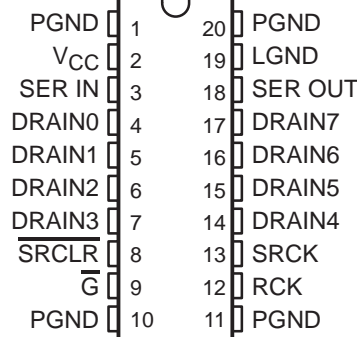
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear ( $\overline{SRCLR}$ ) is high. When  $\overline{SRCLR}$  is low, the input shift register is cleared. When output enable ( $\overline{G}$ ) is held high, all data in the output buffers is held low and all drain outputs are off. When  $\overline{G}$  is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

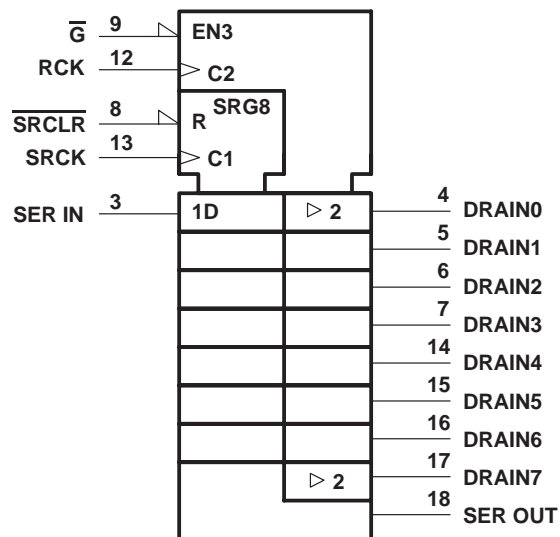
Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND), and pins 1, 10, 11, and 20, power grounds (PGND), must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6595 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

DW OR N PACKAGE  
(TOP VIEW)



## logic symbol†

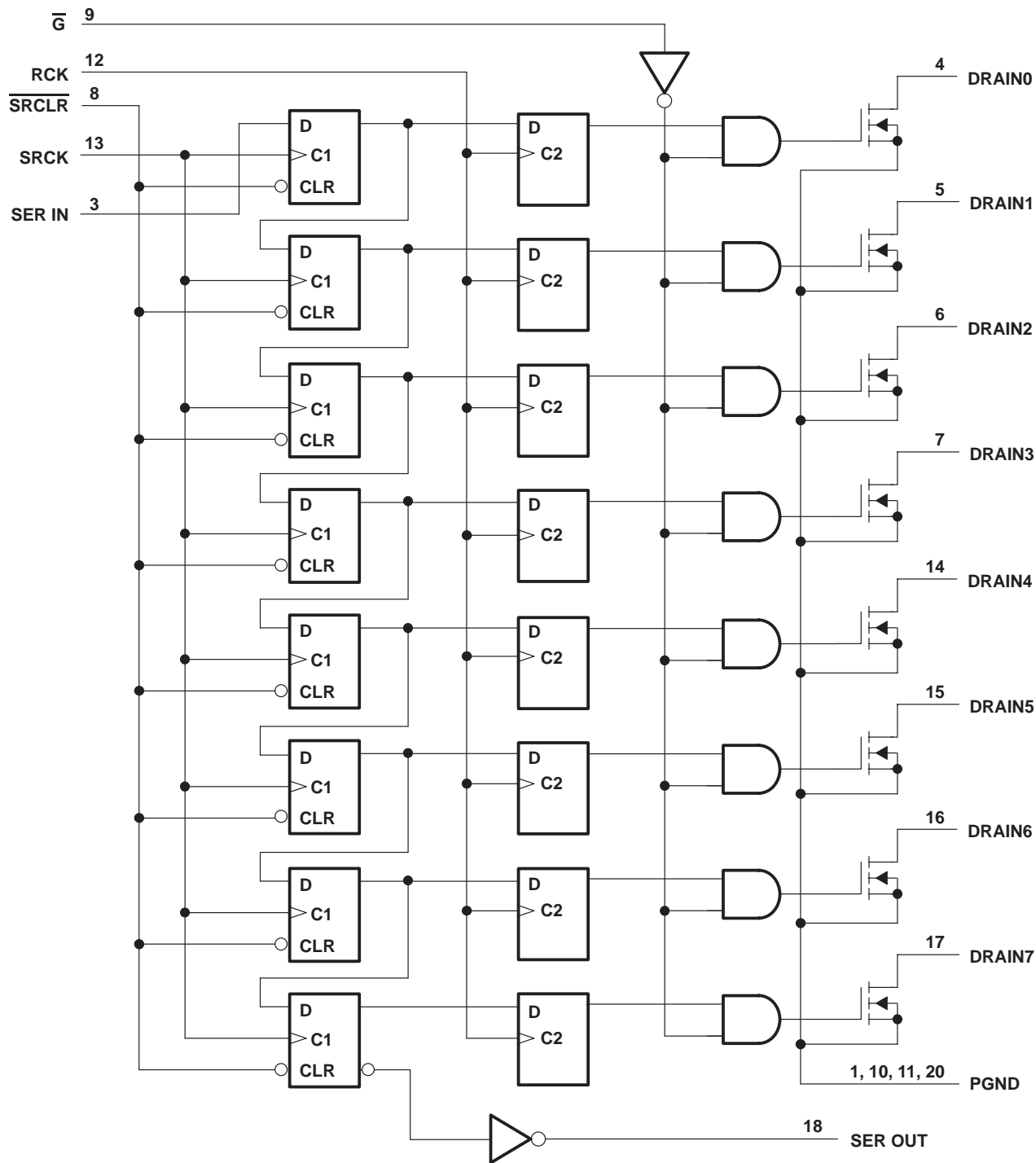


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

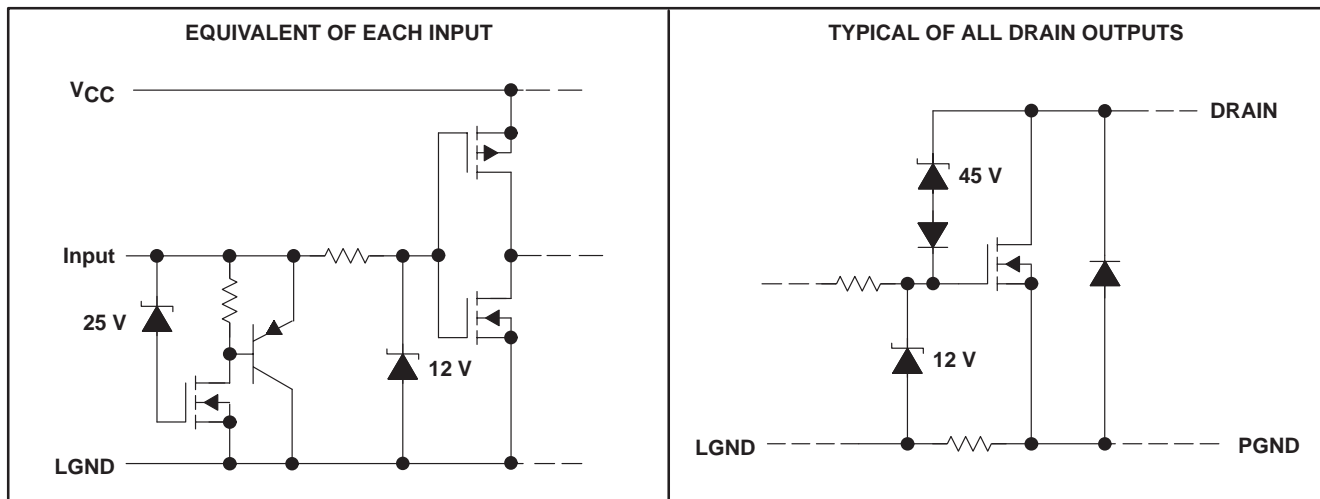
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## logic diagram (positive logic)



**schematic of inputs and outputs**



**absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†**

Logic supply voltage, $V_{CC}$ (see Note NO TAG)	7 V
Logic input voltage range, $V_I$	-0.3 V to 7 V
Power DMOS drain-to-source voltage, $V_{DS}$ (see Note NO TAG)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$ (see Note NO TAG)	750 mA
Continuous drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$	250 mA
Peak drain current single output, $I_{DM}$ , $T_A = 25^\circ\text{C}$ (see Note NO TAG)	2 A
Single-pulse avalanche energy, $E_{AS}$ (see NO TAG)	75 mJ
Avalanche current, $I_{AS}$ (see Note NO TAG)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	-40°C to 150°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to LGND and PGND.
  2. Each power DMOS source is internally connected to PGND.
  3. Pulse duration  $\leq 100 \mu\text{s}$ , duty cycle  $\leq 2\%$
  4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C, L = 100 mH,  $I_{AS} = 1 \text{ A}$  (see NO TAG).

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

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**recommended operating conditions over recommended operating temperature range (unless otherwise noted)**

	MIN	MAX	UNIT
Logic supply voltage, $V_{CC}$	4.5	5.5	V
High-level input voltage, $V_{IH}$	$0.85 V_{CC}$		V
Low-level input voltage, $V_{IL}$	$0.15 V_{CC}$		V
Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-1.8	1.5	A
Setup time, SER IN high before SRCK $\uparrow$ , $t_{su}$ (see NO TAG)	10		ns
Hold time, SER IN high after SRCK $\uparrow$ , $t_h$ (see NO TAG)	10		ns
Pulse duration, $t_w$ (see NO TAG)	20		ns
Operating case temperature, $T_C$	-40	125	$^\circ\text{C}$

**electrical characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-source breakdown voltage	$I_D = 1\text{ mA}$	45			V
$V_{SD}$ Source-drain diode forward voltage	$I_F = 250\text{ mA}$ , See Note 3		0.85	1	V
$V_{OH}$ High-level output voltage, SER OUT	$I_{OH} = -20\text{ mA}$ , $V_{CC} = 4.5\text{ V}$	4.4	4.49		V
	$I_{OH} = -4\text{ mA}$ , $V_{CC} = 4.5\text{ V}$	4.1	4.3		
$V_{OL}$ Low-level output voltage, SER OUT	$I_{OH} = 20\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		0.002	0.1	V
	$I_{OH} = 4\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		0.2	0.4	
$V_{(hys)}$ Input hysteresis	$V_{DS} = 15\text{ V}$		1.3		V
$I_{IH}$ High-level input current	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$			1	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = 5.5\text{ V}$ , $V_I = 0$			-1	$\mu\text{A}$
$I_{CCL}$ Logic supply current	$I_O = 0$ , All inputs low		15	100	$\mu\text{A}$
$I_{CC}(\text{FRQ})$ Logic supply current frequency	$f_{SRCK} = 5\text{ MHz}$ , $I_O = 0$ , $C_L = 30\text{ pF}$ , See Figures 1, 2, and 6		0.6	5	mA
$I_N$ Nominal current	$V_{DS(\text{on})} = 0.5\text{ V}$ , $I_N = I_D$ , $T_C = 85^\circ\text{C}$	See Notes 5, 6, and 7		250	mA
$I_{DSX}$ Off-state drain current	$V_{DS} = 40\text{ V}$		0.05	1	$\mu\text{A}$
	$V_{DS} = 40\text{ V}$ , $T_C = 125^\circ\text{C}$		0.15	5	
$r_{DS(\text{on})}$ Static drain-source on-state resistance	$I_D = 250\text{ mA}$ , $V_{CC} = 4.5\text{ V}$	See Notes 5 and 6 and Figures 9 and 10		1.3	$\Omega$
	$I_D = 250\text{ mA}$ , $T_C = 125^\circ\text{C}$ , $V_{CC} = 4.5\text{ V}$	NO TAG		2	
	$I_D = 500\text{ mA}$ , $V_{CC} = 4.5\text{ V}$			1.3	

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$ Propagation delay time, low-to-high-level output from $\overline{G}$	$C_L = 30\text{ pF}$ , $I_D = 250\text{ mA}$ , See Figures 1 and 2		650		ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output from $\overline{G}$			150		ns	
$t_r$ Rise time, drain output				750		ns
$t_f$ Fall time, drain output				425		ns
$t_a$ Reverse-recovery-current rise time	$I_F = 250\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 3		100		ns	
$t_{rr}$ Reverse-recovery time			300			

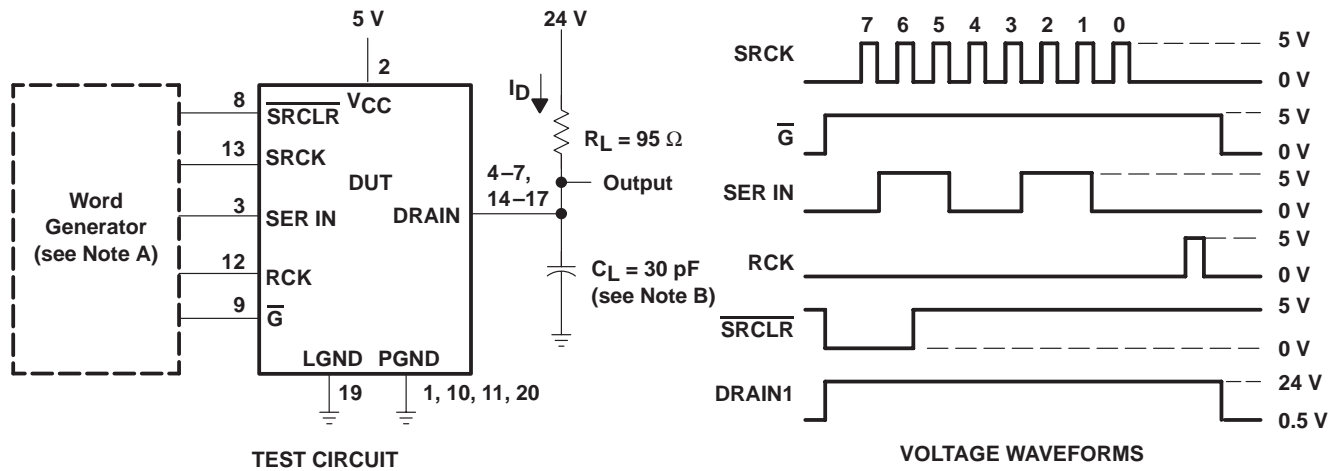
- NOTES:
- Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 2\%$
  - Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.
  - These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
  - Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of  $0.5\text{ V}$  at  $T_C = 85^\circ\text{C}$ .



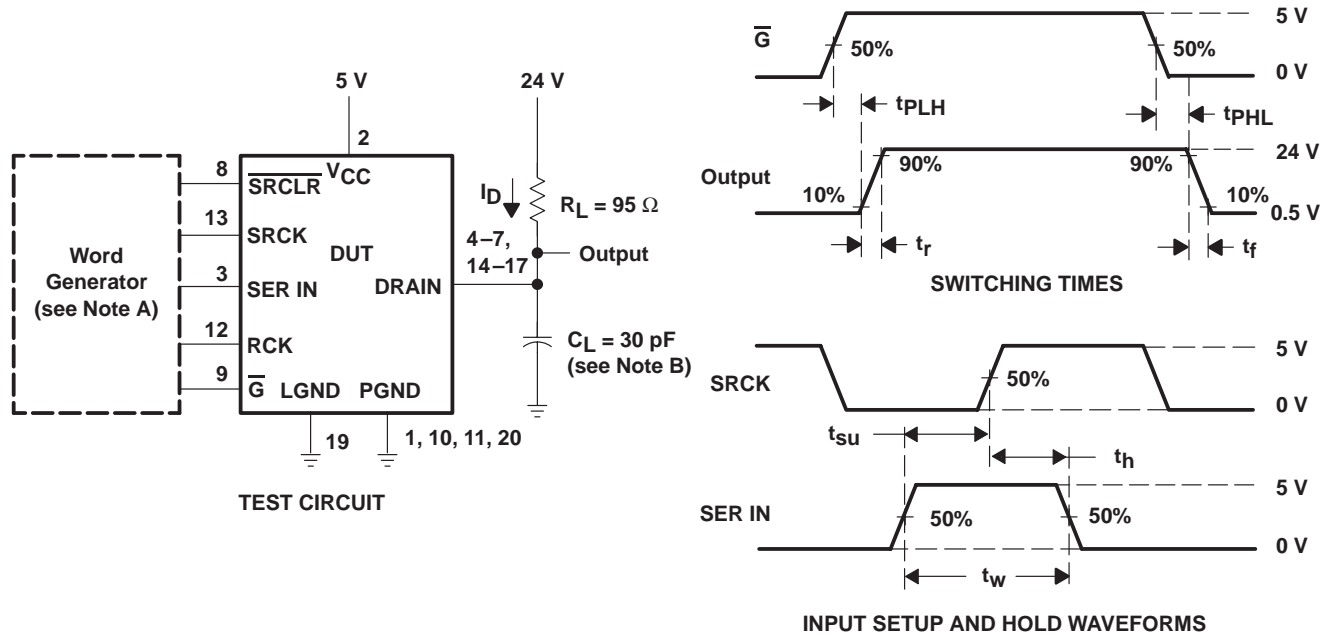
**thermal resistance**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package		111	°C/W
		N package	All 8 outputs with equal power	108	

**PARAMETER MEASUREMENT INFORMATION**



**Figure 1. Resistive Load Operation**



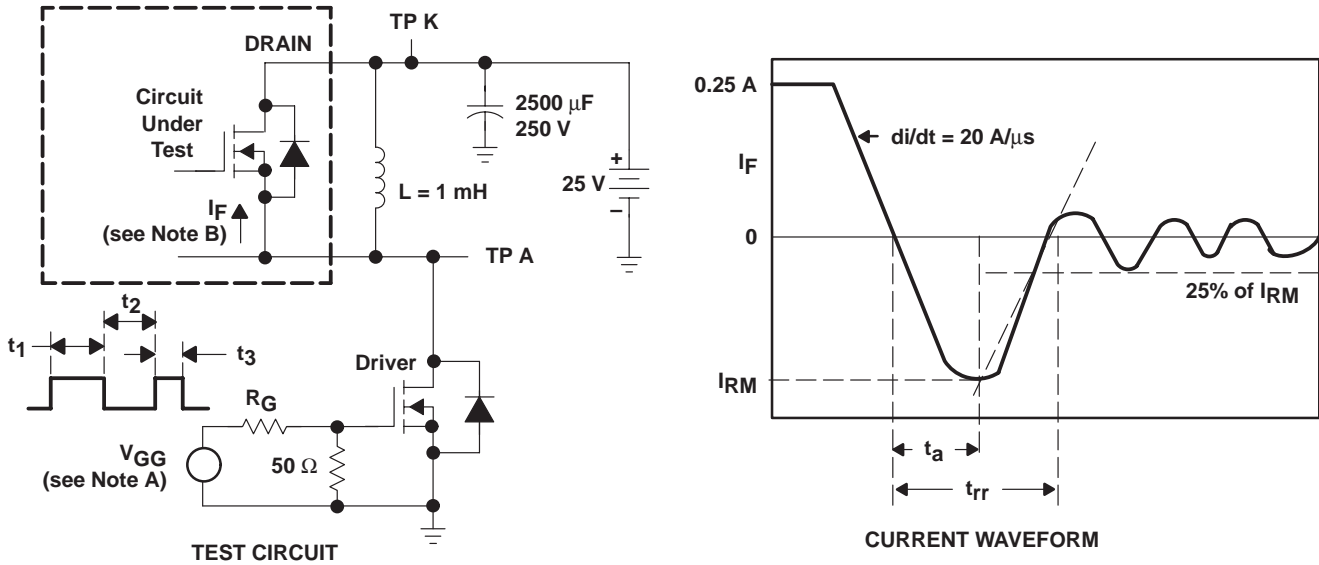
**Figure 2. Test Circuit, Switching Times, and Voltage Waveforms**

- NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $t_w = 300$  ns, pulsed repetition rate (PRR) = 5 kHz,  $Z_0 = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

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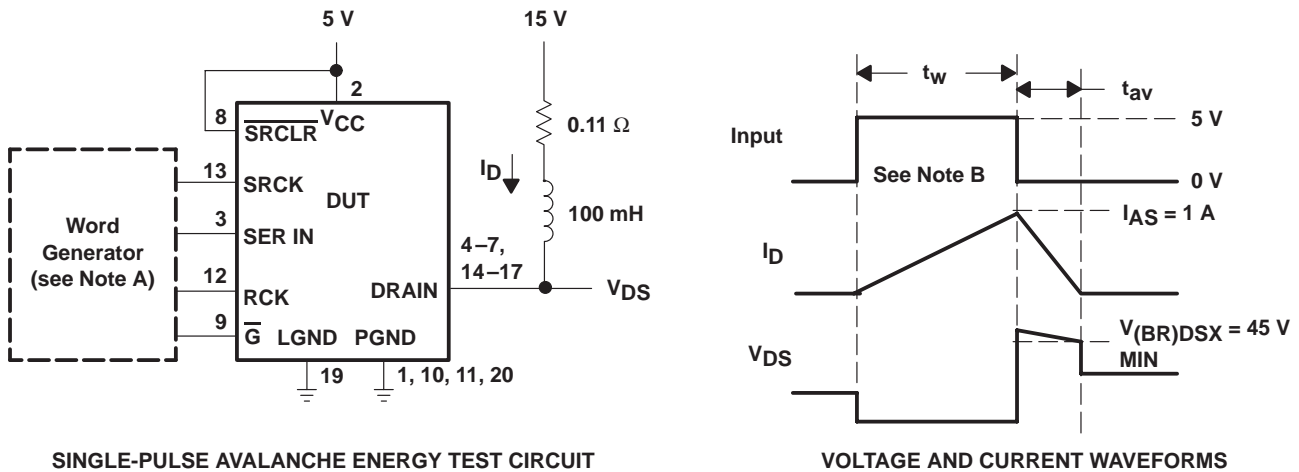
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.25 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .  
 B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
 B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 1 \text{ A}$ .  
 Energy test level is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75 \text{ mJ}$ , where  $t_{av}$  = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

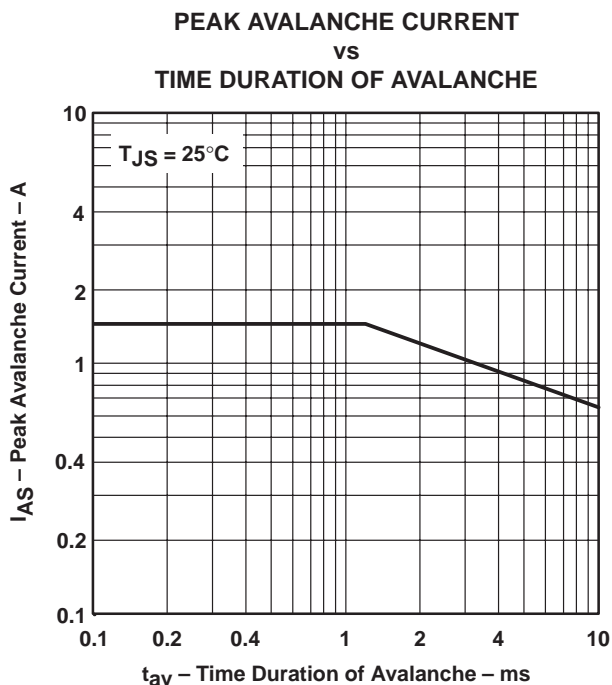


Figure 5

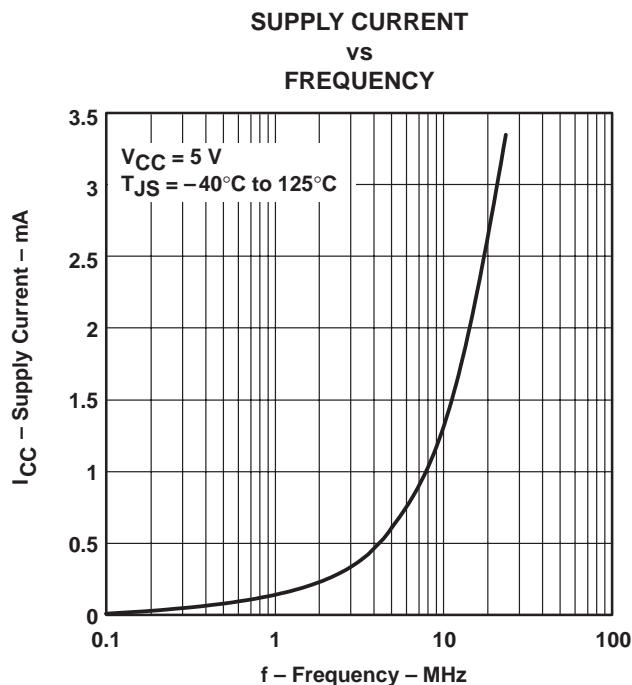


Figure 6

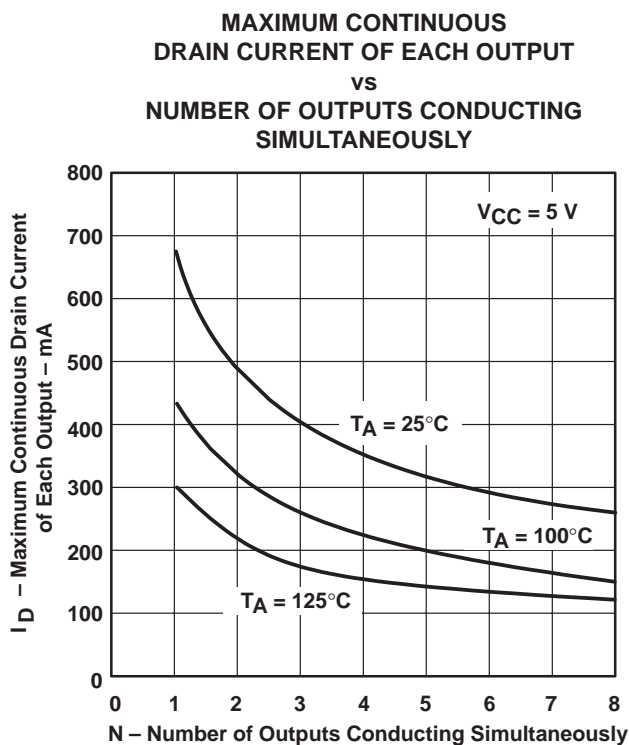


Figure 7

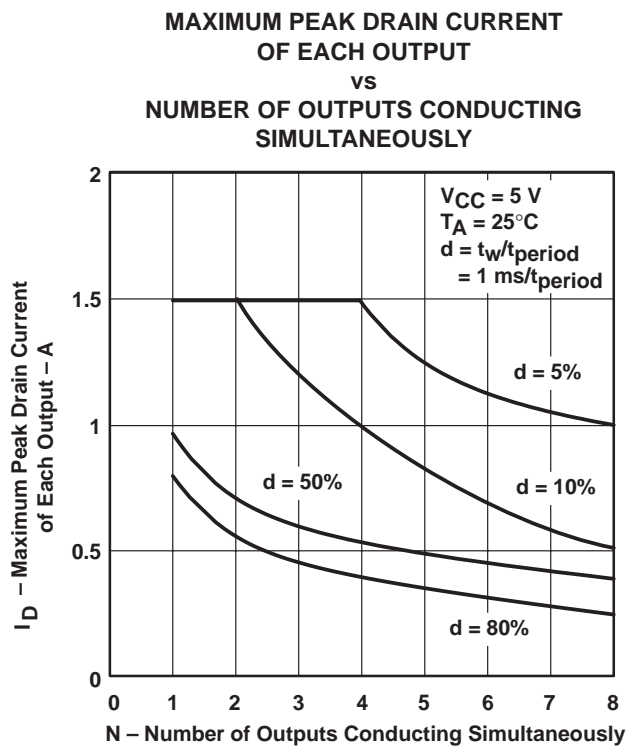


Figure 8

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## TYPICAL CHARACTERISTICS

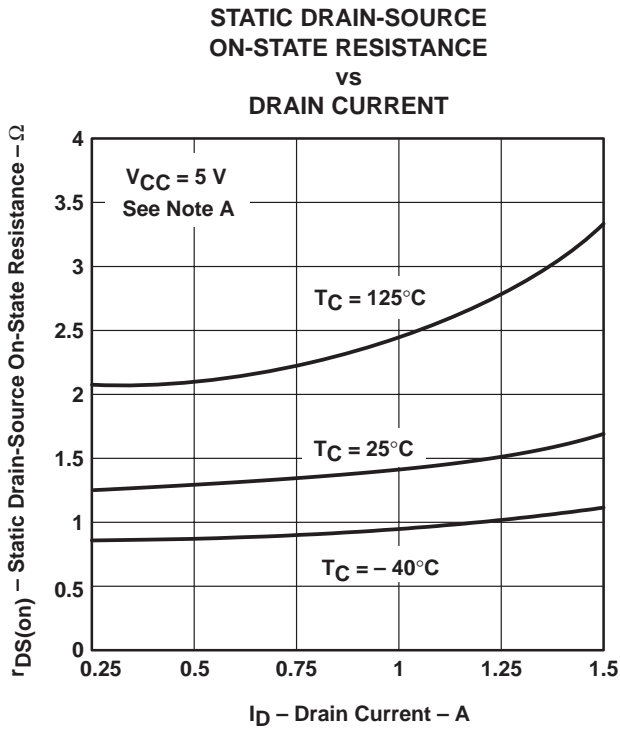


Figure 9

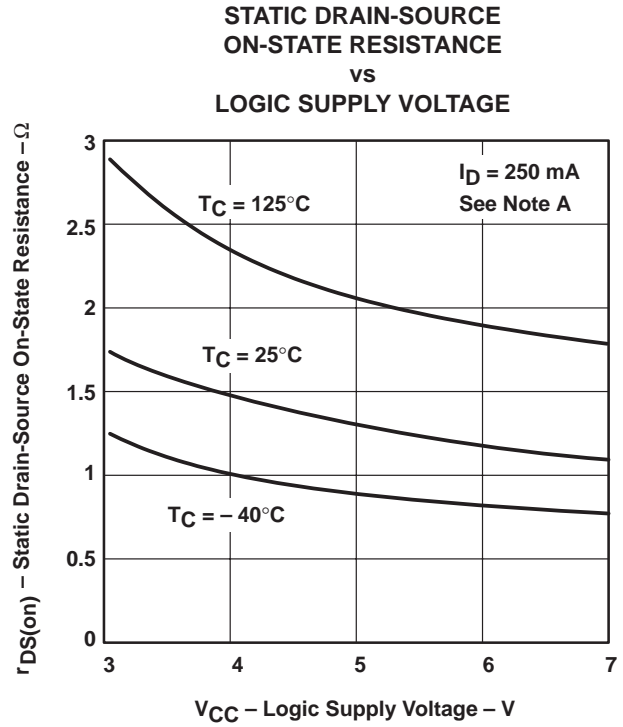


Figure 10

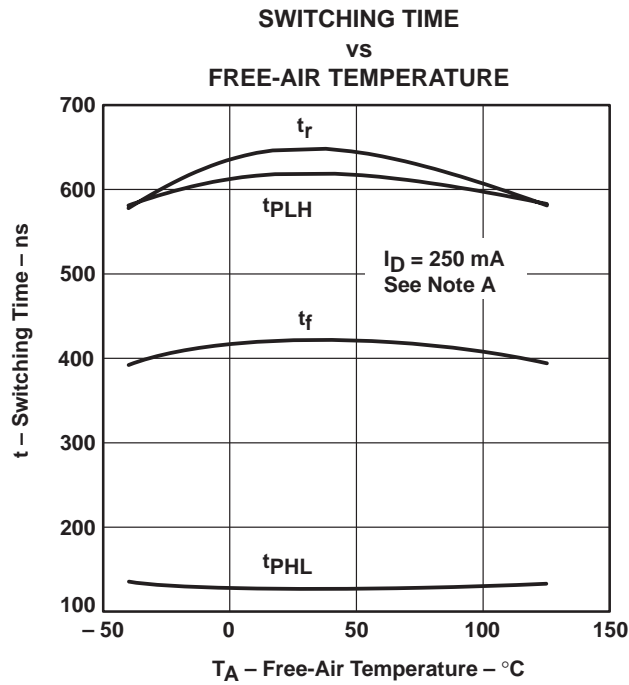


Figure 11

NOTE A: Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.



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