CY7C1061DV33

16-Mbit (1M x 16) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 175 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 25 mA
- Operating voltages of 3.3 ± 0.3V
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$ and CE_2 features
- Available in Pb-free 54-Pin TSOP II and 48-Ball VFBGA packages

Functional Description

The CY7C1061DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

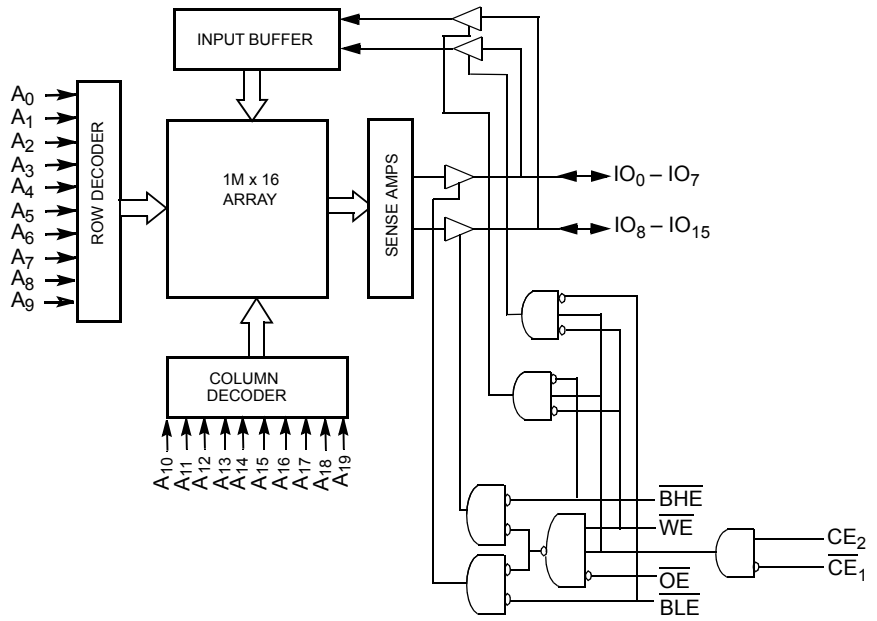
To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the Truth Table on page 9 for a complete description of Read and Write modes.

The input or output pins (IO_0 through IO_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1061DV33 is available in a 54-Pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-Ball VFBGA package.

Logic Block Diagram



Selection Guide

	–10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

Pin Configuration

Figure 1. 54-Pin TSOP II (Top View) [1]

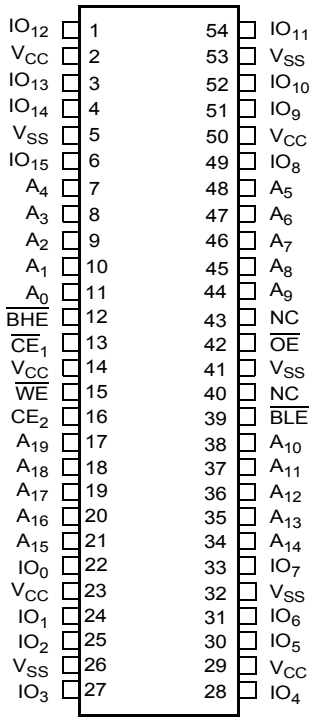
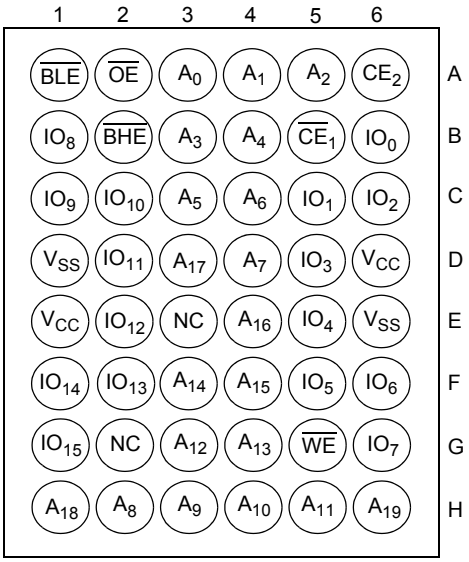


Figure 2. 48-Ball VFBGA (Top View) [1]



Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND [2] ....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State [2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage [2] ..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... .....>2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	3.3V ± 0.3V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	–10		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage [2]		–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = 1/t_{RC}, I_{OUT} = 0 mA CMOS levels		175	mA
I_{SB1}	Automatic CE Power Down Current — TTL Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		30	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		25	mA

Note

2. V_{IL} (min) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	8	pF
C_{OUT}	IO Capacitance		8	10	pF

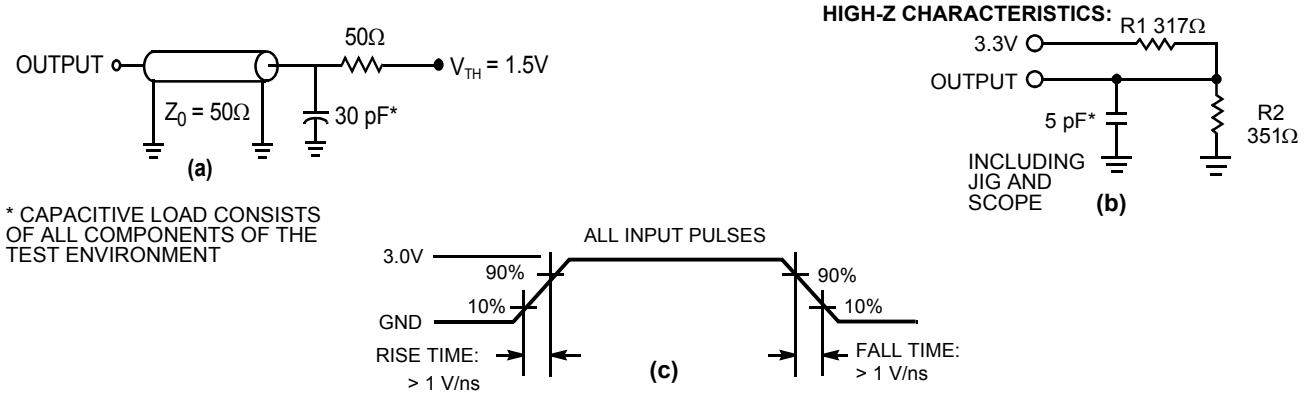
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	28.37	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		5.40	5.79	°C/W

AC Test Loads and Waveforms

The AC test loads and waveform diagram follows. [3]



Note

3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.

AC Switching Characteristics

Over the Operating Range [4]

Parameter	Description	–10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(Typical) to the First Access [5]	100		µs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Data Valid		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [6]		5	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Low Z [6]	3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to High Z [6]		5	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to Power Up [7]	0		ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to Power Down [7]		10	ns
t_{DBE}	Byte Enable to Data Valid		5	ns
t_{LZBE}	Byte Enable to Low Z	1		ns
t_{HZBE}	Byte Disable to High Z		5	ns
Write Cycle [8, 9]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Write End	7		ns
t_{AW}	Address Setup to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		ns
t_{SD}	Data Setup to Write End	5.5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [6]		5	ns
t_{BW}	Byte Enable to End of Write	7		ns

Notes

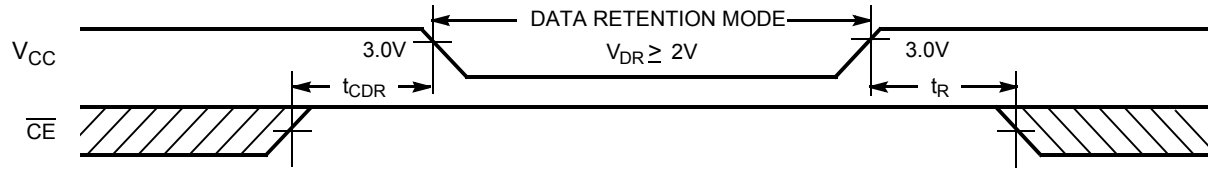
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading shown in part a) of AC Test Loads and Waveforms, unless specified otherwise.
5. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} , t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms. Transition is measured ±200 mV from steady state voltage.
7. These parameters are guaranteed by design and are not tested.
8. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics

Over the Operating Range

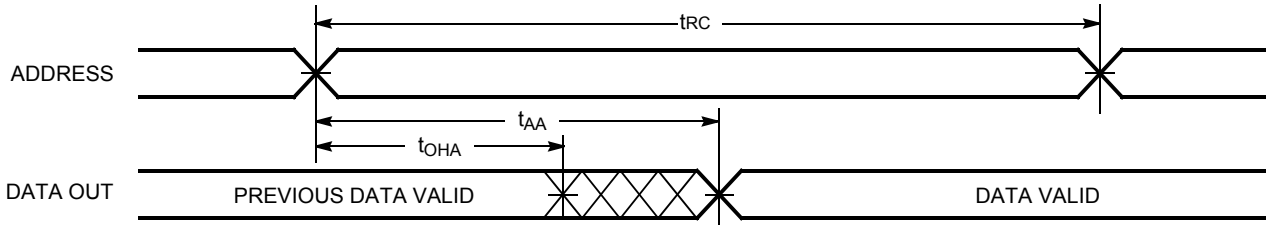
Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention		2			V
I_{CCDR}	Data Retention Current	$V_{CC} = 2V$, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			25	mA
t_{CDR} [10]	Chip Deselect to Data Retention Time		0			ns
t_R [11]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Switching Waveforms

Figure 3. Read Cycle No. 1 [12, 13]



Notes
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.
12. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [13, 14]

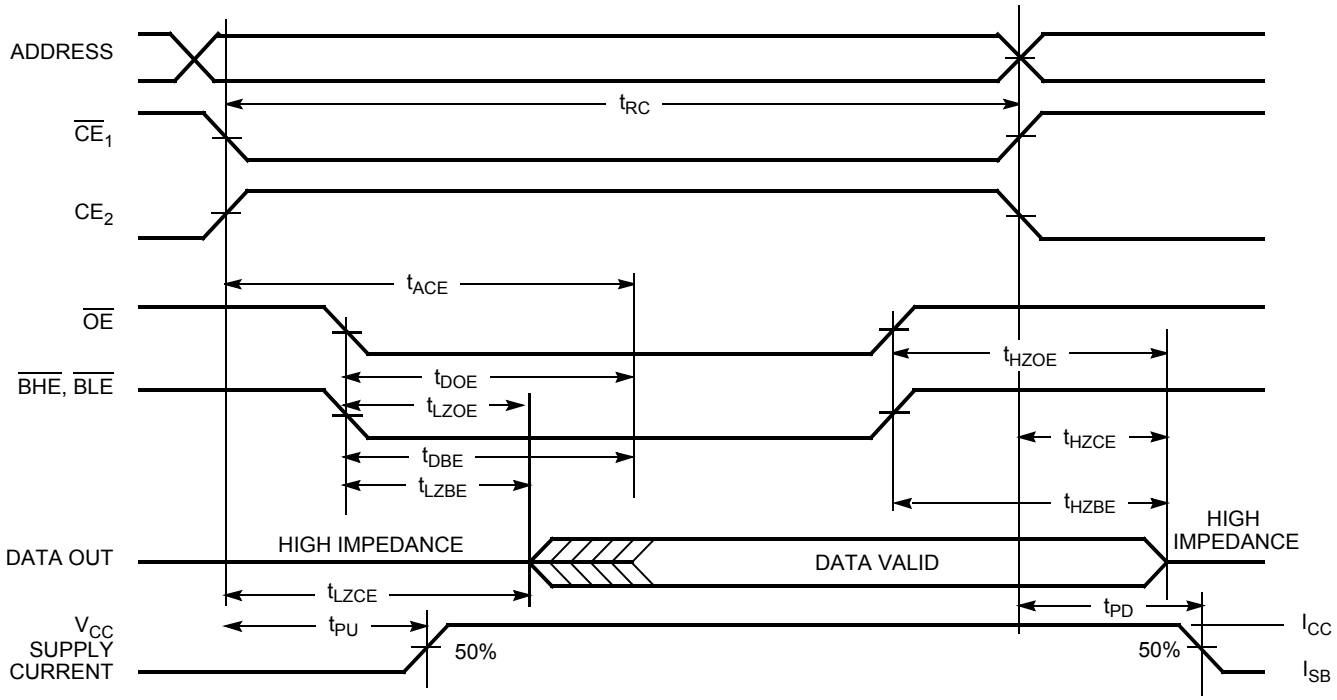
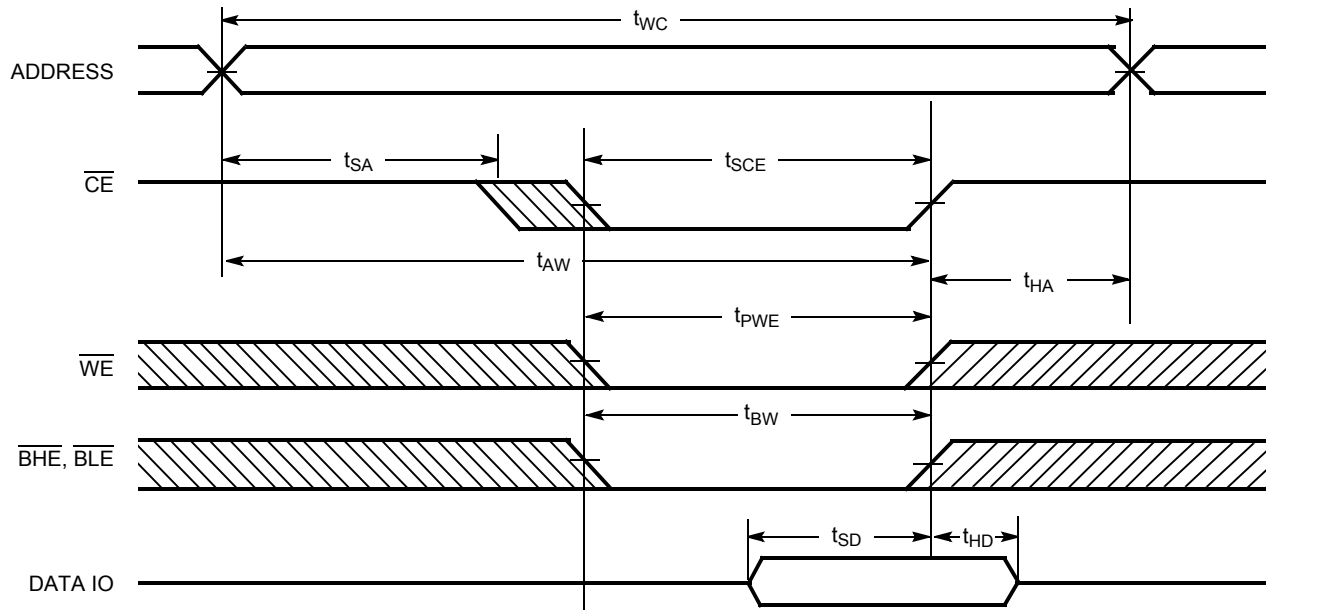


Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [15, 16, 17]



Notes
14. Address valid before or similar to $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
15. $\overline{CE}$ is a shorthand combination of both $\overline{CE_1}$ and CE_2 combined. It is active LOW.
16. Data IO is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [15, 16, 17]

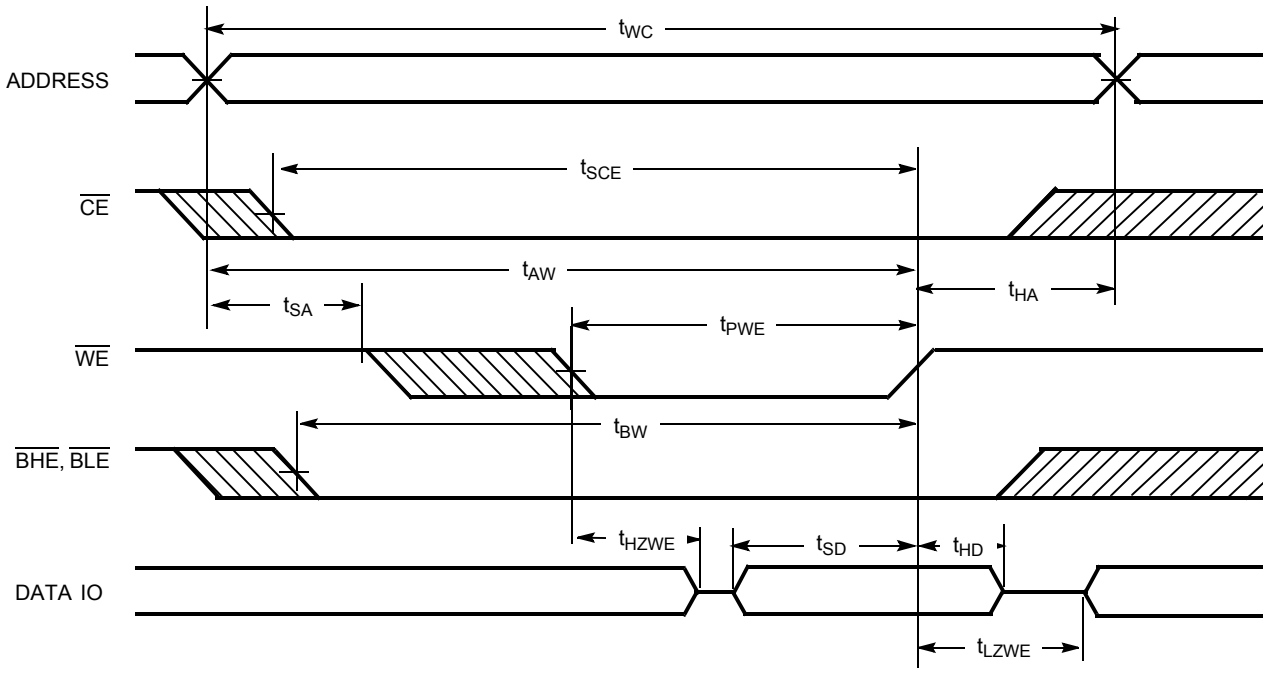
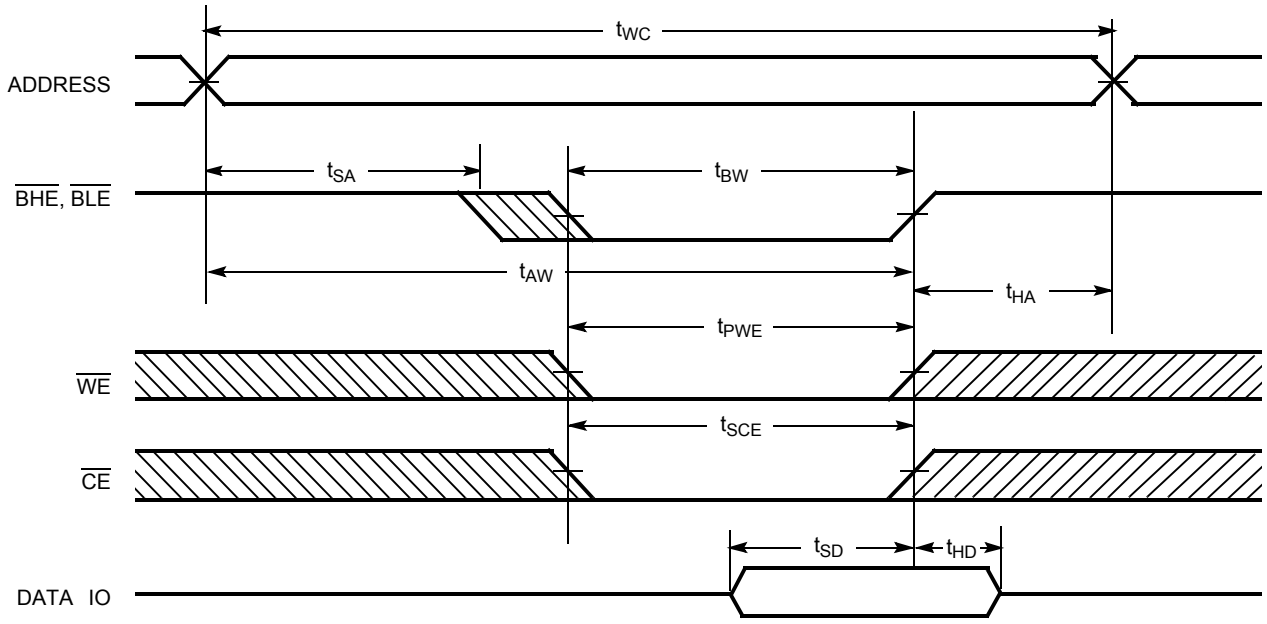


Figure 7. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [15]



Truth Table

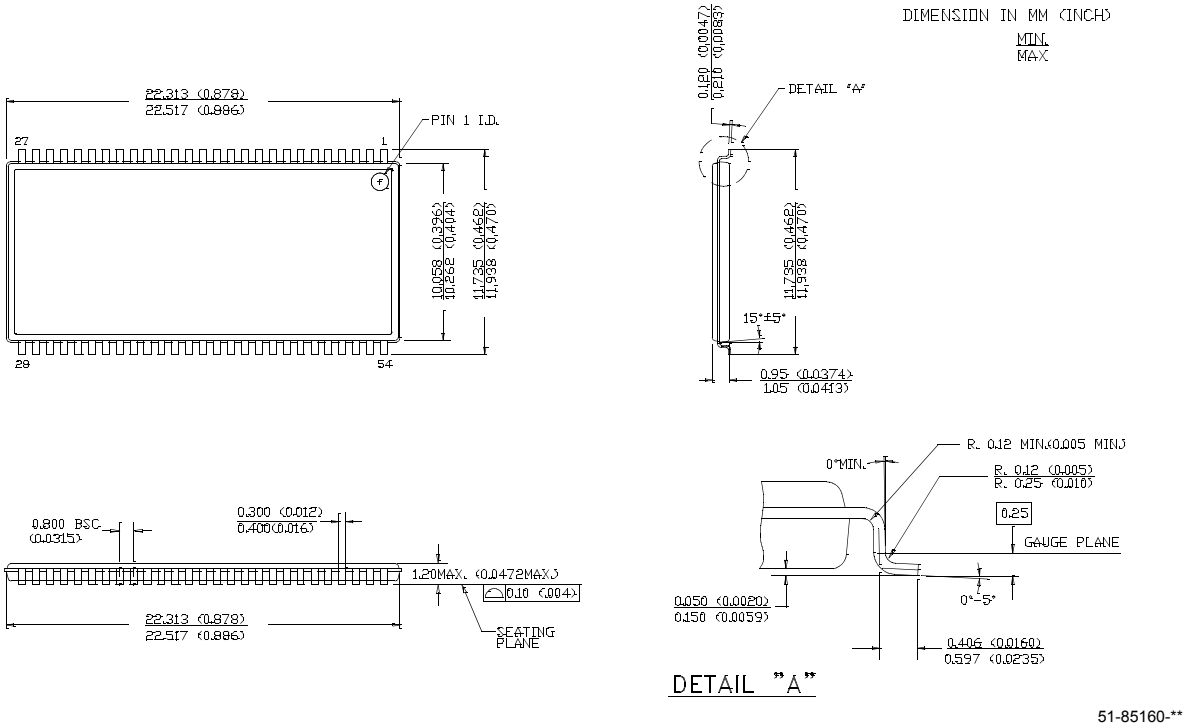
$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$IO_0 – IO_7$	$IO_8 – IO_{15}$	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	H	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I_{CC})
L	H	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	H	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	H	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I_{CC})
L	H	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061DV33-10ZSXI	51-85160	54-Pin TSOP II (Pb-Free)	Industrial
	CY7C1061DV33-10BVXI	51-85178	48-Ball VFBGA (8 × 9.5 × 1 mm) (Pb-Free)	

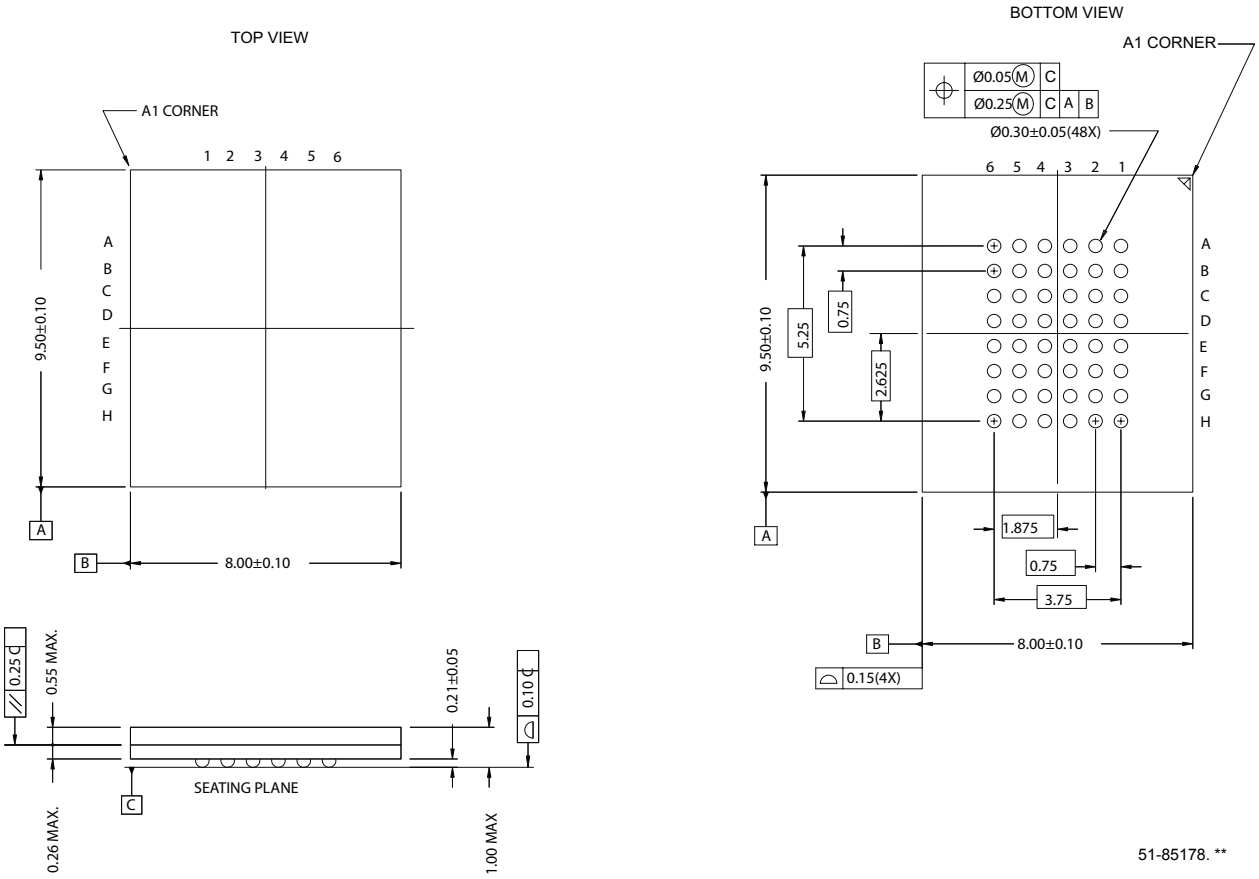
Package Diagrams

Figure 8. 54-Pin TSOP Type II



Package Diagrams (continued)

Figure 9. 48-Ball VFBGA (8 x 9.5 x 1 mm)



Document History Page

Document Title: CY7C1061DV33 16-Mbit (1M x 16) Static RAM Document Number: 38-05476				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance datasheet for C9 IPP
*A	233748	See ECN	RKF	AC, DC parameters are modified as per EROS (Specification number 01-2165) Added Pb-free devices in the Ordering Information
*B	469420	See ECN	NXR	Converted from Advance Information to Preliminary Corrected typo in the Document Title Removed –8 and –12 speed bins from product offering Removed Commercial Operating Range Changed 2G-Ball of FBGA and pin 40 of TSOPII from DNU to NC Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed $I_{CC(Max)}$ from 220 mA to 125 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot specification in footnote 1. Updated the Ordering Information Table
*C	499604	See ECN	NXR	Added note 1 for NC pins Updated Test Condition for I_{CC} in DC Electrical Characteristics table Updated the 48-Ball FBGA Package
*D	1462583	See ECN	VKN/AESA	Converted from preliminary to final Changed I_{CC} specification from 125 mA to 175 mA Updated thermal specs