UE6015

Time-Code Receiver IC

1 Short Description

The UE6015 is a BICMOS integrated straight through receiver circuit, which is suitable for the frequency range from 40kHz up to 120 kHz (ASK modulation). The receiver is equiped with a very high sensitivity and is prepared for single- and multi-band reception. Therefore this IC is designed for all kinds of standard and high valued radio controlled clock applications.
Once used with reference to its application circuit and connected with a corresponding antenna the UE6015 receives and demodulates time code signals transmitted by e.g. DCF77 (Germany), MSF (UK), WWVB (USA), JJY (JPN), HBG (CH) and BPC (China).
The IC includes an integrated antenna-switching circuit, controlled by 2 antenna-switch input-lines. This antenna switch allows to connect other capacitors in parallel to the initial antenna-capacitor. By this way the connected antenna can be tuned to at least 2 other frequencies too. By connection of max. 3 different crystal-filters it is possible to receive transmitting stations working on 3 different carrier frequencies. The UE6015 is the key for single-, dual-, or multi-band receivers.
Integrated functions as stand-by mode, hold mode and a selectable output polarity offer features for universal applications.

2 Features

- Single Chip AM Straight Through Receiver
- Low power consumption
- Very high sensitivity (typ. 0.3µV_{RMS})
- High selectivity by using crystal filters
- Power down mode available
- Only a few external components needed
- Implemented antenna-switches
- Single-, Dual- and Tri-Band receiver IC
- CMOS output stage with selectable polarity
- Output-signal for FSI-indication
- AGC hold mode
- Fast start-up
- Wide frequency range (40 ... 120 kHz)
- Low power battery applications (1.1 .. 3.6 V)

3 Operation Modes

3.1 Power Down Mode

Switching the IC into Power Down Mode the IC becomes current-less. During this operation mode:
– all internal functional blocks are powered OFF
– signal output DAT is set to LOW
– status of antenna-switches is undefined

3.2 ASK Reception mode

This standard reception mode is entered after PowerON Reset and is characterized by:
– AGC-hold function is available (pin HLD; LOW active)
– Data Output Polarity can be changed (pin DATP; LOW active); default polarity (DATP open) = LHL
– Integrated compensation capacitance can be switched OFF (pin CF; LOW active)
– Additional external capacitors can be added in parallel to the antenna capacitor in order to tune the antenna circuitry to a lower frequency (pins CA1, CA2; LOW active)

4 Block Diagram

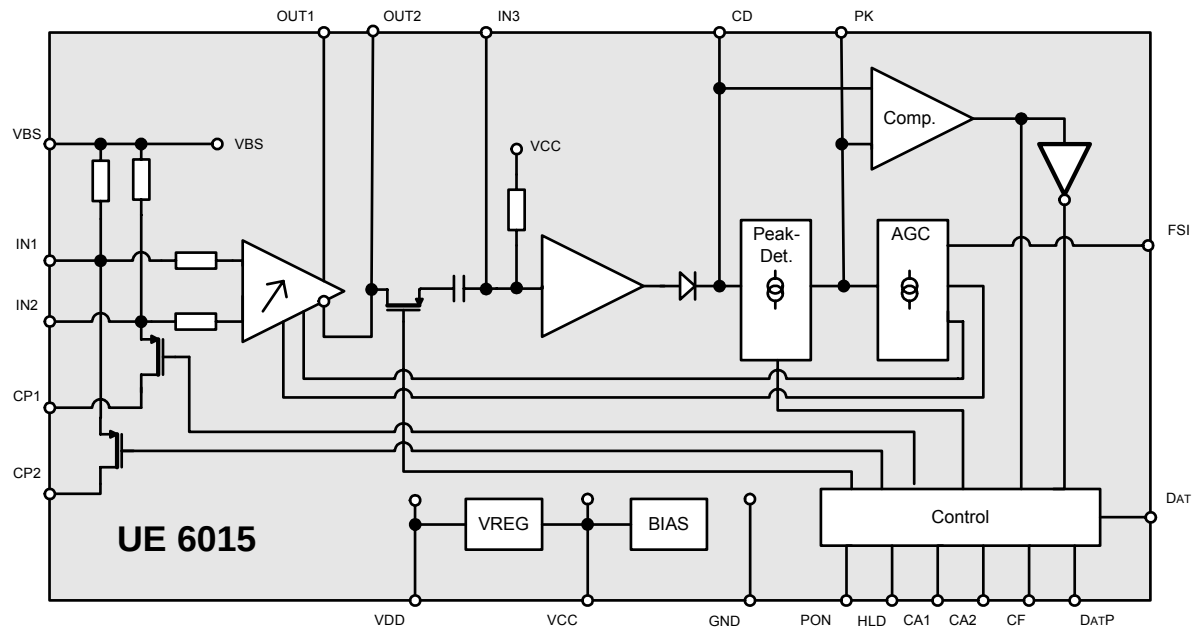


Figure 1: Block diagram

5 Absolute Maximum Ratings

(for T_A = -25 to 85°C)

Pos.	Parameters	Symbol	min.	max.	Unit
1	Supply voltage	V_{CC}	0	3	V
2	Supply voltage V_{DD}	V_{DD}	0	4	V
3	Voltage at any pin (except V_{DD}, DAT, HLD, PON and digital inputs DATP, CF, CA1, CA2)	V_{PIN}	-0.3	V_{CC}+0.3	V
4	Voltage at V_{DD} , DAT, HLD, PON and at digital inputs DATP, CF, CA1, CA2	$V_{PIN\ dig.}$	-0.3	V_{DD}+0.3	V

6 Operation Ratings

Pos.	Parameters	conditions	Symbol	min.	max.	Unit
1	Supply voltage V_{CC}	T_A = 0 … +85°C	V_{CC}	1.1	1.8	V
2	Supply voltage V_{DD}		V_{DD}	2	3.6	V
3	Ambient temperature		T_A	-25	85	°C
4	Frequency range		f_{IN}	40	120	kHz

7 Electrical Characteristics

Unless otherwise specified: V_{DD}=V_{CC}=1.5V; V_{PON} = 0V; f_{IN} = 77.5kHz, v_{IN} = 300µV_{RMS};
AM carrier voltage reduction from 100% to 25% for t_{MOD} = 200ms

7.1 DC-Characteristics

Pos.	Parameters	conditions	Symb.	min.	typ.	max.	Unit
1	Quiescent current	V_{PON}=V_{DD}=3.0V	I_{DD0}			1	µA
2	Quiescent current	V_{PON}=V_{DD}=V_{CC}=1.5V	I_{DC0}			1	µA
3	Supply current with VREG	V_{DD}=3.0V	I_{DD}			130	µA
4	Supply current w/o VREG	V_{DD}=V_{CC}=1.5V	I_{CC}		100	120	µA
5	DAT output voltage HIGH	I_{DAT} = 30uA	V_{DATH}	V_{DD}-0.3			V
6	DAT output voltage LOW	I_{DAT} = - 30uA	V_{DATL}			0.3	V
7	DIG input voltage HIGH	(all digital *)	V_{IH}	V_{DD}*0.7			V
8	DIG input voltage LOW	(all digital *)	V_{IL}			V_{DD}*0.3	V
9	DIG input current HIGH	V_{IX}=H (all digital *)	I_{IHx}			1	µA
10	DIG input current LOW	V_{IX}=L (all digital *)	I_{ILx}	-10			µA
11	PK settling time default	C_{PK} = 1µF	t_{PK}			3	s
12	AGC response time +	V_{PON} = 0V; Δ v_{IN} = +20dB	$t_{AGC+\Delta}$		0.3		s
13	AGC response time -	V_{PON} = 0V; Δ v_{IN} = -20dB	$t_{AGC-\Delta}$		7		s
14	FSI output current min.	v_{IN} = 0	$I_{FSI\ min}$		0.3	1	µA
15	FSI output current max.	v_{IN} = 30mV_{RMS}	$I_{FSI\ max}$		10		µA
16	FSI output voltage	v_{IN} = 30mV_{RMS} ; $I_{FSI\ max}$=10µA	$U_{FSI\ max}$			1	V
17	CPx PMOS-RDS_{ON}	CAx=L	R_{CPx}		6		Ω
18	IN1 / IN2 input impedance		Z_{Inx1}		500		kΩ

*) PON, HLD and digital inputs DATP, CF, CA1, CA2; H=V_{DD} , L=0V

7.2 AC-Characteristics

Pos.	Parameters	conditions	Symb.	Min	Typ	Max	Unit
1	Minimum input voltage	differential input	$v_{IN\ min}$		0.3	0.6	µV_{RMS}
2	Maximum input voltage	differential input	$v_{IN\ max}$	30			mV_{RMS}
3	Output pulse width	DCF, t_{MOD} =200ms	t_{WDAT}	160	185	220	ms
4	Static parallel input capacitance	between IN1 and IN2 w/o using antenna switches	CPS_{IN}		18		pF
5	Additional input capacitance CP1	using CP1	CPP1		6.5		pF
6	Additional input capacitance CP2	using CP2	CPP2		8		pF

8 Internal connection of PAD's

The IC is ESD protected conform to the Human-Body-Model (V_{ESD} = ±1000V on each pin refered to GND).

9 Functional description of PAD's

IN1 / IN2 Antenna inputs

Both antenna inputs, IN1 and IN2, are entitled to the same rights. Each of the antenna inputs is connected by an integrated resistor to the internal Bias-voltage. Generally it is possible to realize a symmetrical or an unsymmetrical operation of the connected ferrit-antenna. The coil of the ferrit-antenna has to be connected between IN1 and IN2.

- symmetrical operation mode:

Recommended operation mode for applications influenced by bigger disturbances and for multi-band receivers. The RF-signal is supplied symmetrically into both antenna inputs. Pin VBS is not used.

- unsymmetrical operation mode:

The RF-signal is supplied into only one of the antenna inputs. The second antenna input is connected to Pin VBS. A capacitor has to be connected between Pin VBS and GND.

CP1 / CP2 PMOS antenna switch inputs

Inputs of two PMOS-switches which are used to connect additional capacitors in parallel to the initial antenna capacitor in order to reduce the resonant frequency of the antenna circuit. The additonal capacitors should be connected between IN1 and CP1 respectively between IN2 and CP2. By this way the antenna can be tuned to other frequencies too.
The implemented antenna switches of UE6015 are characterized by parasitic capacitances as specified in chapter 7.2 .

OUT1 Crystal RF output 1

At the output OUT1 you find the amplified RF-signal. OUT1 is connected to the crystal 1 filter.

OUT2 Crystal RF output 2

At the output OUT2 you find the amplified RF-signal. OUT2 is connected to the crystal 2 filter.

IN 3 Crystal input 1

High resistance input of an amplifier stage. An external crystal has to be connected to IN3 to supply the filtered signal into this amplifier.

CF Filter switch input

CMOS compatible input; LOW active; by default set to HIGH via internal pull-up resistor. Using an odd no. of filter-crystals this pin has to be kept open. Once the receiver is used with 2 filter-crystals then this pin should be switched to LOW during any reception attempt.

CD Demodulator output

An external capacitor (typ. 47nF) has to be connected between pin CD and GND. It is used to demodulate the filtered and amplified RF-signal.

PK Peak Detector output

An external capacitor ($C_{PK} \geq 2.2\mu F$) has to be connected between pin PK and GND. This ensures the function of the peak detector. The value of C_{PK} influences the AGC regulation time.

FSI Field strength indicator

Output FSI supplies a current which is proportional (appr. logarithmic) to the received field-strength. The typical range of output-current is 0.1µA .. 10µA which corresponds with a range of input-voltage of 0.3µV … 30mV. The simpliest way to use this output-information is the use of a resistor (47kΩ .. 100kΩ) between FSI-output and GND. The output stage is a PMOS-current source and can be kept open if it isn't used.
The output-current of this FSI-pin isn't considered in the current consumption specified for the IC.

DATP Data-Output-Polarity selection input

CMOS compatible input; LOW active; by default set to HIGH via internal pull-up resistor.
This pin allows the control of the polarity of output signal obtained on pin DAT. By default (DATP not connected) this pin is HIGH and the resulting polarity of output signal is LHL. In order to change the polarity of output signal to HLH pin DATP has to be connected to LOW during any reception attempt.
If the receiver is switched OFF (PON=HIGH=V_{DD}) then set DATP=HIGH too.

HLD AGC hold input

CMOS compatible, digital input; LOW active; by default set to HIGH via internal pull-up resistor.
AGC hold mode: HLD = HIGH sets normal function, HLD = LOW (V_{HLD} = GND) holds for a short time the AGC voltage. This can be used to prevent the AGC from peak voltages, created by e.g. a stepper motor.
Once HLD is used then it is recommended to keep HLD activated (HLD=LOW) as long as the interference can be detected on the cristal filter. Typical values are 100…200ms.

PON Power ON input

CMOS compatible, digital input; LOW active; by default set to HIGH via internal pull-up resistor.
By this pin the operation mode of IC is controlled. If PON is LOW (connected to GND), the receiver will be activated. If PON is HIGH, the receiver will switch to power-down mode.

DAT Data output

CMOS compatible, digital output w/o any internal pull-resistors.
At the data output pin DAT you find the demodulated time code signal. By default (DATP open) output signal pulses will be HIGH-active (LHL). The polarity can be inverted to HLH once the DATP-pin is used accordingly.

CA1 / CA2 Antenna-Switch control inputs

CMOS compatible, digital inputs; LOW active; by default set to HIGH via internal pull-up resistor.
Inputs used to control the status of those two integrated PMOS-antenna-switches.
Once CA1/CA2 are not connected or set to HIGH then the antenna-switches are open (high impedance).
If one or both of these pins are set to LOW during reception mode, then the corresponding antenna switch is closed and the corresponding capacitor connected to CP1 / CP2 is added to the antenna capacitor.
If the receiver is switched OFF (PON=HIGH=V_{DD}) then also set CA1 = CA2 = HIGH.

VDD Supply voltage, input of voltage regulator

Once we have a 3V-application then the positive power supply voltage for the IC has to be connected to VDD only. It is recommended to provide corresponding RC-elements between VDD and GND in order to get a smooth power supply voltage.
Once the power supply voltage is 1.5V only then pins VDD and VCC should be connected together.

VCC Supply voltage, output of voltage regulator

Common input (together with VDD) of positive power supply voltage for 1.5V applications. An external capacitor (≥ 1µF) has to be connected between pin VCC and GND.
If there is used a 3V power supply voltage then pin VCC has to be connected to the external capacitor only!

GND Supply Ground

GND is the reference potential for all IC-stages and for the internal ESD protection circuit. GND is also connected to the IC-substrate.

VBS Input Bias voltage

Used only during unsymmetrical operation mode of antenna. A capacitor has to be connected between pin VBS and GND. In all other applications this pin shouldn't be connected.

10 Pad Layout and PAD Coordinates

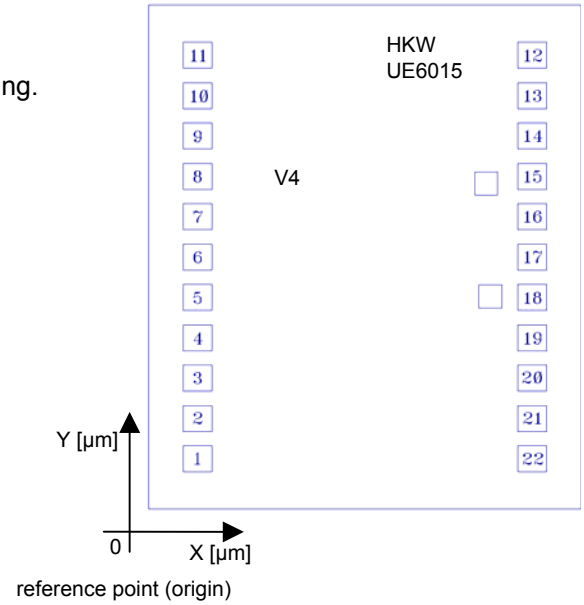
The UE6015 is available as DIE for "chip-on-board" mounting.

DIE size: 1470 µm x 1720 µm
Thickness: 330 µm

PAD size: 100 µm x 90 µm
min. pad-distance: 50 µm
min. pad-pitch: 140 µm

Once the chip-substrate has to be electrically connected then GND has to be used as reference voltage for the chip back-plane.

Note:
- Pad coordinates are refered to the center point of each pad.
- The reference point (origin) for the pad coordinates is the lower left chip edge (0;0).

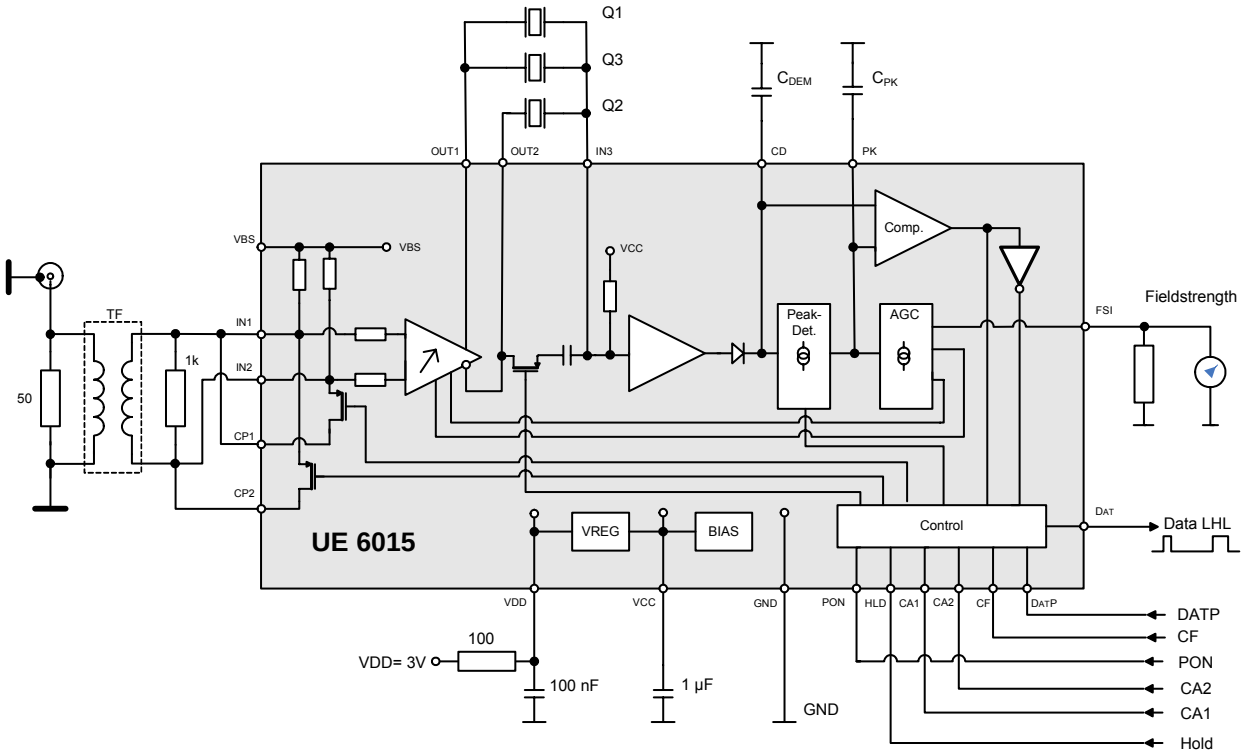


Pad # (dice)	Symbol	Function	x-axis (µm)	y-axis (µm)
1	CP2	PMOS antenna switch input 2	169.1	175.0
2	CP1	PMOS antenna switch input 1	169.1	315.0
3	IN1	Antenna input 1	169.1	455.0
4	IN2	Antenna input 2	169.1	595.0
5	VCC	Supply voltage, output of voltage regulator	169.1	735.0
6	VDD	Supply voltage, input of voltage regulator	169.1	875.0
7	OUT1	Crystal RF output 1	169.1	1015.0
8	OUT2	Crystal RF output 2	169.1	1155.0
9	GND	Supply Ground	169.1	1295.0
10	IN3	Crystal input 1	169.1	1435.0
11	CF	Filter Switch Input	169.1	1575.0
12	DATP	Data-Output-Polarity selection input	1330.9	1575.0
13	FSI	Field strength indicator output	1330.9	1435.0
14	CD	Demodulator output	1330.9	1295.0
15	HLD	AGC hold input	1330.9	1155.0
16	PK	Peak detector output	1330.9	1015.0
17	PON	Power ON input	1330.9	875.0
18	CA1	Antenna Switch control input 1	1330.9	735.0
19	CA2	Antenna Switch control input 2	1330.9	595.0
20	DAT	Data output	1330.9	455.0
21	VBS	Input bias voltage	1330.9	315.0
22	TP	TestPad – do not connect!	1330.9	175.0

11 Ordering Information

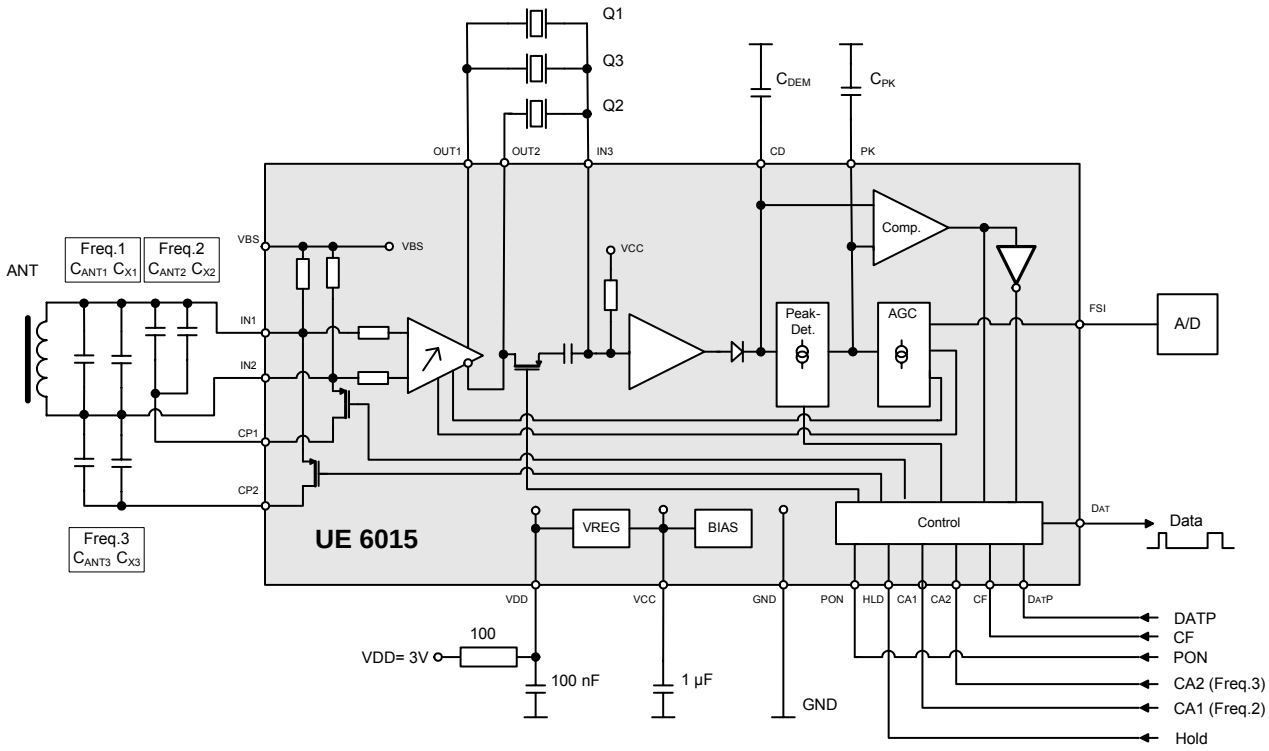
Extended Type Number	Package	Remarks
UE6015 DIT	No	DIE in trace

12 Test Circuitry



13 Application hints

13.1 General application circuit and recommended values (VDD=3V; symmetr. oper. of antenna)

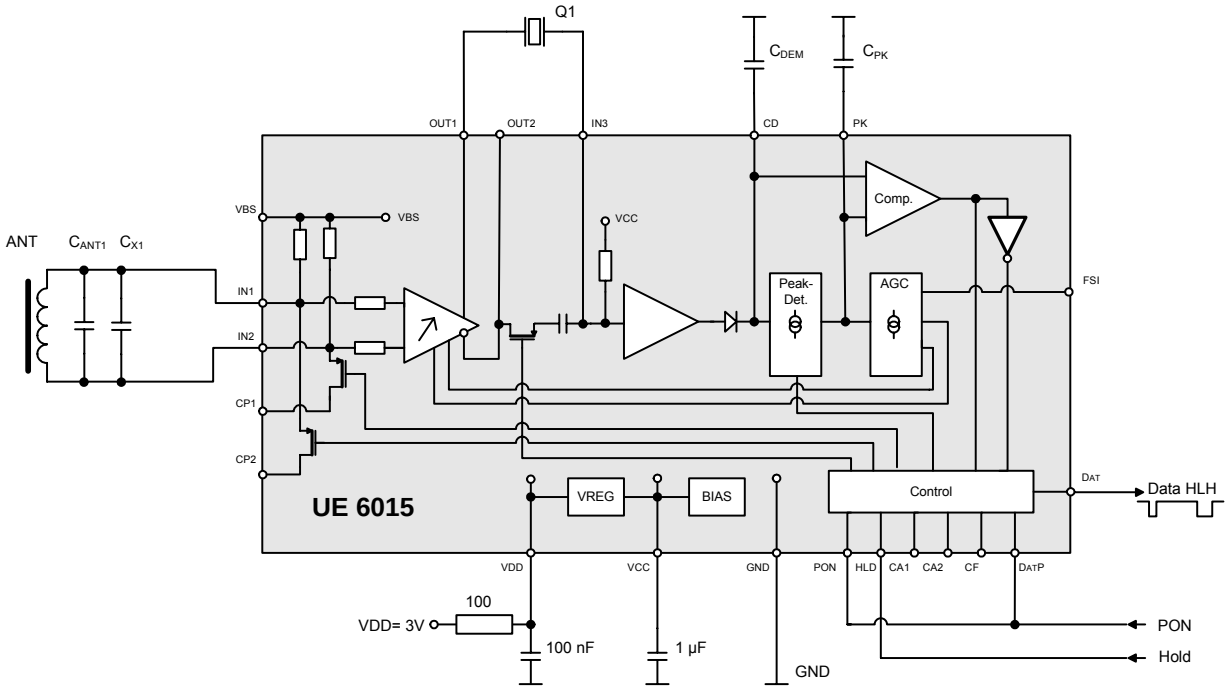


Recommended component values for a typical 3-band application (77.5kHz/60kHz/40kHz; symmetrical antenna operation; VDD=3V) based on the electrical scheme shown above:
Recommended antenna: resonant frequency = 77.5kHz ; L/C-ratio: L=2.29mH / C=1.8nF

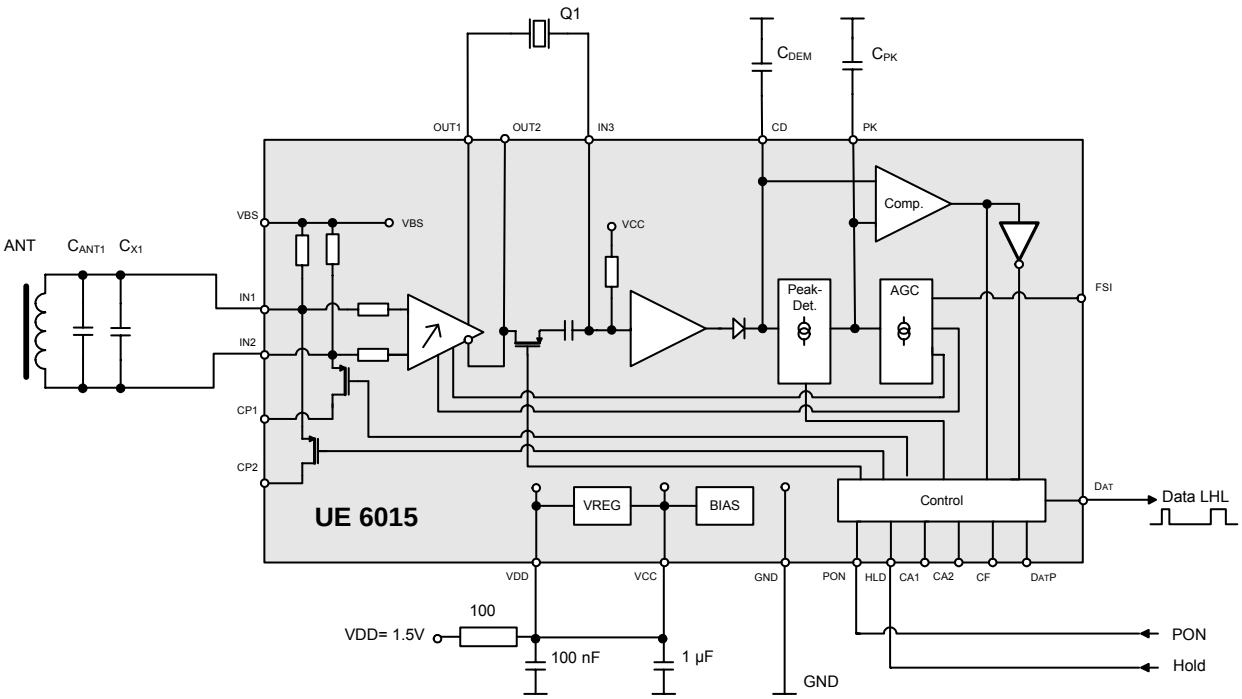
Selected Band (Carrier freq.)	Q1 [kHz]	Q2 [kHz]	Q3 [kHz]	ANT [kHz]	C_{DEM} [nF]	C_{PK} [µF]	C_{ANT1} + C_{X1} [nF]	C_{ANT2} + C_{X2} [nF]	C_{ANT3} + C_{X3} [nF]	CA1	CA2	CF
basic assy.	77.5	60	40	77.5	47	2.2	1.8	1.25	3.93			HIGH (open)
77.5kHz							active			HIGH (open)	HIGH (open)	
60kHz							active	active		LOW	HIGH (open)	
40kHz							active	active	active	LOW	LOW	

Remarks:
a) Pin CA1 controls the antenna switch input CP1 and therefore the use of the additional set of antenna capacitors C_{ANT2} + C_{X2} connected between IN1 and CP1.
b) Pin CA2 controls the antenna switch input CP2 and therefore the use of the additional set of antenna capacitors C_{ANT3} + C_{X3} connected between IN2 and CP2.
c) The values mentioned above for antenna capacitors are theoretical values calculated for the corresponding target frequency with reference to the specified “ideal” antenna. Capacitor- and antenna-tolerances as well as the influence of the product construction and product casing were not taken into account and should be respected accordingly during the antenna tuning procedure.

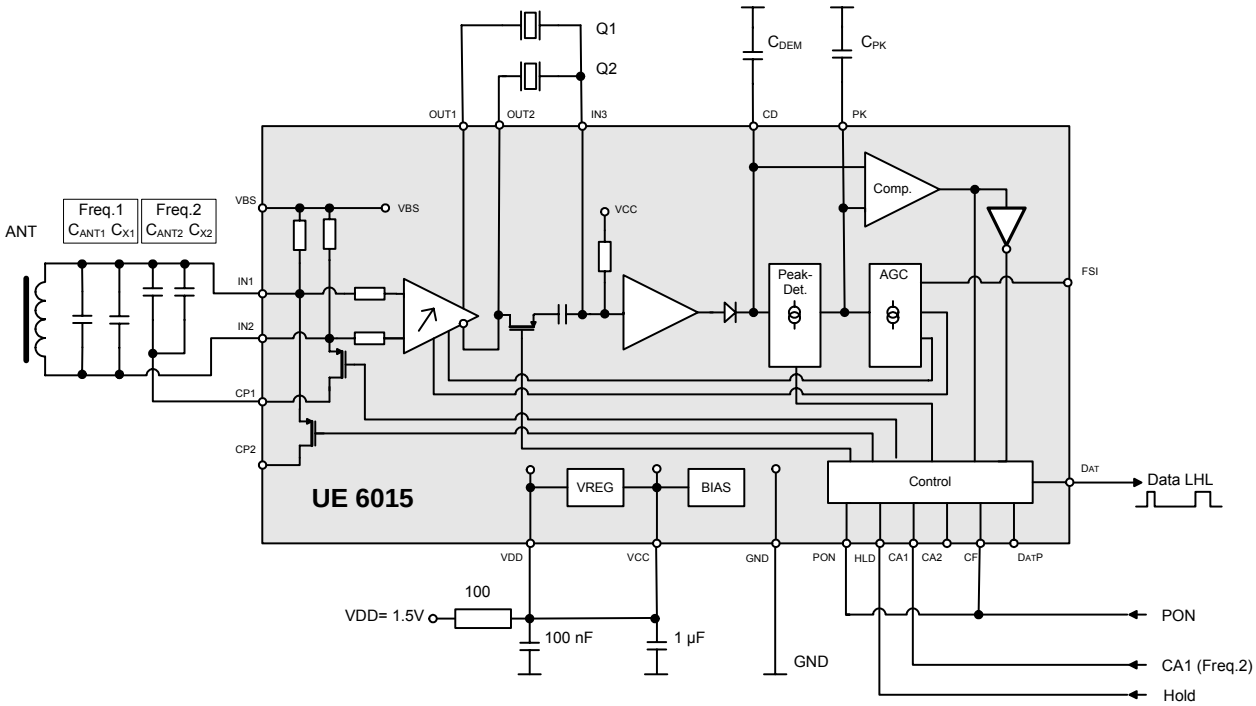
13.2 Application circuit (1-band; VDD=3V; symmetr. operation. of ANT; HLH)



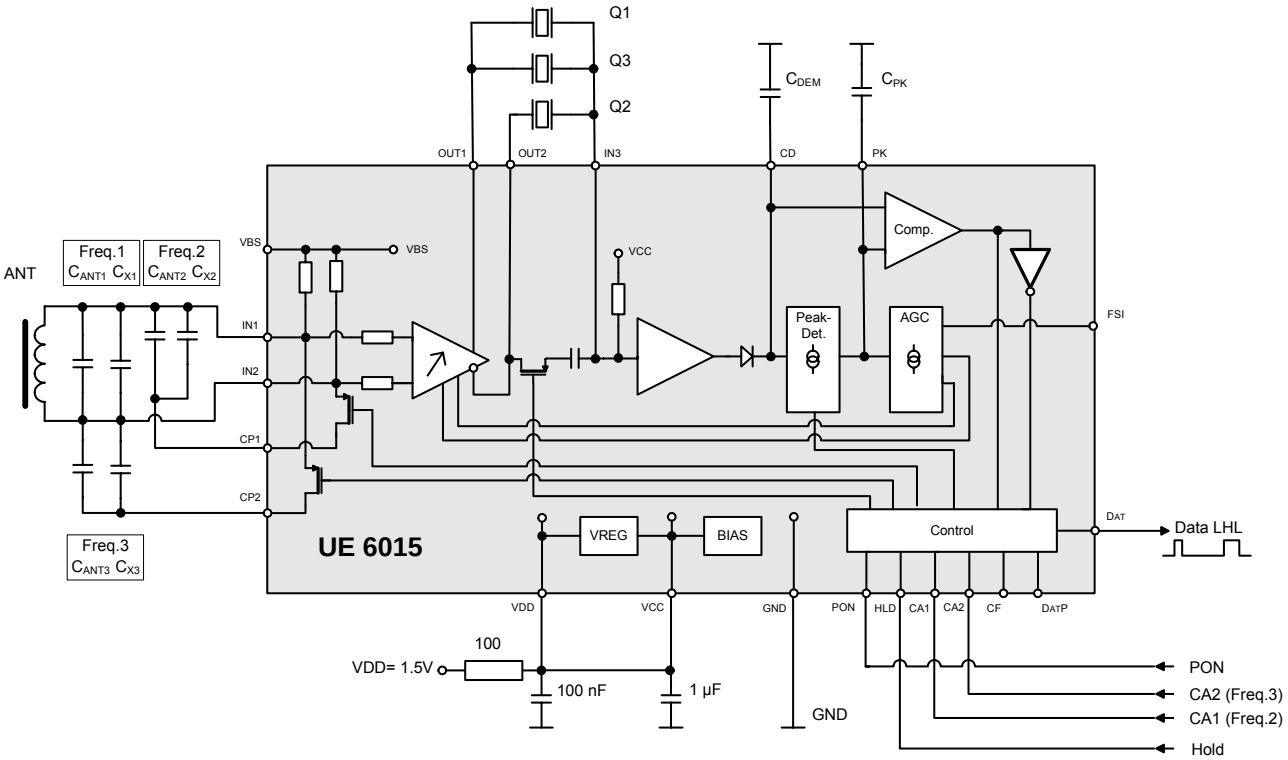
13.3 Application circuit (1-band; VDD=1.5V; symmetr. operation. of ANT; LHL)



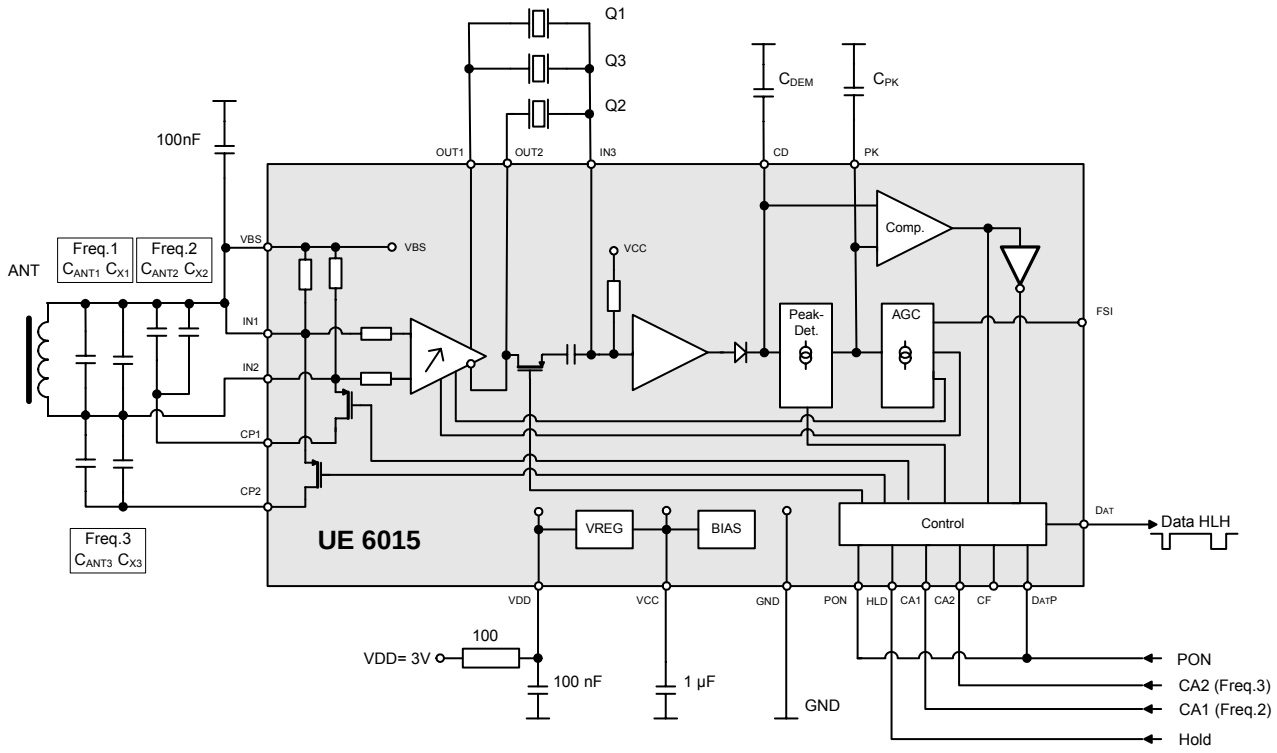
13.4 Application circuit (2-band; VDD=1.5V; symmetr. operation. of ANT; LHL)



13.5 Application circuit (3-band; VDD=1.5V; symmetr. operation. of ANT; LHL)



13.6 Application circuit (3-band; VDD=3V; unsymmetr. operation. of ANT; HLH)



13.7 General aspects concerning the use and connection of control pins CF, CA1, CA2, DATP

All these pins have internal pull-up resistors. By this way they are pre-defined to logic HIGH if no external circuit will force them to LOW = GND.

a) If HIGH-level is that logic level you need for your UE6015-configuration then simply keep the corresponding pin open (not connected).

b) Pin PON is used to switch ON the receiver circuit UE6015 (PON = LOW = GND). Once the UE6015 - configuration for your specific application needs other control-pins connected to LOW too (like CF, CA1, CA2, DATP) then we recommend to set them to LOW in combination with control-line PON. By this way you activate the corresponding control-pins only for the duration of any active reception attempt which minimizes the total power-consumption of UE6015.

13.8 General aspects concerning the use of antenna switches CP1, CP2

a) Antenna switches CP1 and CP2 are compatible to each other. For the realization of 2-band applications there can be used or switch CP1 or switch CP2. Please refer to the alternative solutions a) and b) described in table 13.8 proposed for a typical 2-band configuration.

b) Improvement of antenna effectivity for multiband applications
The antenna for multiband-applications is initially specified and optimized (no. of windings) for the highest frequency to be received. Switching the same antenna to any other, lower frequency by connecting additional antenna-capacitors in parallel, the L/C ratio of antenna automatically becomes suboptimal for the corresponding frequency. This effect cannot be avoided.
In the same time the antenna quality factor has to suffer from the influence of the internal, parasitic channel-impedance of each antenna switch too. The influence of this channel resistance can be reduced if both antenna-switches are used simultaneously.

Therefore, for a 3-band application it is recommended to use both antenna switches (and not only one) in order to tune the antenna to the lowest requested frequency (table 13.8).
In some dual-band watch-applications it can be also useful to split the value of the additionally needed antenna-capacitor into two, approx. equal capacitors, to connect each one of them between CP1 and IN1 respectively between CP2 and IN2 and to operate both antenna switches simultaneously to switch the antenna from frequency 1 to the lower frequency 2.
This procedure helps to improve the antenna-effectivity by reducing the influence of the channel-resistance.

c) possible realization of antenna switching for some typical UE6015-configurations

carrier freq. to be received [kHz]	CA1	CA2	CF	CP1	CP2	target freq. of antenna [kHz]; (+/- offset freq.)	comments
1-band						77.5	
77.5	n.c.	n.c.	n.c.= HIGH	n.c.	n.c.		
2-band a)						60	
60	HIGH	n.c.= HIGH	LOW	open	n.c.		using antenna-switch CA1/CP1
40	LOW			closed	n.c.		
2-band b)						60	
60	n.c.= HIGH	HIGH	LOW	n.c.	open		using antenna-switch CA2/CP2
40		LOW		n.c.	closed		
2-band c)						60	
60	HIGH	HIGH	LOW	open	open		splitting the addit. antenna-cap. and using both antenna-switches together
40	LOW	LOW		closed	closed		
3-band						77.5	
77.5	HIGH	HIGH	n.c.= HIGH	open	open		
60	LOW	HIGH		closed	open		
40	LOW	LOW		closed	closed		using both antenna-switches together

table 13.8: possible realization of antenna switching for some typical UE6015-configurations (n.c. = not connected)

13.9 Special characteristic of Data output DAT

The internal configuration and driving capability of pin DAT allows the direct connection of test- and measurement equipment without big influence onto the reception characteristics. This is an enormous advantage with focus to the arrangement of functional tests of the receiver IC during any production line.

13.10 Advantage of symmetrical antenna connection

The symmetrical connection of antenna is useful especially in applications of digital RC-clocks and –watches. It reduces the interference level seen on the input of UE6015 once it is applied in a noisy environment. There can be reduced, for example, the effect of interferences created by LCDs, matrix-keyboards, etc.

13.11 Typical use of FSI-output

In order to get an information about the existing field-strength of received signal and in order to make a further evaluation of the receiption environment, the FSI-output current can be used. An easy and practical way is the connection of a resistor (47kΩ .. 100kΩ) between FSI-output and GND (figure 13.11.a). Typical values of the characteristic between input voltage V_{IN} of receiver circuit (function of the existing field strenght and antenna factor of used antenna) and V_{FSI} are given in table 13.11 and in figure 13.11.b .

Remarks:
a) type of antenna used for this example: 8mm x 60mm / 77.5kHz
b) R_{FSI} = 47kohm
c) Measurements were made in a shielded room.

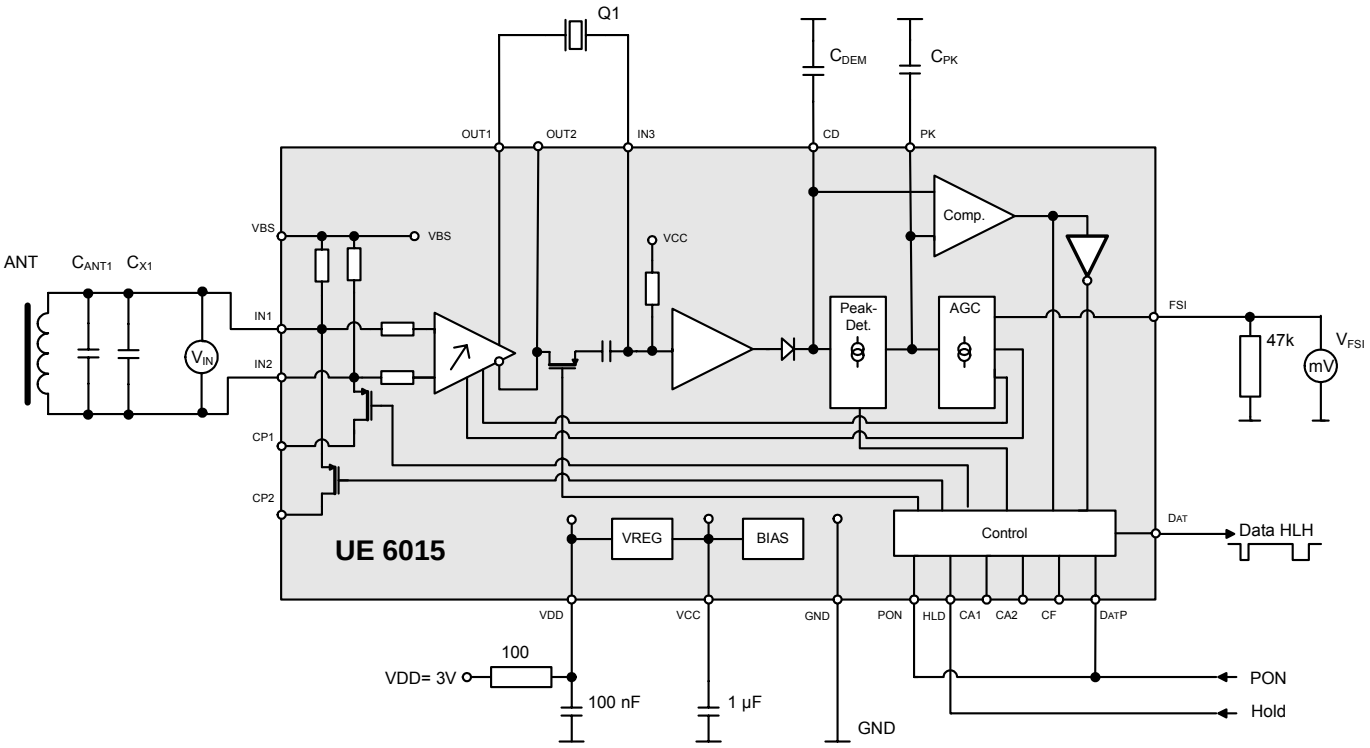


Figure 13.11.a: application circuit used

field strenght of received time code signal E [dBµV/m]	input voltage measured at the antenna input of UE6015 Vin [dBµV]	FSI-output voltage @47kohm V_{FSI} [mV]
30	6	162
35	11	189
40	16	219
45	21	253
50	26	286
55	31	320
60	36	349
65	41	377
70	46	399
75	51	420
80	56	438
85	61	453
90	66	465
95	71	475
100	76	484
105	81	492
110	86	497
115	91	501
120	96	503

Table 13.11: values measured

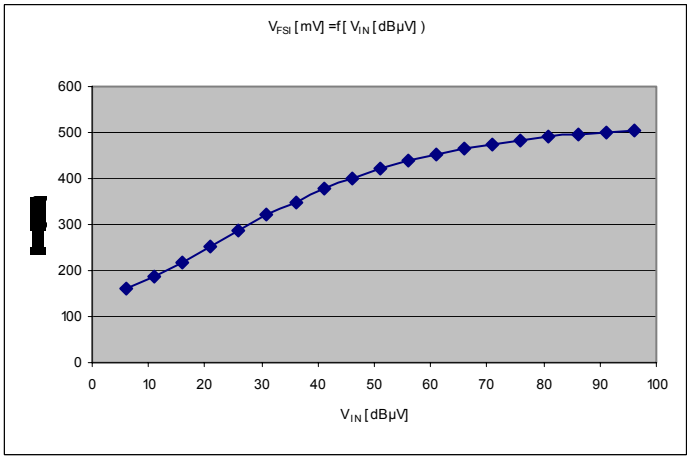


Figure 13.11.b: resulting characteristic
V_{FSI} [mV] = f[V_{IN} [dBµV])

14 Disclaimer of Warranty

HKW-Elektronik GmbH
Industriestraße 12
D-99846 Seebach
Germany

Tel.: +49 (0)36929 82330
Fax: +49 (0)36929 82339
Internet: http://www.hkw-elektronik.de
email: kontakt@hkw-elektronik.de

Distributed by: