

MULTI-STANDARD FULLY INTEGRATED 13.56-MHz RADIO FREQUENCY IDENTIFICATION (RFID) ANALOG FRONT END AND DATA-FRAMING READER SYSTEM

FEATURES

- Completely Integrated Protocol Handling (OSI Model Layer 3 and Below)
- Separate Internal High-PSRR Power Supplies for Analog, Digital, and PA Sections Provide Noise Isolation for Superior Read Range and Reliability
- Dual Receiver Inputs With AM and PM Demodulation to Minimize Communication Holes (Patent Pending)
- Receiver AM and PM RSSI
- Reader-to-Reader Anti-Collision
- High Integration Reduces Total BOM and Board Area
 - Single External 13.56-MHz Crystal Oscillator
 - MCU-Selectable Clock-Frequency Output of RF, RF/2, or RF/4
 - Adjustable 20-mA, High-PSRR LDO for Powering External MCU
- Easy to Use With High Flexibility
 - Auto-Configured Default Modes for Each Supported ISO Protocol
 - 11 User-Programmable Registers
 - Selectable Receiver Gain and AGC
 - Programmable Output Power (100 mW or 200 mW)
 - Adjustable ASK Modulation Range (8% to 30%)
 - Built-In Receiver Band-Pass Filter With User-Selectable Corner Frequencies
- Wide Operating Voltage Range of 2.7 V to 5.5 V

- Ultralow-Power Modes
 - Power Down < 1 μ A
 - Standby 120 μ A
 - Active (Rx only) 10 mA
- Parallel 8-Bit or Serial 4-Pin SPI Interface With MCU Using 12-Byte FIFO
- Ultrasmall 32-Pin QFN Package (5 mm x 5 mm)
- Available Tools
 - Reference Design/EVM With Development Software
 - Source Code Available for MSP430

APPLICATIONS

- Secure Access Control
- Product Authentication
 - Printer Ink Cartridges
 - Blood Glucose Monitors
- Contactless Payment Systems

DESCRIPTION

The TRF7960/61 is an integrated analog front end and data-framing system for a 13.56-MHz RFID reader system. Built-in programming options make it suitable for a wide range of applications for proximity and vicinity RFID systems.

The reader is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

Table 1. PRODUCT SELECTION TABLE

DEVICE	PROTOCOLS					
	ISO14443A/B				ISO15693 ISO18000-3	Tag-it™
	106 kbps	212 kbps	424 kbps	848 kbps		
TRF7960	X	X	X	X	X	X
TRF7961					X	X



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Tag-it is a trademark of Texas Instruments Incorporated.

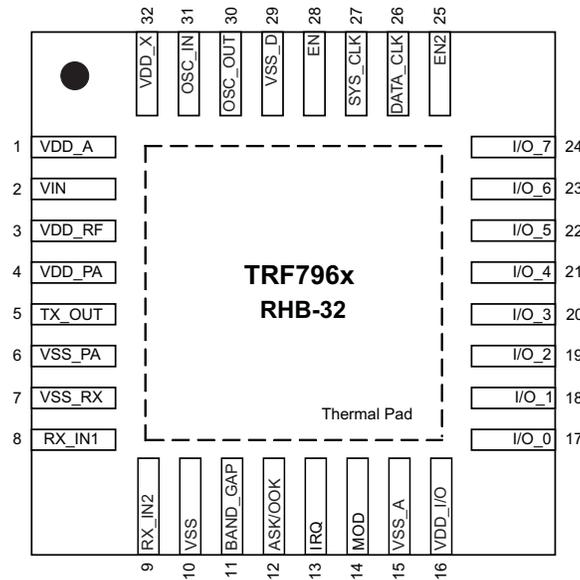


Figure 2. TRF796x Pin Assignments (Top View)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
VIN	Supply voltage	6	V
I _O	Output current	150	mA
Continuous power dissipation		See Dissipation Rating Table	
T _J	Maximum junction temperature, any condition ⁽²⁾	140	°C
	Maximum junction temperature, continuous operation, long-term reliability ⁽²⁾	125	°C
T _{stg}	Storage temperature range	-55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C
ESDS rating	HBM (human body model)	2	kV
	CDM (charged device model)	500	V
	MM (machine model)	200	

- (1) The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified are not implied.
- (2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

TABLE 5. PACKAGING/ORDERING INFORMATION⁽¹⁾

PACKAGED DEVICES	PACKAGE TYPE ⁽²⁾	TRANSPORT MEDIA	QUANTITY
TRF7960RHBT	RHB-32	Tape and reel	250
TRF7960RHBR		Tape and reel	3000
TRF7961RHBT	RHB-32	Tape and reel	250
TRF7961RHBR		Tape and reel	3000

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DISSIPATION RATINGS TABLE PER PACKAGE

PACKAGE	θ_{JC} (°C/W)	$\theta_{JA}^{(1)}$ (°C/W)	POWER RATING ⁽²⁾	
			$T_A \leq 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$
RHB (32)	31	36.4	2.7 W	1.1 W

- (1) This data was taken using the JEDEC standard High-K test PCB.
 (2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Supply voltage	2.7	5	5.5	V
T _J	Operating virtual junction temperature range	–40		125	°C
T _A	Operating ambient temperature range	–40	25	110	°C
	Load impedance at TX OUT (pin 5)		10		Ω

PRODUCT INFORMATION

Full product information is available by contacting TI's Product Information Center (PIC) as shown herein:

- [TI SC Product Information Center - Americas](#)
- [TI SC Product Information Centre - Europe Middle-East Africa](#)
- [TI SC Product Information Center - Japan](#)
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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TRF7960RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRF7960RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRF7961RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRF7961RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

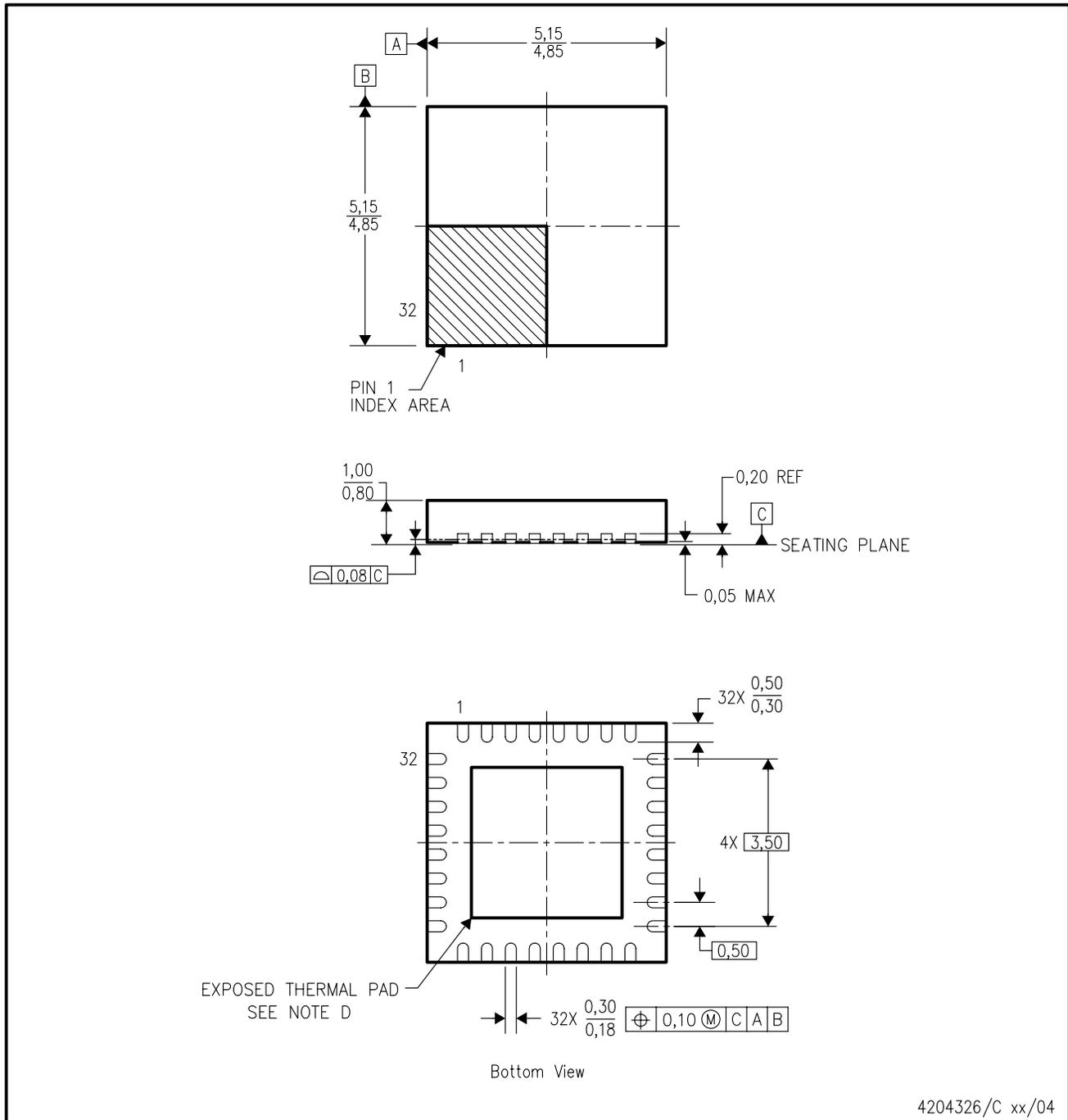
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RHB (S-PQFP-N32)

PLASTIC QUAD FLATPACK



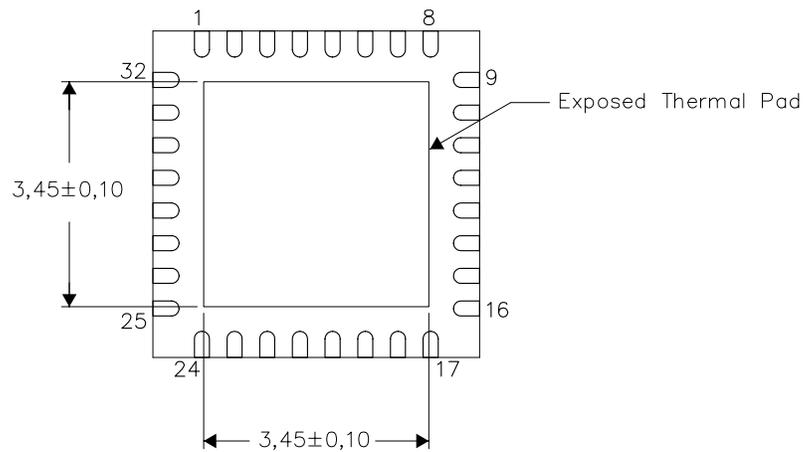
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

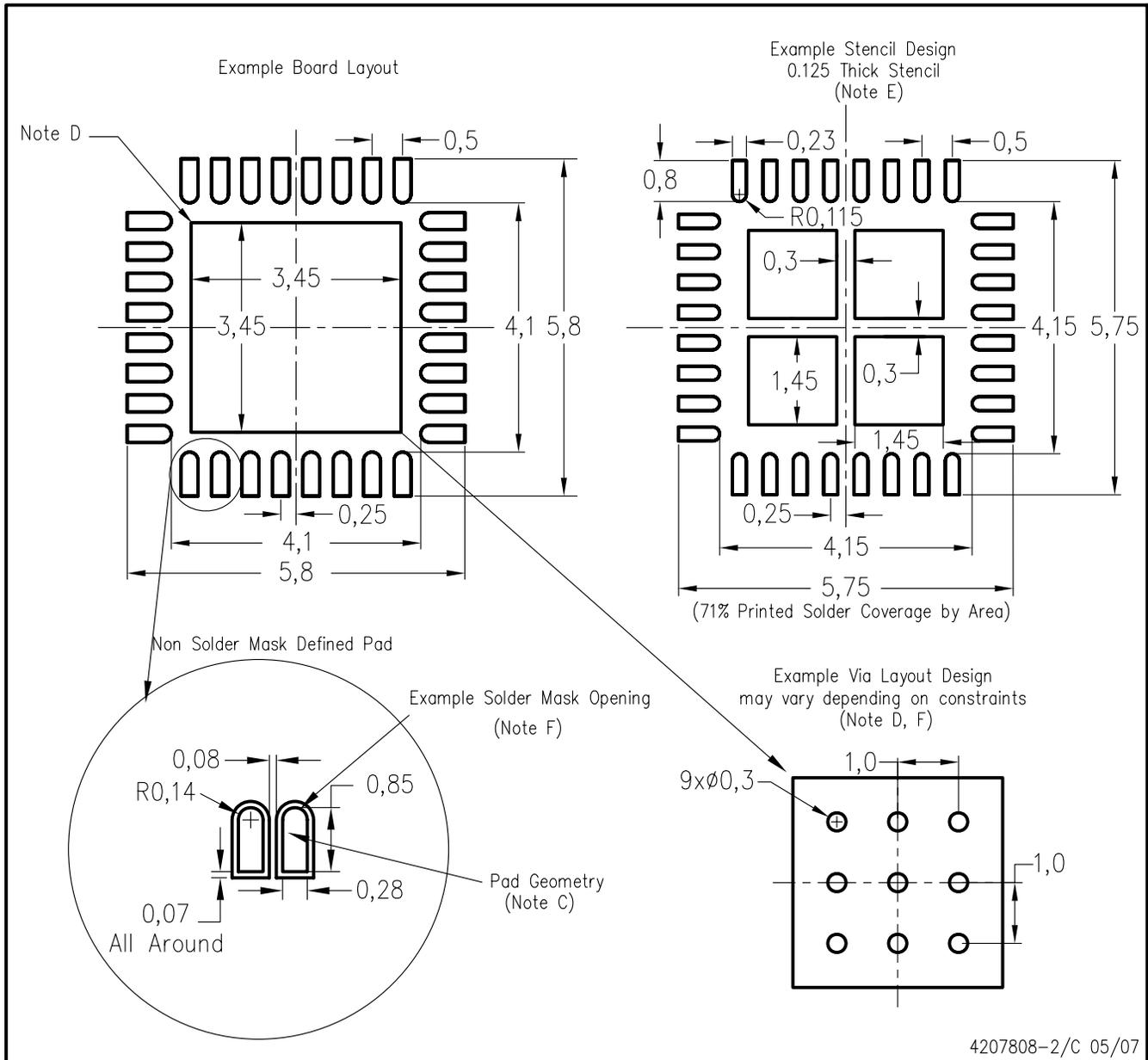


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S-PQFP-N32)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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