Open LVDS Display Interface (OpenLDI) Specification

v0.95

May 13, 1999

This is a draft standard and is subject to change. Implementations built to this draft standard may not be compliant with the standard when it is finally published.

Foreword

The OpenLDI specification was developed through the cooperation of companies in the semiconductor, display, computer system, connector, and cable industries to be an open standard for the digital connection of display sources and display devices. This standard is an evolution of the de facto industry standard for the connection of display controllers to LCD panels in notebook computers. The OpenLDI standard draws upon the work of other standards that are widely used, specifically the Video Electronics Standards Association (VESA) and the American National Standards Institute (ANSI). This standard provides a completely digital, plug and play, interface to provide the sharpest, clearest video image obtainable on a digital display device.

This standard was developed such that there is no material in this standard for which licensing fees must be paid nor for which membership in a particular organization is required (with the concomitant required sharing of intellectual property) in order to implement this standard.

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1 Scope

The OpenLDI specification describes a logical, electrical, and mechanical interface between a display source and a display device for the transfer of digital display data. Included in this interface are communication channels for display identification (DDC/CI and EDID) and connection of peripheral devices (USB). Use of this interface is appropriate for both direct attachment of a display source to a display device in a single assembly, e.g. notebook computers and single cabinet HDTVs, as well as for attachment of a display source to a remote display device, e.g., standalone LCD computer monitors. OpenLDI is an evolutionary development of the de facto industry standard for the interconnection of video controllers to LCD panels in notebook computers.

2 Purpose

The purpose of the OpenLDI specification is to provide for the transfer of digital display data between a display source and a display device, avoiding the conversion of the display data into analog form with its resultant loss of information. Additionally, this specification describes a signaling mechanism that minimizes the number of wires that must be used to connect the display source and display device, as well as minimizes electromagnetic emissions. The interface described provides the flexibility to support a wide range of display formats, refresh rates, and pixel depths.

3 References and Definitions

3.1 Normative References

The following standards are referenced in this specification and their provisions are incorporated where they are cited. The versions listed are current at the time of publication of this specification.

VESA[1] Display Data Channel Command Interface (DDC/CI) Standard, Version 1, August 14, 1998.

VESA Extended Display Identification Data (EDID) Standard, Version 3, November 13, 1997.

Universal Serial Bus Specification, Version 1.0, January 15, 1996.

ANSI/TIA/EIA-644-1995 Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, November 1995.

ANSI/EIA 364-C-1994 Electric Connector Test Procedure

[1] VESA is a registered trademark of the Video Electronics Standards Association.

3.2 Definitions

LVDS	Low Voltage Differential Signaling (ANSI Standard 644)
LDI	LVDS Display Interface
DDC	Display Data Channel
EDID	Extended Display Identification Data
USB	Universal Serial Bus

3.3 Language Conventions

This standard includes normative requirements, optional requirements, and descriptive text. Normative requirements are indicated by the use of the word “shall.” Normative requirements must be incorporated into an implementation of this standard for the implementation to be considered conformant to this standard. Optional requirements are indicated by the use of the word “may.” Optional requirements need not be incorporated into an implementation of this standard for the implementation to be considered conformant to this standard. However, if the optional requirement is implemented, it must be implemented as stated in this standard.

Any text in this standard that does not use either “shall” or “may” is considered descriptive. Descriptive text is used for illustrative purposes only and does not place any requirement on an implementation.

3.4 Ordering Conventions

This standard refers to the individual bits of a multi-bit construct using the following conventions. Multi-bit constructs are written showing both the greatest and the least numbered bits of the construct. The least significant bit of a construct is bit 0 (zero).

When a figure is used to convey information along a time axis, time will flow from left to right. Thus, earlier events are to the left of later events.

4 Overview

With the proliferation of digital display devices, typically flat panel LCDs but also plasma and other technologies, the traditional analog video interface between the display source and display device is not sufficient to provide the image fidelity that is available from both the source and display. OpenLDI describes an interface between a display source and display device that is entirely digital. Any loss of image fidelity that is the result of the conversion of digital display data into analog form for transmission from the source to the display is eliminated.

This standard describes a plug and play mechanism to convert digital parallel pixel data, synchronization and control signals to a serial bit stream, transfer this bit stream from the display source to the display device over a multi-conductor cable and recover the parallel pixel data, synchronization and control signals at the display. The standard also describes an electrical interface that enables the transmission of the pixel, synchronization and control information using a minimum number of conductors, while also minimizing radiated emissions and susceptibility to electromagnetic interference. The final portion of the standard describes the mechanical interface and cable assembly.

5 Logical Interface

5.1 Overview

Display information in digital systems is represented in pixels. Each pixel represents a single, tiny element of the information to be displayed. By combining a large number of individual pixels, displays of any size may be created. The size of a display is measured in the number of pixels contained in one horizontal row and the number of rows that are stacked vertically. Thus, a display that is 640 pixels wide and 480 rows tall is said to be a 640×480 display and contains 307,200 pixels.

In digital systems, each pixel is a binary encoding of color and intensity. The number of bits used to encode this information is often referred to as the color depth or color resolution. Monochrome systems often use a single byte to encode each pixel, resulting in a total of 256 available shades. Color systems commonly use 18 or 24 bits to encode each pixel, resulting in 262,144 or 16,777,216 colors.

Pixels are usually stored in the display source in a memory called a frame buffer. The pixels are stored in parallel format and sent out serially to the display device. The order in which the pixels are sent to the display device is based on the electron beam scanning method used in analog CRTs, since most display controllers in use are designed to support CRTs. The electron beam scanning pattern of a CRT begins in the upper left corner of the display and proceeds horizontally to the right, completing one scan line. During this scan line, the controller sends each of the pixels for the first scan line to the display. After completing the first scan line, the display controller issues a horizontal sync, returning the electron beam to the left edge of the display, ready to begin the second scan line. The controller sends the pixels for the second scan line as the electron beam again proceeds horizontally to the right. Again the controller sends a horizontal sync to return the beam to the left. This process continues until all of the scan lines have been sent to the display. After the end of the last scan line, the controller issues a vertical sync, along with the horizontal sync, that causes the electron beam to return to the upper left corner of the display, ready to begin the process again. The time when the electron beam is returning to the beginning of a scan line is called the retrace time. The total time for both horizontal and vertical retrace can consume as much as 40% of the total time required to display an image on a CRT.

Because most display controllers are designed for use with CRTs, the order in which pixels are sent to a flat panel display is, generally, the same as that in which they are sent to a CRT. There are some exceptions to this statement, particularly where two pixels are sent simultaneously. The synchronization signals are also the same, though the signal names may be different. When two pixels are sent to the display simultaneously, the display is normally divided into an upper and a lower half, with one pixel being sent to the upper half of the display and the other sent to the lower half. The scan lines are synchronized in both halves of the display such that the upper and lower scan lines begin and end at the same time. The vertical scanning of the upper and lower halves of the display is also synchronized. Because newer display technologies are not based upon the electron gun technology of CRTs, these technologies require little or no time to be allocated for retrace. Without the bandwidth consumed by retrace, pixels may be sent to a

display using new technology at a lower rate than would be required for a display of the same size on a CRT.

OpenLDI serializes the parallel pixel data and sends it from the display source to the display device where the pixels are once again returned to their parallel format. Conceptually, the architecture of OpenLDI is shown in Figure 5-1.

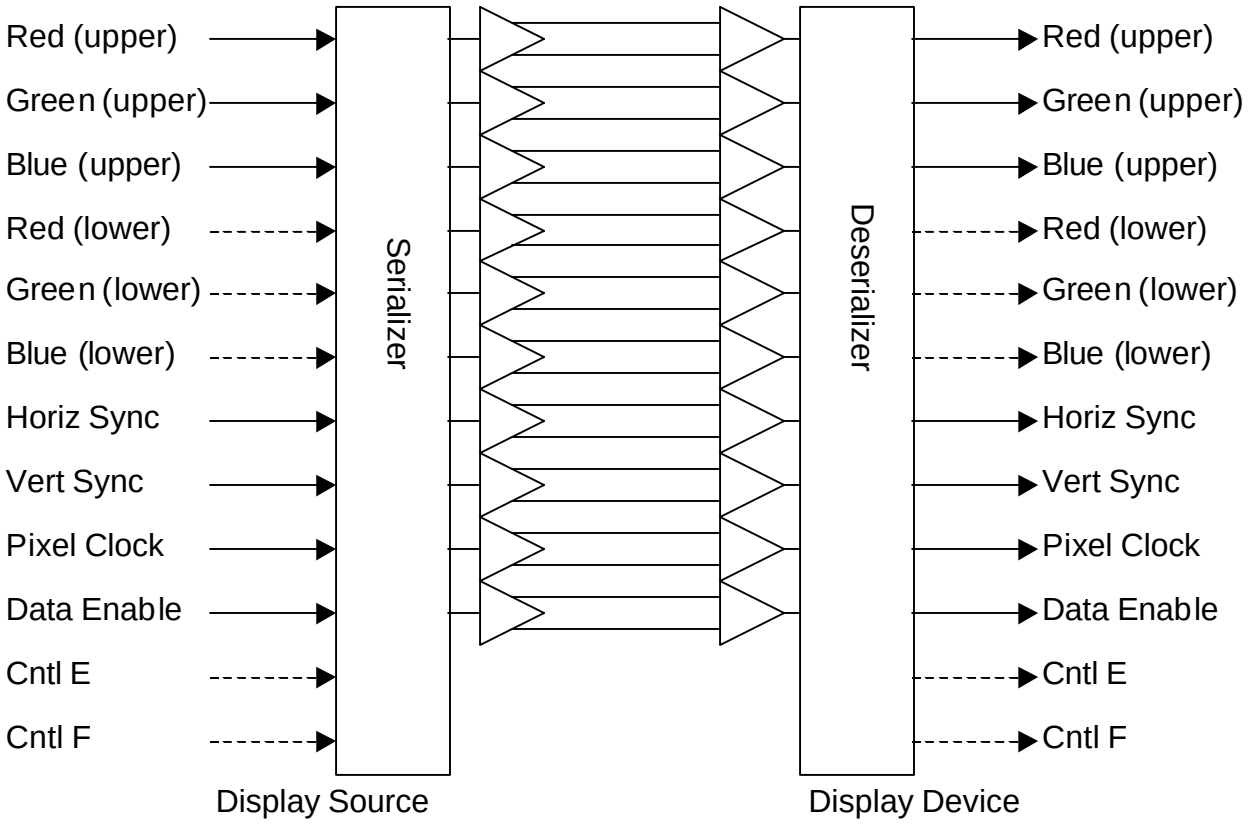


Figure 5-1, OpenLDI Architecture

The input signals to the OpenLDI transmitter at the display source are the pixel data, horizontal synchronization, vertical synchronization, a data enable control, the pixel clock, and two miscellaneous control signals. These signals are serialized and transmitted over LVDS differential pairs. At the display device the LVDS signals are received, converted to parallel form and output from the OpenLDI receiver.

The object of this section of the standard is to describe how the various parallel pixel formats that are stored in a frame buffer and the synchronization information are to be sent over the OpenLDI to the display device.

5.1.1 Security of Data Transmitted via OpenLDI

OpenLDI provides a “clear channel” interface. It does not provide protection of the digital video stream through encipherment, or any other mechanism. If protection of the data transferred via OpenLDI is desired, such protection should be performed prior to making the pixel data available to OpenLDI for transmission in the display source. A corresponding mechanism to recover the protected pixel information will be required in the display device.

Protection of the digital display information transmitted over the OpenLDI interface is a subject of ongoing investigation. This issue may be addressed in a future version of this standard.

5.2 Operation of OpenLDI

When power is initially applied to an OpenLDI display source, default configurations are used to ensure a visible display is provided to the viewer and that the display device is not damaged. This section describes the plug and play operation of OpenLDI, its default configuration and the procedure for changing the configuration to adapt to available display device resolutions.

5.2.1 Default Configuration of OpenLDI

5.2.1.1 Default Configuration for a Display Source

Upon the initial application of power to an OpenLDI display source, the default configuration for the interface shall be that the interface is programmed to display a 640×480, 60 Hz, VGA image using the single pixel mode and 24 bits per pixel. The display source shall implement all OpenLDI interface lines. The interface shall enable only the lower pixel interface lines. This configuration shall be maintained until such time as the EDID data structure may be retrieved from the display device using the DDC2B protocol and alternate configurations, mutually supported by both display source and display device, may be determined.

5.2.1.2 Default Configuration for a Display Device

Upon initial application of power to an OpenLDI display device, the default configuration for the interface shall be to receive a 640×480, 60 Hz, VGA image using the single pixel mode and 18 bits per pixel. A display device may implement 640×480, 60 Hz, and 24 bits per pixel, as its default configuration. The display device may implement only those OpenLDI interface lines that are necessary for support of the included display resolutions. Any unimplemented OpenLDI interface lines shall be properly terminated. The interface shall receive only on the lower pixel interface lines, while in the default configuration. This configuration shall be maintained until such time as the EDID data structure may be retrieved from the display device using the DDC2B protocol and alternate configurations, mutually supported by both display device and display source, may be determined. The display device shall be able to respond using the DDC2B protocol immediately upon the application of power to the display device or upon the connection of the OpenLDI interface, whichever occurs later.

The default VGA display is not required to fill the entire display area. It may occur at any location in the display area and may be repeated. If display scaling is available from the display device, it may be used to scale the VGA display information to fill the entire display area.

If no signal is detected on the OpenLDI interface, the display device may blank the display and enter a low power standby mode of operation, waiting to receive from the OpenLDI interface.

5.2.2 Plug and Play Operation of OpenLDI

OpenLDI provides for full plug and play, hot plug operation. This allows for the connection or removal of a display device to a display source at any time, without damage or additional user intervention. This section describes this operation.

5.2.2.1 Display Device Attach Event

A Display Device Attach hot plug event shall be detected by the display source when a current draw in excess of 1mA is detected on the +5Vdc DDC power pin. This event shall be provided to the system to which the display source is attached, allowing the system to retrieve the EDID data structure from the display device, to determine mutually supported configurations, and to adapt the configuration of the OpenLDI interface. Until such time as the EDID is retrieved and a mutually supported configuration is determined, the display source shall operate in the default configuration, as described in 5.2.1.1

5.2.2.2 Display Device Removal Event

A Display Device Removal hot plug event shall be detected by the display source when a current draw less than 500µA is detected on the +5Vdc DDC power pin. This event shall be provided to the system to which the display source is attached, allowing the system to disable the OpenLDI interface.

5.2.2.3 Display Source Attach Event

The display device shall detect a Display Source Attach event when the voltage on the +5Vdc DDC power pin exceeds 3.0V. The display device shall ensure that a minimum current of 1mA is drawn on this pin. The current draw on the +5Vdc DDC power pin shall not exceed 95mA.

When the Display Source Attach event is detected, the display device shall enable the OpenLDI interface in the default configuration, as described in 5.2.1.2.

5.2.2.4 Display Source Removal Event

The display device shall detect a Display Source Removal event when the voltage on the +5Vdc DDC power pin is less than 2.0V. The display device shall disable the OpenLDI interface. The display device may begin a standby mode of operation.

5.2.3 DDC

Both the display source and display device shall support DDC2B operation. The display source shall be capable of supplying a minimum of 100mA on the +5Vdc DDC power pin.

5.2.4 EDID

The display source shall support both EDID 1.3 and 2.0 data structures.

The display device shall support at least one of EDID 1.3 or 2.0 data structures. The default display device configuration may be omitted from the EDID data structure. However, it is recommended that all supported display modes be included in the data structure. If the display

device is fixed resolution, i.e., not capable of supporting other than a single display resolution, the EDID "Preferred Timing Mode" bit shall be set in the EDID data structure and the native resolution of the display device shall be reported in the first detailed timing field of the data structure. The Preferred Timing Mode bit is located at offset 18h, bit 1, in the EDID 1.2 data structure and at offset 7Eh, bit 0Eh in the EDID 2.0 data structure.

5.2.5 Gamma Correction

Because the vast majority of display sources are connected to CRT-based display devices, the display device precompensates the pixel data to display proper color on a CRT. Since the transfer characteristics of a CRT are not necessarily the same as those of other display device technologies, this precompensation, or "gamma" correction, must be removed in order to allow the display device to display the correct colors. The compensation factor is called gamma (γ) and is used in the following transfer function:

$Y = X^{\gamma}$,

where X is the "true" pixel color, Y is the pixel value required to display the true color of X on a particular display device, and γ is the conversion factor.

5.2.5.1 Display Source Gamma Correction

The display source shall apply a compensation factor of γ=1/2.2. This factor precompensates the pixel data for proper display on a CRT. The typical display transfer function of a CRT involves a γ=2.2.

5.2.5.2 Display Device Gamma Correction

The display device shall apply a gamma correction, specific to the technology of the display device, to the pixel data it receives. The OpenLDI pixel data will be precompensated as described in 5.2.5.1.

5.3 Pixel Formats

The following pixel formats are supported by OpenLDI: 18-bit single pixel, 24-bit single pixel, 18-bit dual pixel, and 24-bit dual pixel formats. All pixels represent RGB (red, green, blue) intensity information. Many arbitrary display resolutions are readily supported by OpenLDI. The common display resolutions supported are listed in Table 5-1.

Table 5-1, Common Display Resolutions

Resolution	Common Name
640×480	VGA
800×600	SVGA
1024×768	XGA
1280×1024	SXGA
1600×1024	SXGAW
1600×1200	UXGA
1920×1080	HDTV
1900×1200	UXGAW
2048×1536	QXGA

5.3.1 18-bit Single Pixel Format

The 18-bit single pixel format represents a pixel as three 6-bit values, R5-0, G5-0, and B5-0, one each for the intensity of red, green and blue. This pixel format shall be as defined for format 20h in Table 4.11 of the VESA EDID version 3 standard.

5.3.2 24-bit Single Pixel Format

The 24-bit single pixel format represents a pixel as three 8-bit values, R7-0, G7-0, and B7-0, one each for the intensity of red, green, and blue. This pixel format shall be as defined for format 24h in Table 4.11 of the VESA EDID version 3 standard.

5.3.3 18-bit Dual Pixel Format

The 18-bit dual pixel format represents two pixels as three pairs of 6-bit values,RU5-0, RL5-0, GU5-0, GL5-0, BU5-0, and BL5-0, each pair representing the intensity of red, green, and blue for the two pixels. This pixel format shall be as defined for format 34h in Table 4.11 of the VESA EDID version 3 standard.

5.3.4 24-bit Dual Pixel Format

The 24-bit dual pixel format represents two pixels as three pairs of 8-bit values, RU7-0, RL7-0, GU7-0, GL7-0, BU7-0, and BL7-0, each pair representing the intensity of red, green, and blue for the two pixels. This pixel format shall be as defined for format 38h in Table 4.11 of the VESA EDID version 3 standard.

5.4 Serialization

OpenLDI serializes the parallel pixel stream for transmission from the display source and the display device. There are 8 serial data lines (A0 through A7) and two clock lines (CLK1 and CLK2) in the OpenLDI interface. The number of serial data lines may vary, depending on the pixel formats supported. For the 18-bit single pixel format, serial data lines A0 through A2 shall be used. For the 24-bit single pixel format, serial data lines A0 through A3 shall be used. For the 18-bit dual pixel format, serial data lines A0 through A2 and A4 through A6 shall be used. For the 24-bit dual pixel format, serial data lines A0 through A7 shall be used. Only those serial data lines required for use by the formats supported by an implementation need to be active. The

serial data stream on each signal line shall be at a bit rate that is seven times the pixel clock. The CLK1 line shall carry the pixel clock. The CLK2 line shall also carry the pixel clock when dual pixel mode is used. When dual pixel mode is not used or when it is known that the display device does not require the CLK2 signal, CLK2 may be left inactive. The CLK2 signal is provided for compatibility with earlier systems and to support display device designs that use independent receivers for the upper and lower pixels.

There are two modes of operation, unbalanced and DC balanced. Each of the unbalanced and DC balanced modes use one mode for single pixel transmission and a second for dual pixel transmission. The following sections describe the operation in each mode for each pixel format. In the figures that follow, R, G, and B are used to represent the red, green, and blue components of single pixel formats. RU, BU, and GU are used to represent the red, blue, and green components of the upper pixel of dual pixel formats. Similarly, RL, BL, and GL are used to represent the components of the lower pixel. HSYNC, VSYNC, and DE are used to represent the horizontal synchronization, vertical synchronization, and data enable signals. In dual pixel formats, two additional, implementation specific control signals may be transmitted, CNTLE and CNTLF.

5.4.1 Mapping Pixel Bit Numbers Onto Interface Bit Numbers

The bit numbering of pixels in a typical display source frame buffer is big endian, where the most significant bit has the largest bit number. These bit numbers are not the same as those of the OpenLDI. Bit numbers shall be mapped as shown in Table 5-2.

Table 5-2, Bit Number Mappings

18 bits per pixel bit number	24 bits per pixel bit number	OpenLDI bit number
5	7	5
4	6	4
3	5	3
2	4	2
1	3	1
0	2	0
	1	7
	0	6

This method of bit mapping allows a display device that supports only 18 bits per pixel to connect to a display source using 24 bits per pixel and still display a useful image.

5.4.2 Unbalanced Operating Modes

In the unbalanced operating modes, only pixel and control information is sent from the display source to the display device. No provision is made to minimize either the short- or long-term buildup of DC bias on the signal lines.

5.4.2.1 18-bit Single Pixel Mode, Unbalanced

In the 18-bit single pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-2. Outputs A3 through A7 and CLK2 shall be inactive in this mode and fixed at a single value.

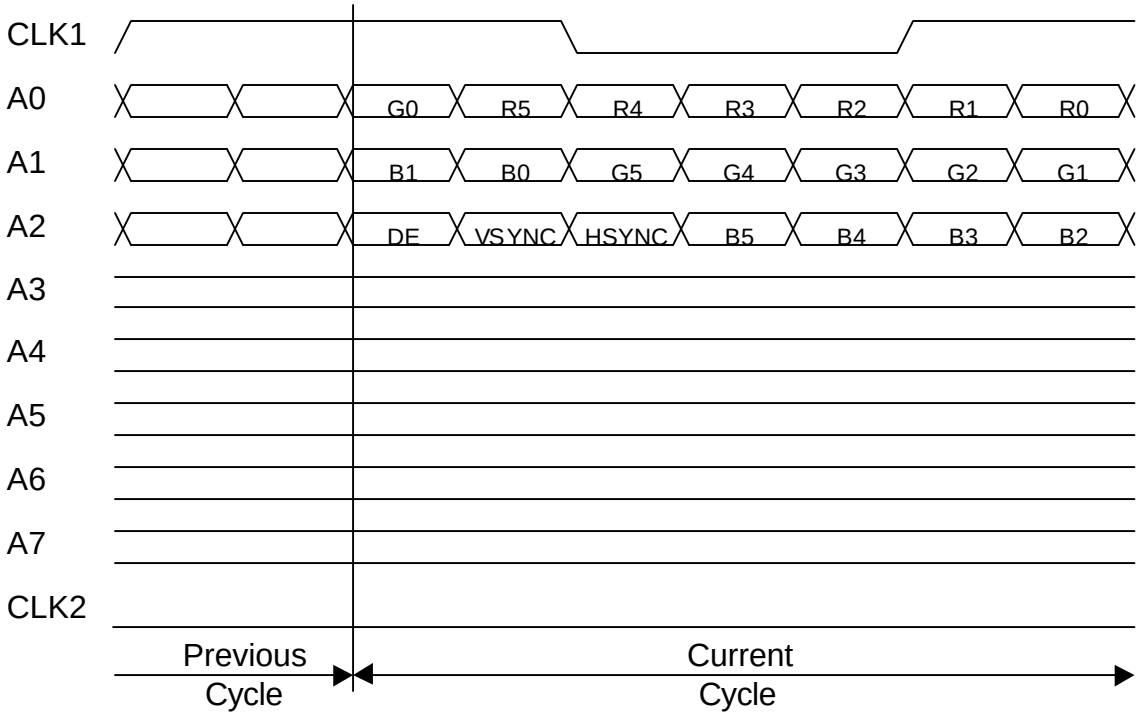


Figure 5-2, 18-bit Single Pixel Transmission, Unbalanced

5.4.2.2 24-bit Single Pixel Mode, Unbalanced

In the 24-bit single pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-3. Outputs A4 through A7 and CLK2 shall be inactive in this mode and fixed at a single value. Bits marked RES are reserved for future use and may take any value.

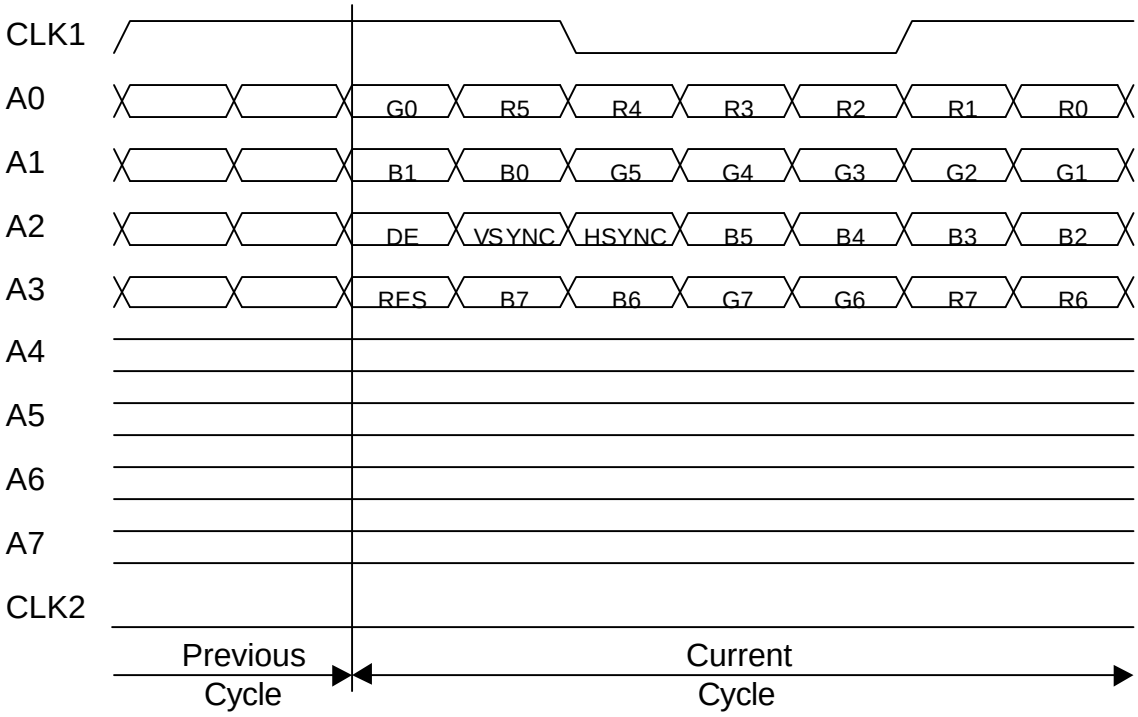


Figure 5-3, 24-bit Single Pixel Transmission, Unbalanced

5.4.2.3 18-bit Dual Pixel Mode, Unbalanced

In the 18-bit dual pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-4. Outputs A3 and A7 shall be inactive in this mode and fixed at a single value. Bits marked RES are reserved for future use and may take any value.

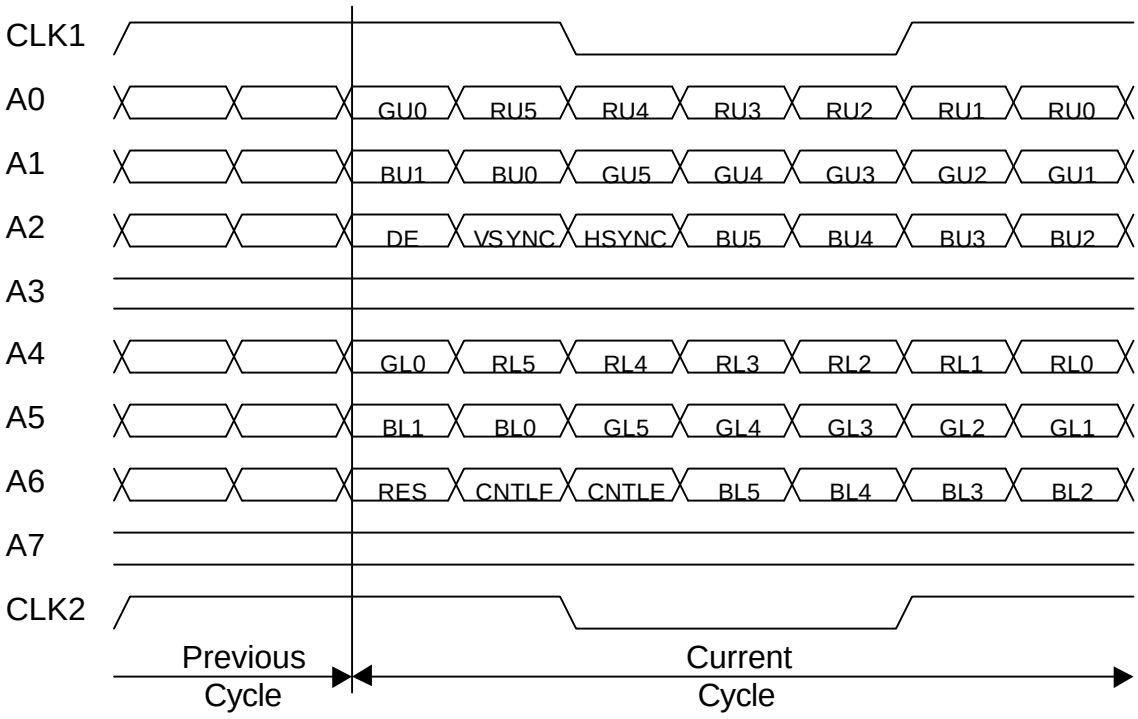


Figure 5-4, 18-bit Dual Pixel Transmission, Unbalanced

5.4.2.4 24-bit Dual Pixel Mode, Unbalanced

In the 24-bit dual pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-5. Bits marked RES are reserved for future use and may take any value.

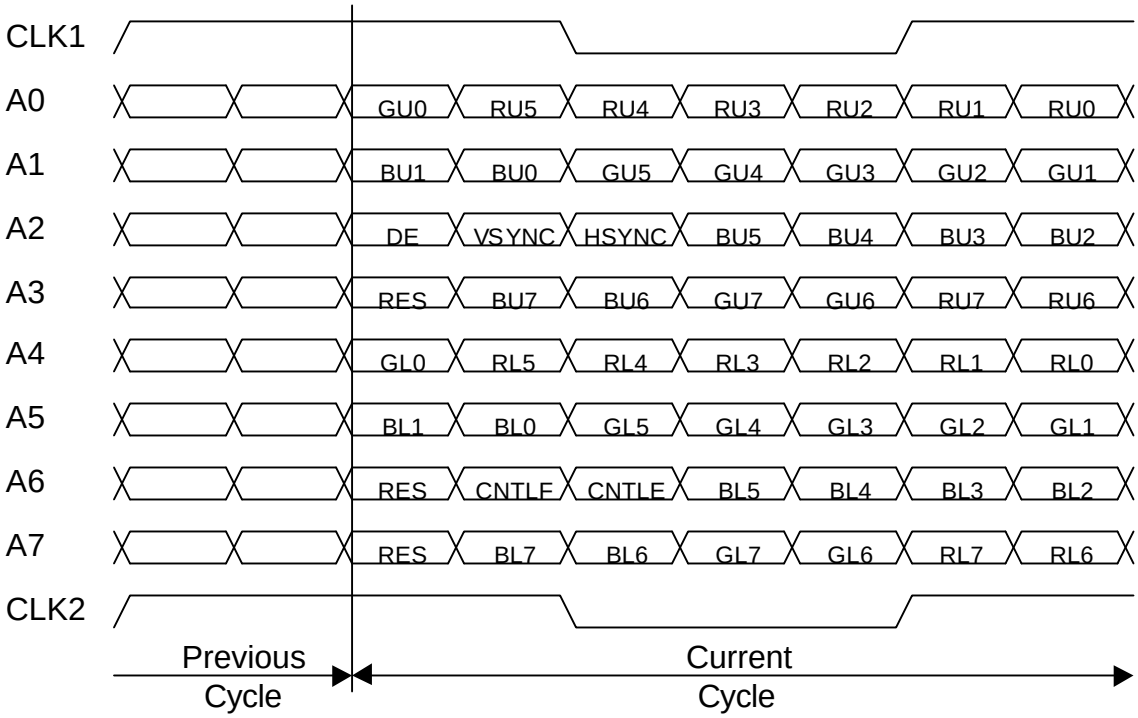


Figure 5-5, 24-bit Dual Pixel Transmission, Unbalanced

5.4.3 Balanced Operating Modes

In the balanced operating modes, in addition to pixel and control information an additional bit is transmitted on every signal line during each cycle. This bit is the DC Balance bit (DCBAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the pixel data either unmodified or inverted.

The value of the DC Balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word shall be calculated by subtracting the number of bits of value 0 from the number of bits of value 1 in the current word. Initially, the running word disparity may be any value between +10 and -9. The running word disparity shall be calculated as a continuous sum of all of the modified data disparity values, where the modified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity shall saturate at +10 and –9.

The value of the DC Balance bit shall be 0 when the data is sent unmodified and 1 when the data is sent inverted. To determine whether to send pixel data unmodified or inverted, the running word disparity and the current data disparity are used. If the running word disparity is positive

and the current data disparity is positive, the pixel data shall be sent inverted. If the running word disparity is positive and the current data disparity is zero or negative, the pixel data shall be sent unmodified. If the running word disparity is negative and the current data disparity is positive, the pixel data shall be sent unmodified. If the running word disparity is negative and the current data disparity is zero or negative, the pixel data shall be sent inverted. If the running word disparity is zero, the pixel data shall be sent inverted.

The control information, such as HSYNC and VSYNC, is always sent unmodified. The value of the control word to send is determined by the running word disparity and the value of the control to be sent. If the running word disparity is positive and the value of the control to be sent is zero, the control word sent shall be 111000. If the running word disparity is zero or negative and the value of the control to be sent is zero, the control word sent shall be 111100. If the running word disparity is positive and the value of the control to be sent is one, the control word sent shall be 110000. If the running word disparity is zero or negative and the value of the control to be sent is one, the control word sent shall be 111110. The DC Balance bit shall be sent as 0 when sending control information.

The data enable control signal (DE) is a special case in the balanced mode of operation. The DE signal delineates between pixel data being sent from the display source to the display device and control information being sent. Thus, it must be continuously available to the OpenLDI receiver at the display device in order to correctly separate pixel data from control information. For this reason, DE shall be sent on the clock signals, CLK1 and CLK2, when operating in the balanced modes. The value of the control word sent on the clock signals shall be chosen based on the running word disparity and whether the signal is representing the clock or the data enable control signal. If CLK1 and CLK2 signals are carrying the clock information, the value of the data word sent on the CLK1 and CLK2 lines shall be 000001. If the CLK1 and CLK2 signals are carrying the data enable control signal, the value of the data word sent shall be determined as follows. If the running word disparity is positive and the value of the control to be sent is zero, the control word sent shall be 111110. If the running word disparity is zero or negative and the value of the control to be sent is zero, the control word sent shall be 110000. . If the running word disparity is positive and the value of the control to be sent is one, the control word sent shall be 111100. If the running word disparity is zero or negative and the value of the control to be sent is one, the control word sent shall be 111000.

5.4.3.1 18-bit Single Pixel Mode, Balanced

In the 18-bit single pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-6. Outputs A3 through A7 and CLK2 shall be inactive in this mode and fixed at a single value.

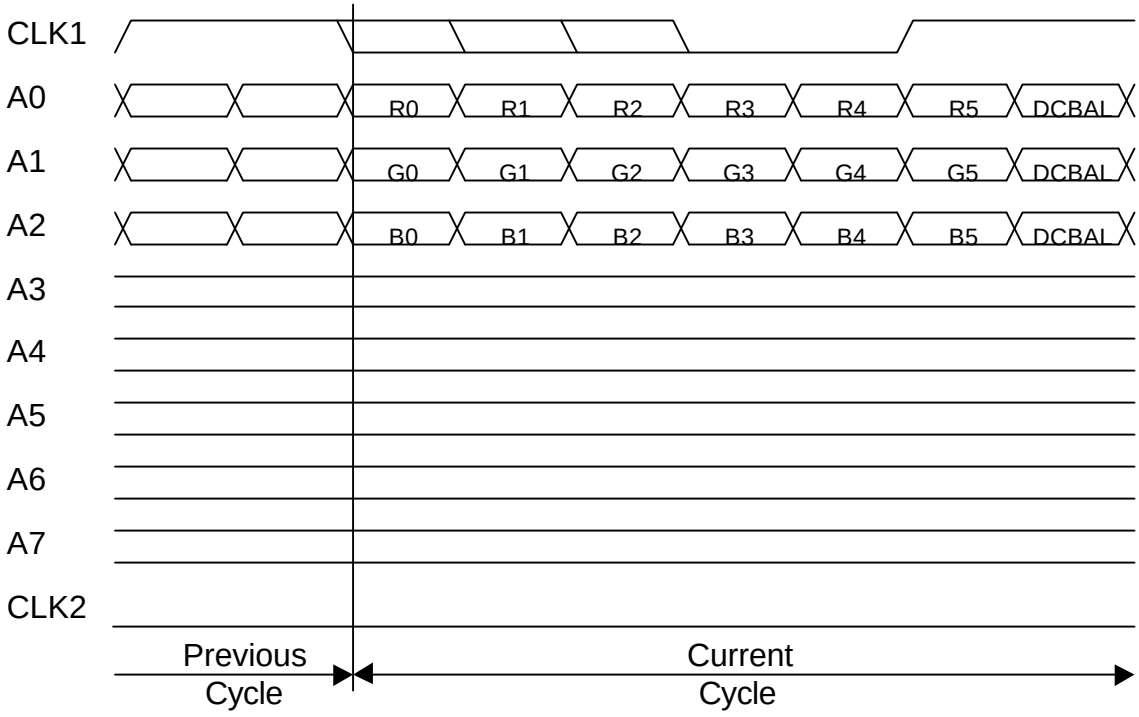


Figure 5-6, 18-bit Single Pixel Transmission, Balanced

The control inputs shall be transmitted in the blanking interval. The blanking interval shall be determined to be when the Data Enable input is false. This is system dependent and may occur when the DE signal is either high or low. During the blanking interval, the control inputs shall be transmitted as shown in Table 5-3. The data pattern in the table is transmitted leftmost bit first.

Table 5-3, Control Transmission in 18-bit Balanced Single Pixel Mode

Control Signal	Signal Level	Output Signal	Data Pattern
DE	High	CLK1 and CLK2	1111000 or 1110000
	Low		1111100 or 1100000
HSYNC	High	A0	1100000 or 1111100
	Low		1110000 or 1111000
VSYNC	High	A1	1100000 or 1111100
	Low		1110000 or 1111000

5.4.3.2 24-bit Single Pixel Mode, Balanced

In the 24-bit single pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-7. Outputs A4 through A7 and CLK2 shall be inactive in this mode. and fixed at a single value.

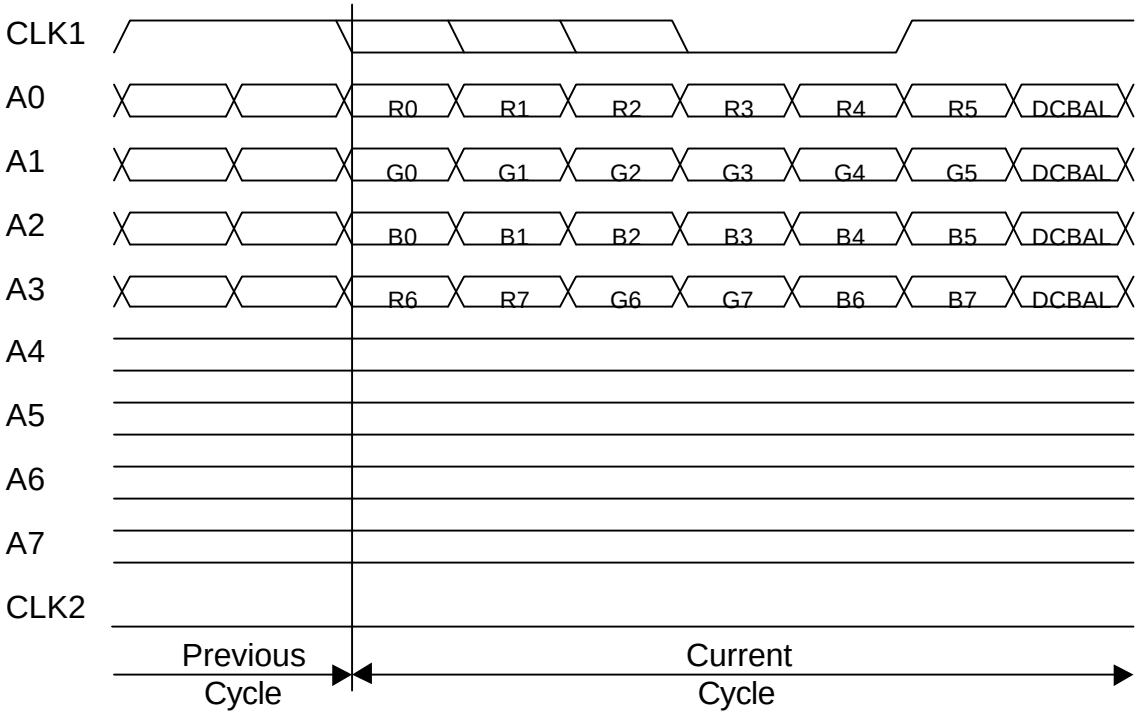


Figure 5-7, 24-bit Single Pixel Transmission, Balanced

The control inputs shall be transmitted in the blanking interval. The blanking interval shall be determined to be when the Data Enable input is false. This is system dependent and may occur when the DE signal is either high or low. During the blanking interval, the control inputs shall be transmitted as shown in Table 5-4. The data pattern in the table is transmitted leftmost bit first.

Table 5-4, Control Transmission in 24-bit Balanced Single Pixel Mode

Control Signal	Signal Level	Output Signal	Data Pattern
DE	High	CLK1 and CLK2	1111000 or 1110000
	Low		1111100 or 1100000
HSYNC	High	A0	1100000 or 1111100
	Low		1110000 or 1111000
VSYNC	High	A1	1100000 or 1111100
	Low		1110000 or 1111000

5.4.3.3 18-bit Dual Pixel Mode, Balanced

In the 18-bit dual pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 5-8. Outputs A3 and A7 shall be inactive in this mode and fixed at a single value.

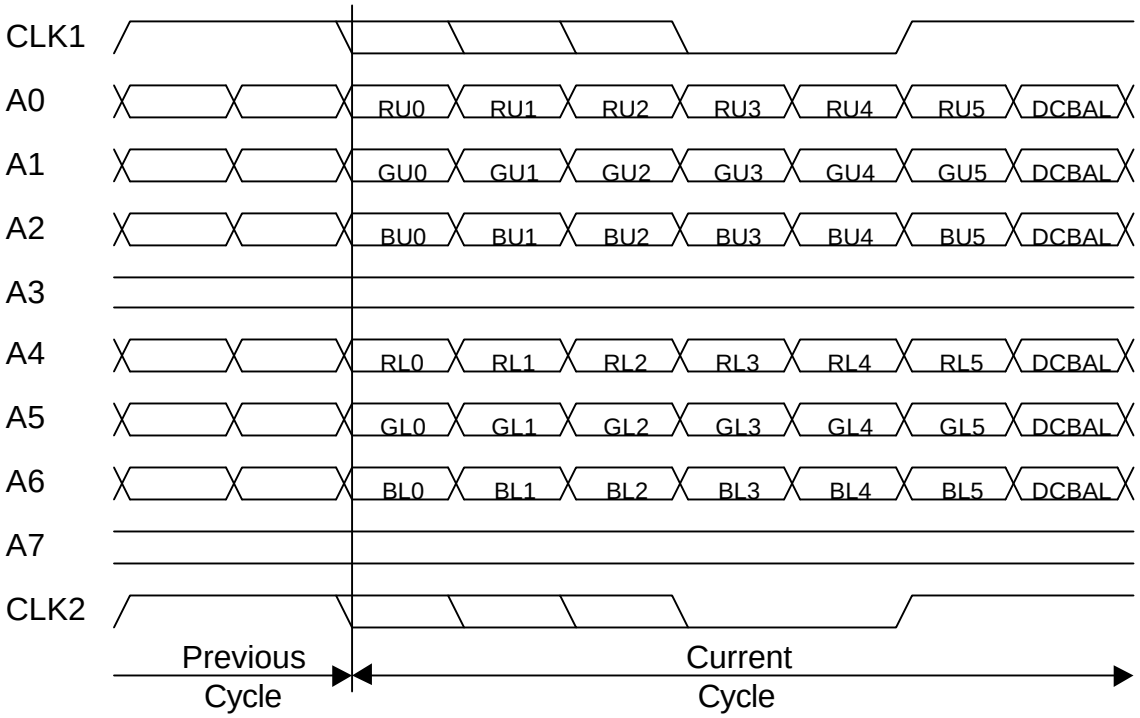


Figure 5-8, 18-bit Dual Pixel Transmission, Balanced

The control inputs shall be transmitted in the blanking interval. The blanking interval shall be determined to be when the Data Enable input is false. This is system dependent and may occur when the DE signal is either high or low. During the blanking interval, the control inputs shall be transmitted as shown in Table 5-5. The data pattern in the table is transmitted leftmost bit first.

Table 5-5, Control Transmission in 18-bit Balanced Dual Pixel Mode

Control Signal	Signal Level	Output Signal	Data Pattern
DE	High	CLK1 and CLK2	1111000 or 1110000
	Low		1111100 or 1100000
HSYNC	High	A0	1100000 or 1111100
	Low		1110000 or 1111000
VSYNC	High	A1	1100000 or 1111100
	Low		1110000 or 1111000
CNTLE	High	A5	1100000 or 1111100
	Low		1110000 or 1111000
CNTLF	High	A4	1100000 or 1111100
	Low		1110000 or 1111000

5.4.3.4 24-bit Dual Pixel Mode, Balanced

In the 24-bit dual pixel mode, the RGB inputs shall be transmitted as shown in Figure 5-9.

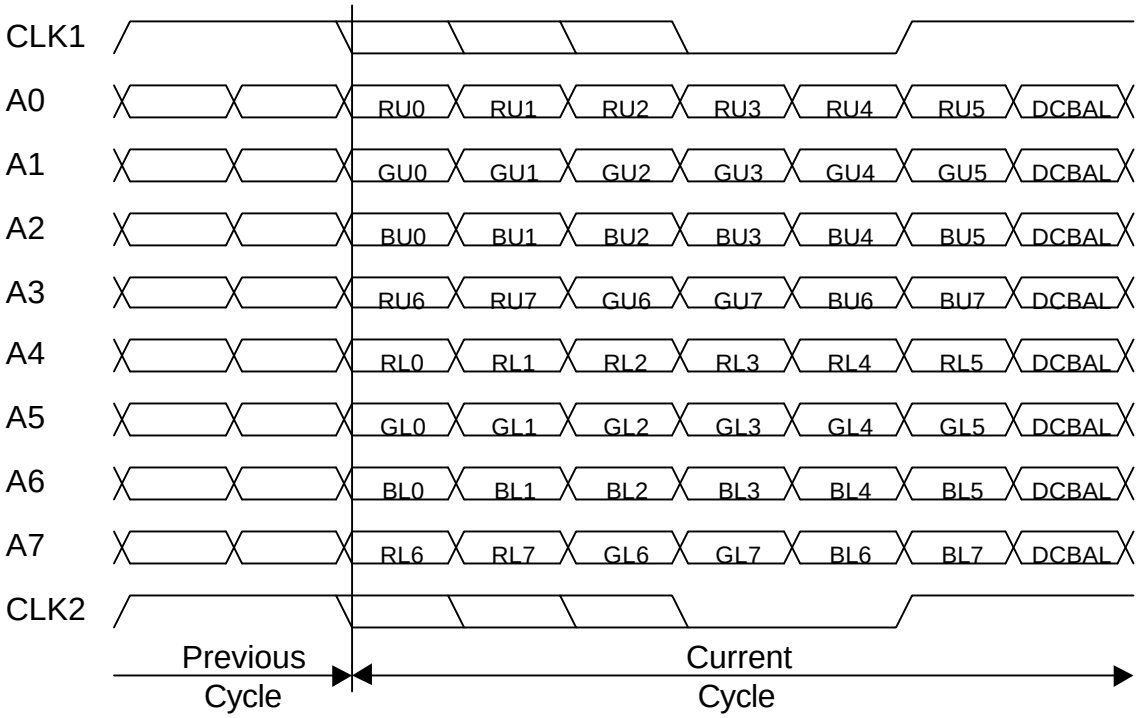


Figure 5-9, 24-bit Dual Pixel Transmission, Balanced

The control inputs shall be transmitted in the blanking interval. The blanking interval shall be determined to be when the Data Enable input is false. This is system dependent and may occur when the DE signal is either high or low. During the blanking interval, the control inputs shall be transmitted as shown in Table 5-6. The data pattern in the table is transmitted leftmost bit first.

Table 5-6, Control Transmission in 24-bit Balanced Dual Pixel Mode

Control Signal	Signal Level	Output Signal	Data Pattern
DE	High	CLK1 and CLK2	1111000 or 1110000
	Low		1111100 or 1100000
HSYNC	High	A0	1100000 or 1111100
	Low		1110000 or 1111000
VSYNC	High	A1	1100000 or 1111100
	Low		1110000 or 1111000
CNTLE	High	A5	1100000 or 1111100
	Low		1110000 or 1111000
CNTLF	High	A4	1100000 or 1111100
	Low		1110000 or 1111000

6 Electrical Interface

6.1 Overview

The OpenLDI interface provides for the transmission of digital pixel information, communication of display device characteristics, and delivery of the USB interface. This section describes the electrical requirements of these three sub-interfaces.

6.2 LVDS Interface

6.2.1 ANSI/EIA/TIA-644

The signal lines used for LVDS signaling (A0P-A7P, A0M-A7M, CLK1P, CLK1M, CLK2P, CLK2M) shall meet the requirements of ANSI/EIA/TIA-644.

6.2.1.1 Bit Times

The OpenLDI LVDS signal lines shall support a minimum bit time of 893 ps. This corresponds to a pixel clock rate of 160 MHz.

6.2.2 Additional Pre-emphasis

In order to achieve reliable communication when using longer cables, pre-emphasis may be applied to the LVDS signal lines. When used, pre-emphasis shall be applied at the transmitter as shown in Figure 6-1. The figure depicts a signal template. A signal with pre-emphasis applied shall be within the boundaries of the template.

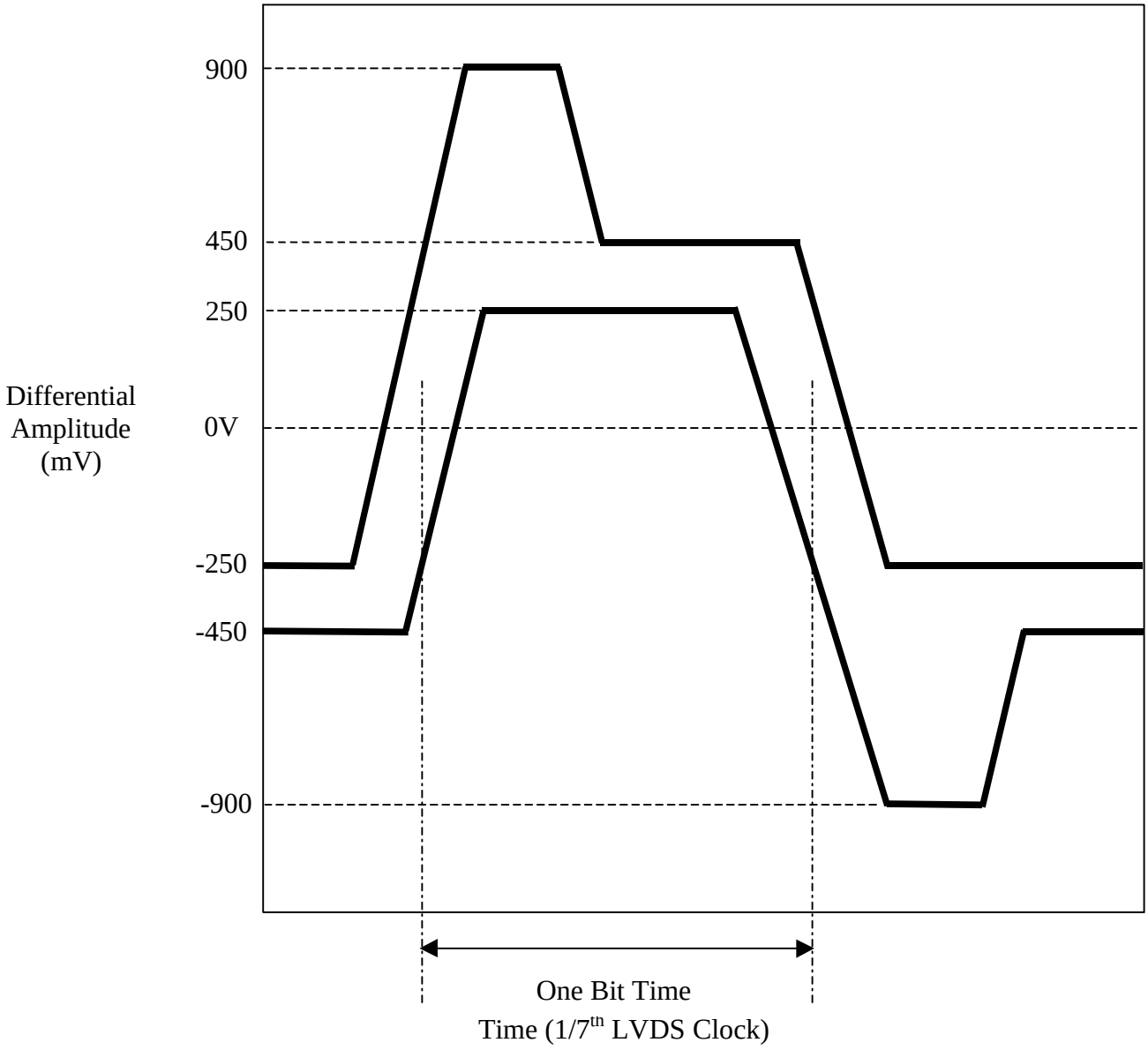


Figure 6-1, Pre-emphasis Template

6.2.3 Intra-pair Skew Tolerance

The OpenLDI receiver shall be able to tolerate a minimum of 300ps skew between the signals arriving on a single differential pair.

6.2.4 Inter-pair Skew Tolerance

The OpenLDI receiver shall be able to tolerate a minimum of 1 bit time skew between signals arriving on independent differential pairs.

6.3 USB Interface

The signal lines used for USB (USB+, USB-, +5VDC USB PWR, USB PWR GND) shall meet the requirements of the Universal Serial Bus Specification, Version 1.0, January 15, 1996.

6.4 DDC Interface

The signal lines used for DDC (DDC/SCL, DDC/SDA, +5VDC DDC PWR, DDCPWR GND) shall meet the requirements of the VESA Display Data Channel Command Interface (DDC/CI) Standard, Version 1, August 14, 1998.

7 Mechanical Interface

7.1 Overview

This section describes the OpenLDI receptacle connector and cable interface required on the display source and display device. General dimensions, tolerances and description of those features which affect the intermateability of the receptacle and plug connectors are described in this section. The panel cutout and pinouts for the receptacle connector are also described in this section.

The OpenLDI interface may be implemented with either shielded or unshielded twisted pair cabling. The connection of both types of cabling is shown in the figures later in this section.

7.2 OpenLDI Connector

The OpenLDI connector shall be a two row shielded ribbon contact connector with contacts on .050" spacing. A 360° "delta" shaped metal shell shall enclose the plug and receptacle contacts to provide shielding and proper polarity when mated. The contacts are designed to handle power, ground and digital signals. The connector receptacle shall be the equivalent of the part numbers listed in Table 7-1.

Table 7-1, Part Numbers for OpenLDI Connector Receptacles

Manufacturer	Part Number
3M	
AMP	

Equivalent compatible connector plugs are listed in Table 7-3.

Table 7-3, Part Numbers for OpenLDI Connector Receptacles

Manufacturer	Part Number
3M	
AMP	

The OpenLDI connector may be omitted when the OpenLDI is an interface internal to an assembly and not accessible externally.

7.2.1 Pin Assignment – Shielded Twisted Pair

The assignment of signals to the connector pins shall be as shown in Figure 7-1. There is no difference between the display source end of the cable and that of the display device. Thus, either end of the cable may be connected to the display source or display device.

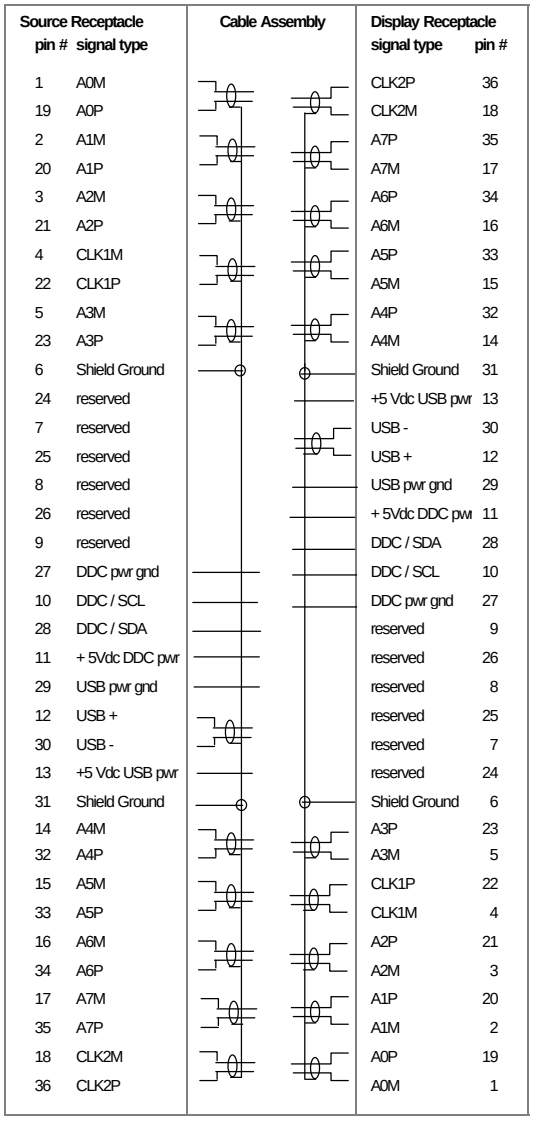


Figure 7-1, Pin Assignment for Shielded Twisted Pair Cabling

7.2.2 Pin Assignment – Unshielded Twisted Pair

The assignment of signals to the connector pins shall be as shown in Figure 7-2. . There is no difference between the display source end of the cable and that of the display device. Thus, either end of the cable may be connected to the display source or display device.

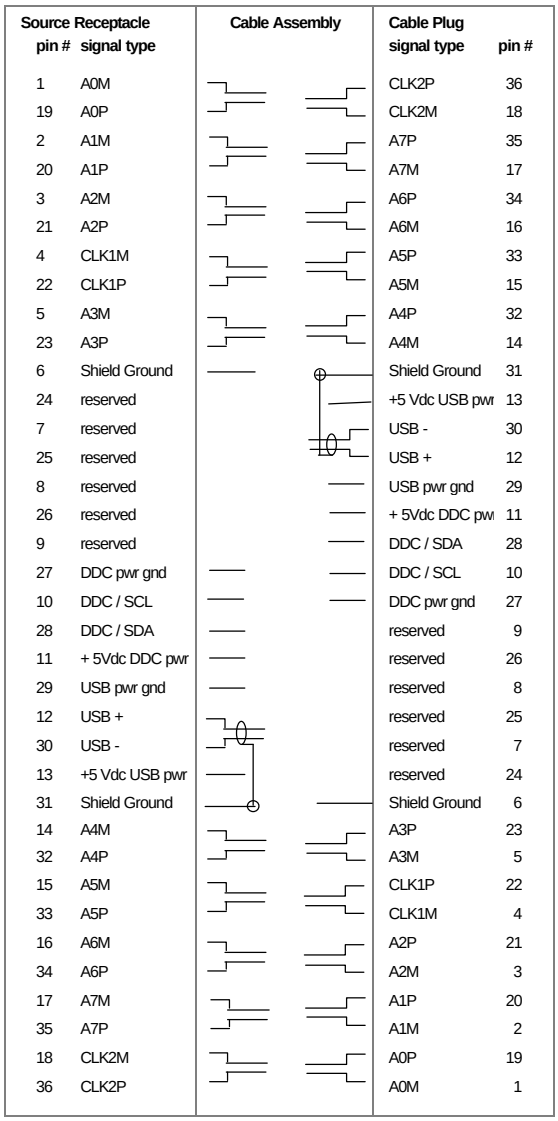


Figure 7-2, Pin Assignment for Unshielded Twisted Pair Cabling

7.2.3 Mechanical Drawings

This section depicts the dimensions and mechanical outline of the connector receptacles on the display source, display device and cable assembly. The connector receptacle on the display source and display device is shown in Figure 7-3. The panel cutout for the display source and display device is shown in Figure 7-3. The cable assembly plug is shown in Figure 7-5. These figures are for illustrative purposes, only. Conformant connectors are those that are equivalent to connectors listed in Table 7-1

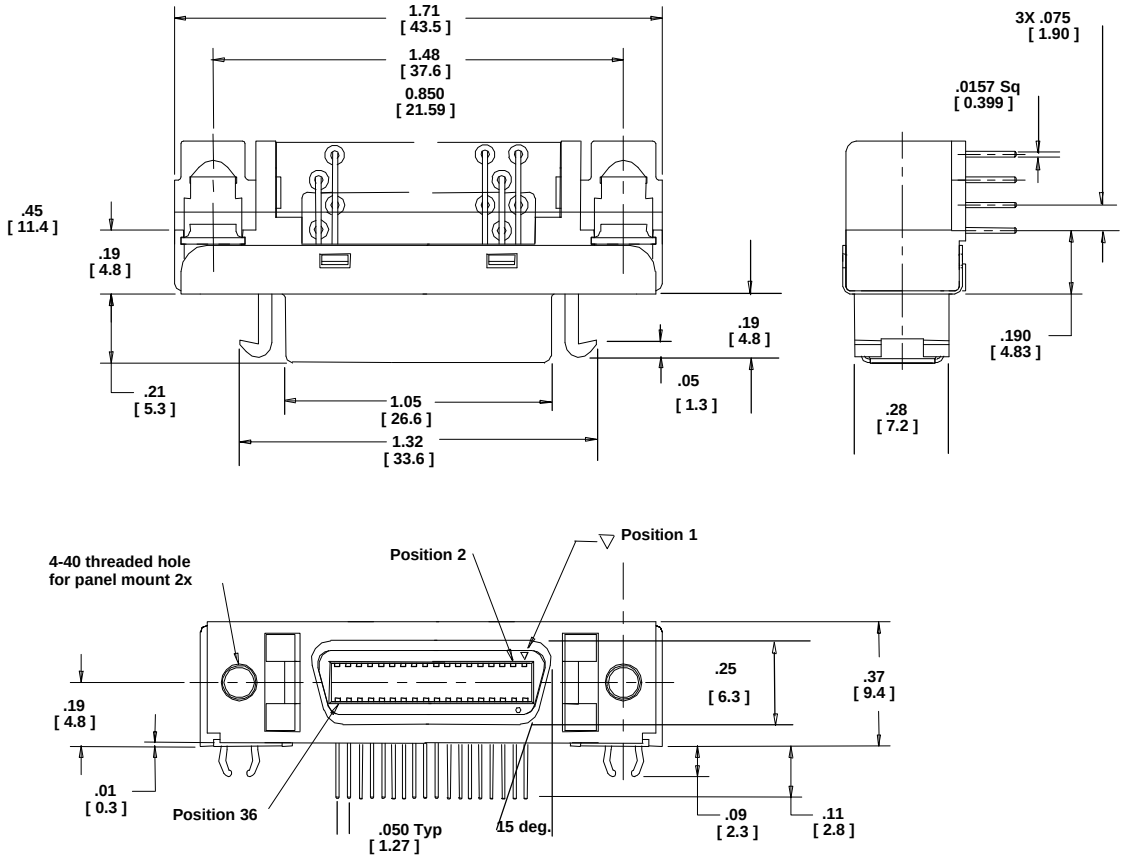
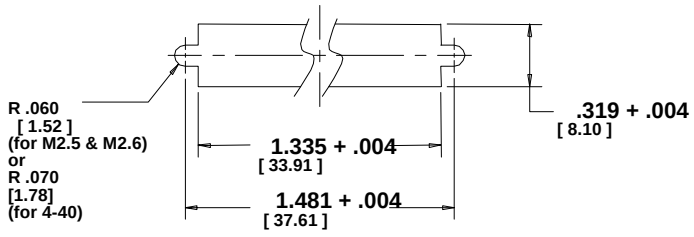


Figure 7-3, Example OpenLDI 36 Position Receptacle Mechanical Drawing



Note: Panel Thickness .079 [2.00]

Figure 7-4, Example Panel Cutout for OpenLDI 36 Position Receptacle

Figure 7-5, Example OpenLDI 36 Position Plug (TBD)

7.2.4 Connector Retention

The receptacle on the display source and the plug on the cable assembly shall be retained by 4-40 screws that ensure the proper mating of the connector reference surfaces. Proper mating is critical to minimizing radiated emissions and electromagnetic interference.

7.2.5 Contact Finish

The contacts of the connector receptacles of the display source and cable assembly shall be plated with a noble metal or noble metal alloy that meets the following minimum requirements 0.76μm gold over 1.26μm nickel, or 0.25μm gold over 0.76μm palladium-nickel alloy.

7.2.6 Shell Finish

The connector shell shall be plated with a minimum of 3.03μm tin or tin alloy.

7.3 OpenLDI Cabling

An OpenLDI cable assembly shall consist of a cable meeting the requirements of this section with an OpenLDI plug on each end or an OpenLDI plug on one end and the other end permanently affixed to the display device. Acceptable cables for OpenLDI may use either shielded or unshielded twisted pairs. It is up to the manufacturer of the OpenLDI equipment to use the grade and type of cable required to meet applicable regulatory requirements. Adherence to this standard does not guarantee regulatory compliance.

When the OpenLDI is an interface internal to an assembly and not accessible externally, the OpenLDI cable may be replaced with any cable or connection means appropriate to the requirements of the assembly.

7.3.1 Cable Length

The maximum cable length shall be 10m.

7.3.2 Number of Signal Conductors

The OpenLDI cable shall comprise 11 twisted pairs and 10 individual conductors.

7.3.3 Wire Gauge

Each conductor in an OpenLDI cable shall be no less than 28AWG.

7.3.4 Conductor Resistance

The resistance of a single conductor of an OpenLDI cable shall not exceed 4Ω when the conductor is of the maximum length specified in this standard.

7.3.5 Insulation

Each conductor in the cable shall be separately insulated. The minimum insulation resistance shall be 1GΩ.

7.3.6 Shield Requirement

The OpenLDI cable shall be encompassed by a single shield, surrounding all conductors in the cable. The shield shall provide a minimum of 90% coverage.

For shielded twisted pair cable, each twisted pair shall be shielded individually. Each shield shall provide a minimum of 90% coverage.

7.3.7 Single Twisted Pair Transmission Skew (Intra-pair Skew)

The differential time of transmission (single pair transmission skew) of a pulse through a single differential pair in an OpenLDI cable shall not exceed ±150ps.

7.3.8 Multiple Twisted Pair Transmission Skew (Inter-pair Skew)

The differential time of transmission (pair to pair transmission skew) of a pulse through any two differential pairs in an OpenLDI cable shall not exceed ±1 bit time.

7.3.9 USB Cable Requirements

The conductors used for transmission of USB signals on the OpenLDI cable shall meet the requirements stated in the Universal Serial Bus Specification, Version 1.0, January 15, 1996.

7.3.10 DDC Cable Requirements

The conductors used for transmission of DDC signals on the OpenLDI cable shall meet the requirements stated in the VESA Display Data Channel Command Interface (DDC/CI) Standard, Version 1, August 14, 1998.

8 Testing Requirements

The performance and testing requirements for the OpenLDI connector plug and receptacle are described in this section. Test procedures and requirements from ANSI/EIA/TIA 364 are used, where applicable.

8.1 Environmental Requirements

8.1.1 Temperature Life

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-17, Condition 4 at 105°C for 250 hours, using method A while connectors are mated.

8.1.2 Cyclic Humidity

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-31, Conditions A and C, Method III omitting 7A and 7B. Contact resistance shall be measured according to ANSI/EIA/TIA 364-23. Contact resistance shall not exceed 15mΩ. Contact resistance shall not change more than 10mΩ from the original resistance measured.

8.1.3 Thermal Shock

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-32, Condition 1 for 10 cycles mated and unmated. Contact resistance shall be measured according to ANSI/EIA/TIA 364-23. Contact resistance shall not exceed 15mΩ. Contact resistance shall not change more than 10mΩ from the original resistance measured.

8.1.4 Corrosion Resistance

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-65, Environmental Class II with the sample located in zone 14.

8.2 Electrical Requirements

8.2.1 Dielectric Withstanding Voltage

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-20, using a test voltage of 500VDC with the connector unmated and unmounted, at a barometric pressure of 15psi.

8.2.2 Insulation Resistance

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-21, using Method C with a test voltage of 500VDC and the connector unmated and unmounted. Minimum insulation resistance shall be 1GΩ between adjacent contacts and between each contact and the connector shell.

8.2.3 Contact Resistance

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-23 The resistance shall be no more than 15mΩ per mated contact pair. Throughout all tests there shall be no more than 10mΩ change from the original resistance measured.

8.2.4 Shell to Shell and Shell to Bulkhead Resistance

The connector and plug shall be tested with the connectors mated and mounted to a bulkhead. The resistance from shell to shell and from shell to bulkhead shall be no more than 50mΩ.

8.2.5 Impedance of Digital Signal Lines

The connector, plug and cable shall be tested according to ANSI/EIA/TIA 364-67, using the time domain reflectometry method normalized to 1ns rise time, with single-ended 1:1 S:G ratio. The impedance of each line shall be 65Ω) 10Ω.

8.2.6 Impedance of LVDS and USB Differential Signal Lines

The connector, plug and cable shall be tested according to ANSI/EIA/TIA 364-67, using the time domain reflectometry method normalized to 500ps rise time, with single-ended 1:1 S:G ratio. The impedance of the source and the impedance of the load shall be 100Ω. Only the shell shall be grounded. The impedance of each differential pair shall be 100Ω) 10Ω.

8.2.7 Contact Current Rating

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-70, using TP-70 and a minimum current of 1.0A at an ambient temperature no more than 55°C. The contact temperature shall not increase more than 85°C.

8.2.8 Bandwidth of Digital Signal Lines

Bandwidth testing of the digital signal lines is a subject of ongoing investigation. This is a topic for future standardization.

8.2.9 Bandwidth of LVDS and USB Differential Signal Lines

Bandwidth testing of the LVDS and USB differential signal lines is a subject of ongoing investigation. This is a topic for future standardization.

8.2.10 Crosstalk of LVDS and USB Differential Signal Lines

The connector, plug and cable shall be tested according to ANSI/EIA/TIA 364-90, using a 1V signal with 500ps rise time. Both the near end crosstalk (NEXT) and far end crosstalk (FEXT) shall be measured, with only the shield grounded. The measured crosstalk shall not exceed 5%.

8.3 Mechanical Requirements

8.3.1 Durability

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-09, two mated pairs for 500 cycles.

8.3.2 Mating and Unmating Force

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-13, inserted and extracted at 25mm per minute. The mating force shall not exceed 4kgf nor be less than 2kgf.

8.3.3 Mechanical Shock

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-27, Condition G. Continuity shall be measured according to ANSI/EIA/TIA 364-46 for all contacts. No discontinuities shall be longer than 1μs.

8.3.4 Vibration

The connector plug and receptacle shall be tested according to ANSI/EIA/TIA 364-28, Condition 3. Continuity shall be measured according to ANSI/EIA/TIA 364-46 for all contacts. No discontinuities shall be longer than 1μs.

9 Conformance Statement Proforma†

9.1 Introduction

The supplier of an implementation that is claimed to conform to this standard shall complete the following Conformance Statement proforma.

A completed conformance statement proforma is the conformance statement for the implementation in question. The conformance statement is a statement of which capabilities and options of the standard have been implemented. The conformance statement can have a number of uses, including use

a) By the implementer, as a checklist to reduce the risk of failure to conform to the standard through oversight
b) By the supplier and acquirer, or potential acquirer, of the implementation, as a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard conformance statement proforma
c) By the user, or potential user, of the implementation, as a basis for initially checking the possibility of interworking with another implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible conformance statement proformas)
d) By a tester, as the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation.

9.2 Abbreviations and Special Symbols

9.2.1 Status Symbols

M mandatory
O optional
O.<n> optional, but support of at least one of the group of options labeled by the same numeral <n> is required

pred: conditional symbol, including predicate identification

9.2.2 General Abbreviations

IUT implementation under test
N/A not applicable

† Copyright release for conformance statement proforma: Users of this standard may freely reproduce the conformance statement proforma in this section so that it can be used for its intended purpose and may further publish the completed conformance statement.

9.3 Instructions for Completing the Conformance Statement Proforma

9.3.1 General Structure of the Conformance Statement Proforma

The first part of the conformance statement proforma, Implementation Identification and Conformance Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the conformance statement proforma is a fixed questionnaire, divided into parts, each containing a number of individual items. Answers to the questionnaire items are to be provided in the rightmost column, by simply marking an answer to indicate a choice.

Each item is identified by an item reference in the first column. The second column contains the question to be answered. The third column contains the reference or references to the material that specifies the item in the main body of this standard. The remaining columns record the status of each item, i.e., whether support is mandatory, optional, or conditional, and provide the space for the answers. Marking an item as supported is to be interpreted as a statement that all relevant requirements, cited in the References column for the item, are met by the implementation.

A supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<*I*> or X<*I*>, respectively, for cross-referencing purposes, where <*I*> is any unambiguous identification for the item (e.g., simply a numeral). There are no other restrictions on its format or presentation.

A completed conformance statement proforma, including any Additional Information and Exception Information, is the Conformance Statement for the implementation in question.

Note – Where an implementation is capable of being configured in more than one way, a single conformance statement may be able to describe all such configurations. However, the supplier has the choice of providing more than one conformance statement, each covering some subset of the implementation's capabilities, if this makes for easier and clearer presentation of the information.

9.3.2 Additional Information

Items of Additional Information allow a supplier to provide further information intended to assist in the interpretation of the conformance statement. It is not intended or expected that a large quantity of information will be supplied, and a conformance statement can be considered complete without any such information. Examples of such Additional Information might be an outline of the ways in which an (single) implementation can be set up to operate in a variety of environments and configurations, or information about aspects of the implementation that are outside the scope of this standard but have a bearing upon the answers to some items.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

9.3.3 Exception Information

It may happen occasionally that a supplier will wish to answer an item with mandatory status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No pre-printed answer will be found in the Support column for this. Instead, the supplier shall write the missing answer into the Support column, together with an X<*I*> reference to an item of Exception Information, and shall provide the appropriate rationale in the Exception Information item itself.

An implementation for which an Exception Information item is required in this way does not conform to this standard.

Note – A possible reason for the situation described above is that a defect in this standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

9.3.4 Conditional Status

The conformance statement proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply, mandatory or optional, are dependent upon whether or not certain other items are supported.

Where a group of items is subject to the same condition for applicability, a separate preliminary question about the condition appears at the head of the group, with an instruction to skip to a later point in the questionnaire if the "Not Applicable" answer is selected. Otherwise, individual conditional items are indicated by a conditional symbol in the Status column.

A conditional symbol is of the form "<pred>:<S>", where "<pred>" is a predicate as described below, and "<S>" is one of the status symbols M or O.

If the value of the predicate is true, the conditional item is applicable, and its status is given by S: the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

A predicate is one of the following:

a) An item-reference for an item in the conformance statement proforma: the value of the predicate is true if the item is marked as supported, and is false otherwise.
b) A boolean expression constructed by combining item-references using the boolean operators. The value of the predicate is true if the boolean equation combining the item references is true (where each individual item reference is true if the item is supported), and is false otherwise.

Each item referenced in a predicate, or in a preliminary question for grouped conditional items, is indicated by an asterisk in the Item column.

9.4 Conformance Statement Proforma—OpenLDI

9.4.1 Implementation Identification

Supplier	
Contact point for queries about the conformance statement	
Implementation Name(s) and Version(s)	
Other information necessary for full identification, e.g., name(s) and version(s) of the machines and/or operating systems(s), system names	

Notes

a) Only the first three items are required for all implementations. Other information may be completed as appropriate in meeting the requirement for full identification.

b) The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model)

9.4.2 Conformance Summary, OpenLDI

Identification of Protocol Standard	OpenLDI
Identification of Amendments and Corrigenda to this conformance statement proforma that have been completed as part of this conformance statement	Amd. : Corr. : Amd. : Corr. :
Have any Exception items been required? (See 9.3.3: the answer Yes means that the implementation does not conform the OpenLDI standard.)	Yes ❑ No ❑

Date of statement (dd/mm/yyyy)	

9.4.3 IUT Configuration

Item	IUT Configuration	References	Status	Support
	What is the configuration of the IUT?			
CF1	Internal interface	7.2, 7.3	O.1	Yes ❑ No ❑
* CF2	External interface	7.2, 7.3	O.1	Yes ❑ No ❑
* CF3	Display Source	4	O.1	Yes ❑ No ❑
* CF4	Display Device	4	O.1	Yes ❑ No ❑
* CF5	Fixed Resolution Display Device	4	O.1	Yes ❑ No ❑

Item	Default Configurations	References	Status	Support
	Is the default configuration supported?			
D1	640×480, 60 Hz, 24 bpp, single pixel mode, lower pixel active	5.2.1.1	CF3:M	Yes ❑ No ❑ N/A ❑
D2	640×480, 60 Hz, 18 bpp, single pixel mode, lower pixel active	5.2.1.2	CF4:M	Yes ❑ No ❑ N/A ❑
D3	640×480, 60 Hz, 24 bpp, single pixel mode, lower pixel active	5.2.1.2	CF4:O	Yes ❑ No ❑ N/A ❑
D4	Are all Signal lines terminated properly?	5.2.1.2	CF4:M	Yes ❑ No ❑ N/A ❑
D5	Does the device respond to DDC2B protocol immediately after application of power or connection of the OpenLDI interface?	5.2.1.2	CF4:M	Yes ❑ No ❑ N/A ❑
D6	Does the device blank the display and enter a low power mode of operation when the OpenLDI interface is not connected?	5.2.1.2	CF4:O	Yes ❑ No ❑ N/A ❑

Item	Plug and Play Operation	References	Status	Support
	Is the plug and play operation supported?			
P1	Is a display device attach hot plug event detected?	5.2.2.1	CF3:M	Yes ❑ No ❑ N/A ❑
P2	Is a display device removal hot plug event detected?	5.2.2.2	CF3:M	Yes ❑ No ❑ N/A ❑
P3	Is a display source attach hot plug event detected?	5.2.2.3	CF4:M	Yes ❑ No ❑ N/A ❑
P4	Does the display device operate in its default configuration after a display source attach hot plug event?	5.2.2.3	CF4:M	Yes ❑ No ❑ N/A ❑
P5	Is a display source removal hot plug event detected?	5.2.2.4	CF4:M	Yes ❑ No ❑ N/A ❑
P6	Does the display device begin a standby mode of operation after the detection of a display source removal hot plug event?	5.2.2.4	CF4:O	Yes ❑ No ❑ N/A ❑
P7	Is DDC2B supported?	5.2.3	M	Yes ❑ No ❑
P8	Does the display source supply a minimum of 100 mA to the +5 VDC DDC Power line?	5.2.3	CF3:M	Yes ❑ No ❑ N/A ❑
P9	Does the display source support both EDID 1.3 and 2.0?	5.2.4	CF3:M	Yes ❑ No ❑ N/A ❑
P10	Does the display device support EDID 1.3?	5.2.4	CF4:O.2	Yes ❑ No ❑ N/A ❑
P11	Does the display device support EDID 2.0?	5.2.4	CF4:O.2	Yes ❑ No ❑ N/A ❑
P12	Is the Preferred Timing Mode bit set and the native resolution reported in the first detailed timing field of the	5.2.4	CF5:M	Yes ❑ No ❑ N/A ❑

Item	Plug and Play Operation	References	Status	Support
	EDID data structure?			
P13	Display source gamma correction	5.2.5.1	CF3:M	Yes ❑ No ❑ N/A ❑
P14	Display device gamma correction	5.2.5.2	CF4:M	Yes ❑ No ❑ N/A ❑

Item	Transmission Modes Supported	References	Status	Support
	What pixel transmission modes are supported?			
X1	18-bit single pixel, unbalanced	5.4.2.1, 5.3.1	M	Yes ❑ No ❑
X2	24-bit single pixel, unbalanced	5.4.2.2, 5.3.2	M	Yes ❑ No ❑
X3	18-bit dual pixel, unbalanced	5.4.2.3, 5.3.3	O	Yes ❑ No ❑ N/A ❑
X4	24-bit dual pixel, unbalanced	5.4.2.4, 5.3.4	O	Yes ❑ No ❑ N/A ❑
* X5	18-bit single pixel, balanced	5.4.3.1, 5.3.1	O	Yes ❑ No ❑ N/A ❑
* X6	24-bit single pixel, balanced	5.4.3.2, 5.3.2	O	Yes ❑ No ❑ N/A ❑
* X7	18-bit dual pixel, balanced	5.4.3.3, 5.3.3	O	Yes ❑ No ❑ N/A ❑
* X8	24-bit dual pixel, balanced	5.4.3.4, 5.3.4	O	Yes ❑ No ❑ N/A ❑
	How is the balanced transmission mode implemented?			
X9	Data disparity calculation	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X10	Running word disparity calculation	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X11	Running word disparity saturation	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X12	DC Balance bit value	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X13	Transmit unmodified or inverted	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X14	Control information transmission	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X15	Data Enable sent on CLK1	5.4.3	X5 or X6 or X7 or X8:M	Yes ❑ No ❑ N/A ❑
X16	Data Enable sent on CLK2	5.4.3	X7 or X8:M	Yes ❑ No ❑ N/A ❑

Item	Electrical Interface	References	Status	Support
	Which electrical interfaces are supported?			
E1	LVDS	6.2.1	M	Yes ❑ No ❑
E2	Minimum bit time	6.2.1.1	M	Yes ❑ No ❑
E3	LVDS with pre-emphasis	6.2.2	O	Yes ❑ No ❑ N/A ❑
* E4	USB	6.3	O	Yes ❑ No ❑ N/A ❑
E5	DDC	6.4	M	Yes ❑ No ❑

Item	Receptacle	References	Status	Support
R1	Is the receptacle compatible with those listed?	7.2	M	Yes ❑ No ❑
R2	Is the shielded twisted pair pinout as described?	7.2.1	M	Yes ❑ No ❑
R3	Is the unshielded twisted pair pinout as described?	7.2.2	O	Yes ❑ No ❑ N/A ❑

Item	Cable	References	Status	Support
	Is the interface accessible external to the assembly?			
C1	Cable length ≤ 10m	7.3.1	CF2:M	Yes ❑ No ❑ N/A ❑
C2	Number of conductors and types	7.3.2	CF2:M	Yes ❑ No ❑ N/A ❑
C3	Wire gauge	7.3.3	CF2:M	Yes ❑ No ❑ N/A ❑
C4	Conductor resistance	7.3.4	CF2:M	Yes ❑ No ❑ N/A ❑
C5	Insulation resistance	7.3.5	CF2:M	Yes ❑ No ❑ N/A ❑
C6	Cable shield	7.3.6	CF2:M	Yes ❑ No ❑ N/A ❑
C7	Single pair transmission skew	7.3.7	CF2:M	Yes ❑ No ❑ N/A ❑
C8	Multiple pair transmission skew	7.3.8	CF2:M	Yes ❑ No ❑ N/A ❑

Item	Cable	References	Status	Support
C9	Meets USB requirements	7.3.9	CF2 and E4:M	Yes ❑ No ❑ N/A ❑
C10	Meets DDC requirements	7.3.10	CF2:M	Yes ❑ No ❑ N/A ❑

Item	Testing	References	Status	Support
T1				Yes ❑ No ❑
T2				Yes ❑ No ❑
T3				Yes ❑ No ❑