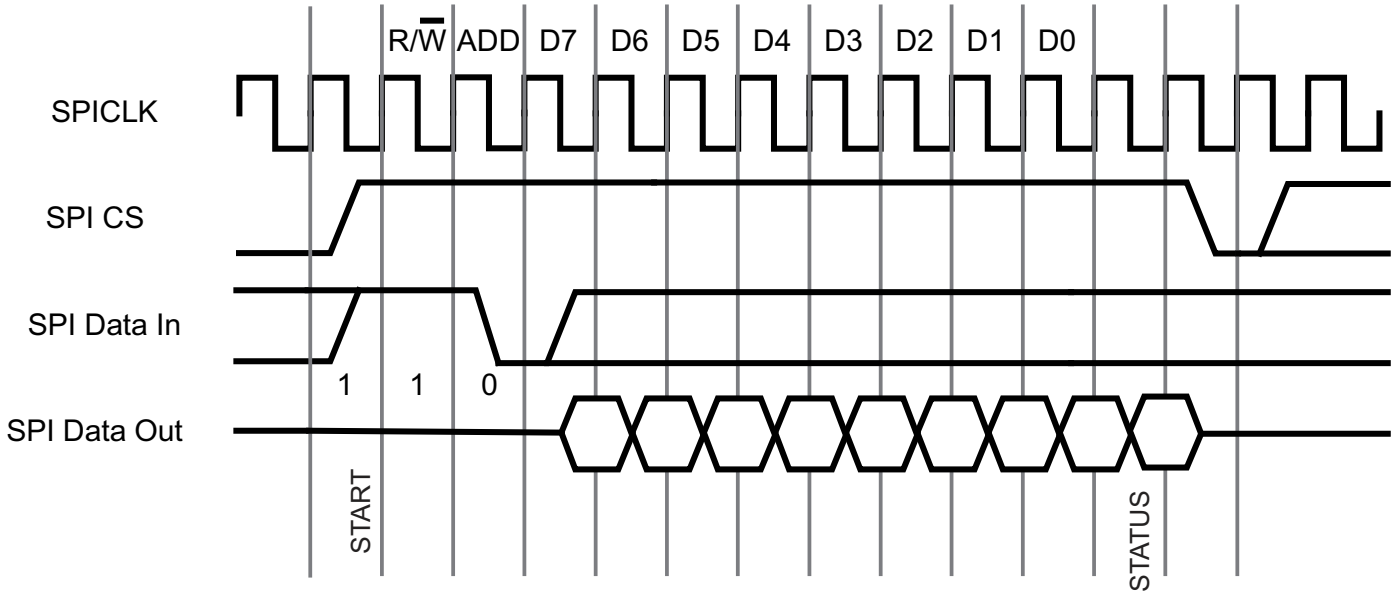
2.5 SPI Interface Signal Descriptions and Timing Diagrams

Table 8 - Data and Control Bus Signal Mode Options - SPI Interface

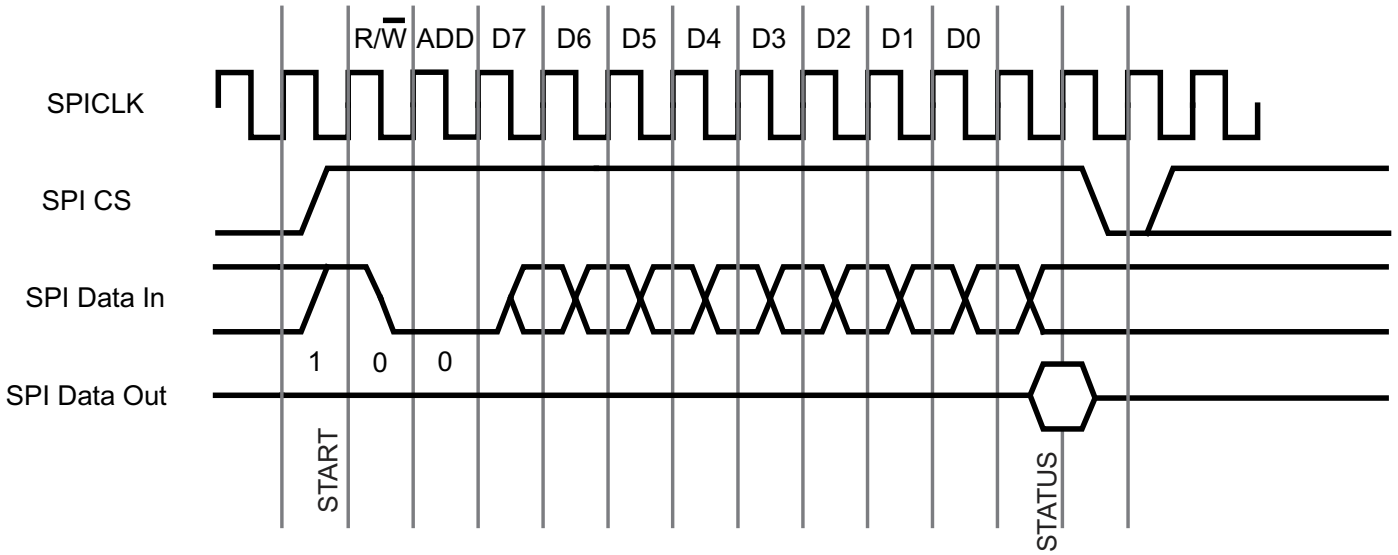
Pin No.	Name	Type	Description
31	SCLK	Input	SPI Clock input, 12MHz maximum.
32	SDI	Input	SPI Serial Data Input
33	SDO	Output	SPI Serial Data Output
34	CS	Input	SPI Chip Select Input

Figure 6 - SPI Slave Data Read Cycle



From Start - SPI CS must be held high for the entire read cycle, and must be taken low for at least one clock period after the read is completed. The first bit on SPI Data In is the R/W bit - inputting a '1' here allows data to be read from the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is read from. During the SPI read cycle a byte of data will start being output on SPI Data Out on the next clock cycle after the address bit, MSB first. After the data has been clocked out of the chip, the status of SPI Data Out should be checked to see if the data read is new data. A '0' level here on SPI Data Out means that the data read is new data. A '1' indicates that the data read is old data, and the read cycle should be repeated to get new data. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 7 - SPI Slave Data Write Cycle



From Start - SPI CS must be held high for the entire write cycle, and must be taken low for at least one clock period after the write is completed. The first bit on SPI Data In is the R/W bit - inputting a '0' here allows data to be written to the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status

register (‘1’) is written to. During the SPI write cycle a byte of data can be input to SPI Data In on the next clock cycle after the address bit, MSB first. After the data has been clocked in to the chip, the status of SPI Data Out should be checked to see if the data read was accepted. A ‘0’ level on SPI Data Out means that the data write was accepted. A ‘1’ indicates that the internal buffer is full, and the write should be repeated. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 8 - SPI Slave Data Timing Diagrams

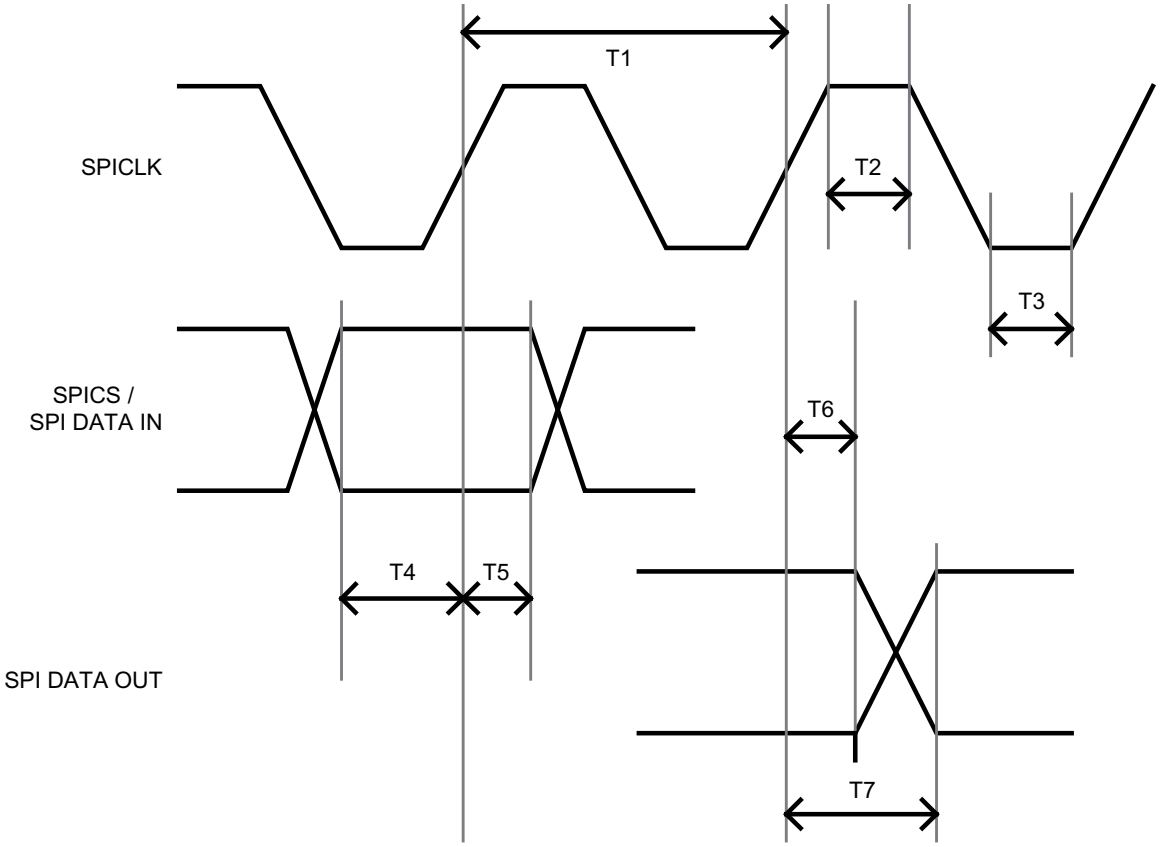


Table 9 - SPI Slave Data Timing

Time	Description	Min	Typical	Max	Unit
T1	SPICLK Period	83	-	-	ns
T2	SPICLK High	20	-	-	ns
T3	SPICLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Hold TIme	10	-	-	ns
T6	Output Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 10 - Status Register (ADD = ‘1’)

Bit	Description
0	RXF#
1	TXE#
2	-
3	-
4	RXF IRQEn
5	TXE IRQEn
6	-
7	-

