1 Second Time Base From Crystal Oscillator

The schematic below illustrates dividing a crystal oscillator signal by the crystal frequency to obtain an accurate (0.01%) 1 second time base. Two cascaded 12 stage counters (CD4040) form a 24 stage binary counter and the appropriate bits are gated together to produce the desired division. Using a crystal of some even multiple of 2 is desirable so that one stage of the counter automatically toggles every second which eliminates the need for the NAND gate and reset circuitry, however the circuit below illustrates using a crystal which is not an even multiple of 2 and so requires additional components.

Using a 50 Khz crystal, a count of 50000 is detected when the appropriate counter bits that add up to 50000 are all high. This corresponds to bits 15 (32768) + 14 (16384) + 9 (512) + 8 (256) + 6 (64) + 4 (16). Bits 14 and 15 are the 3rd and 4th stages of the second counter, bit 0 is the first stage of the first counter (Q1, pin 9). To use a 100 Khz crystal, each bit would be moved one to the right so the total would be (65536 + 32768 + 1024 + 512 + 128 + 32 = 100,000). Using a 1 Mhz crystal, the following bits would be needed:

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Bit 19 - Right counter - Q8 - pin 13  -  Decimal value = 524288
    18                   7        4                    262144
    17                   6        2                    131072
    16                   5        3                     65536
    14                   3        6                     16384
     9 - Left counter  - 10       14                       512
     6                   7        4                        64
                                                     ---------
                                                     1,000,000
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At 1 Mhz, the 330K resistor in the oscillator circuit will need to be reduced proportionally to about 15K. When the terminal count is reached, a 7 uS reset pulse is generated by the Schmitt Trigger inverter stage that follows the NAND gate. The 47K resistor and 470 picofarad capacitor sustain the output so that the counters are reliably reset

to zero. This is less than one clock cycle at 50Khz and does not introduce an error but would amount to 7 cycles at 1 MHz which would cause the counters to lose 7 microseconds of time per second. It's not much of an error (7 parts in a million) but it would be there. The minimum reset pulse width for the 4040 CMOS counters is about 1.5 uS, so the reset pulse cannot be made much shorter.