Why the Propeller Works

by Chip Gracey

One of our customers recently posted this message to the Propeller discussion forum:

> ***"Interesting that someone is brave enough to use a propeller chip in a professional application. This chip doesn't even have a datasheet, and it is very likely that it has never been tested against any of the usual standards for integrated circuits. I would not even think about using it for anything other than hobby projects."***

This concern is quite understandable, given the current lack of documentation. The reality, though, is that the Propeller has received an inordinate amount of attention to its design, and it is quite robust. I will elaborate.

I am the person who designed, debugged, tuned, and tested the Propeller. This project took eight years of my time, plus two years of a layout engineer's time. An excruciating amount of attention went into every aspect of the Propeller's implementation and testing, and I allowed no compromises.

Industry metrics:

As for industry-standard tests, we recently hired a company called Nano Measurements to perform their own environmental and ESD testing on the Propeller. Specifically, the following tests were conducted:

PPOT - Pressure pot, autoclave: 121°C, 100% RH, 15 PSIG, 336 hours
TMCL - Temperature cycle, air, standard ramp: -65°C to 150°C, 500 cycles
PREC - Preconditioning (simulates soldering process): 30°C, 60% RH, 192 hours
HTSL - High temperature storage life: 150°C, 1000 hours
ESD HBM - ESD human body model: All pins tested up to ±8kV (limit of tester)

Here are the results:	(lots of 77 devices ensure 3-sigma quality with one failure)
PPOT - 3 lots of 77 devices (PDIP, LQFP, QFN):	0 failures
TMCL - 2 lots of 77 devices and 1 lot of 76 (all):	0 failures
PREC - 3 lots of 77 devices (PDIP, LQFP, QFN):	0 failures
HTSL - 1 lot of 230 devices (PDIP, LQFP, QFN):	0 failures
ESD HBM - 3 devices each of PDIP, LQFP, QFN:	All I/O pins survived ±8kV zap with VSS and VDD grounded, VSS-to-VDD zap failed at ±3kV or greater

So, there were no environmental failures, and no testable ESD failures on I/O pins, though the power supply pins failed at ±3kV or greater, which is quite acceptable. All these environmental tests say almost nothing about the quality of the chip, but only that the plastic packaging was good. The ESD test starts to give some metric of the silicon quality, but says nothing of what is far more likely to be a problem -- design quality. There are no universal metrics for this, and it can only be understood by actually applying the device.

About design quality:

The Propeller was an entirely "full-custom" effort. Every polygon of the Propeller's mask artwork was made here at Parallax. We designed our own logic, RAMs, ROMs, PLLs, band-gap references, oscillators, and even ESD-hardened I/O pads. All these structures were first fabricated on test chips and then thoroughly evaluated, often resulting in design changes. This yielded an ideal set of known-good blocks, which could be confidently applied to the overall design. Then, the whole chip was fabricated and subsequently tested at many levels. This allowed us to fix any problems resulting from integration and to fine-tune the clocking systems that are key to the Propeller's low power consumption. The final chip, which is the only version we've ever sold, is the third iteration of this whole-chip process and has no known problems.

In order to perform all this testing and tuning, we built up our own lab that gave us the "hands" and "eyes" that we needed to work on our chip. First, we invested in a Micrion FIB (focused ion beam) machine that allowed us to perform microscopic surgery, so that we could check failure hypotheses and make experimental modifications. Think "wire cutters", "soldering iron", and "solder" for the sub-micrometer wiring inside the chip. The other big thing we acquired was a Schlumberger e-beam prober -- essentially a scanning electron microscope which can use its electron beam to measure voltages on those same tiny wires while the chip runs at full-speed. Think "7GHz, non-loading, 10nm-tip, contactless oscilloscope". These machines are almost Star Trek in their technology, and they get you all the way down to where you need to be in order to see and fix problems. We were able to purchase these machines, used, for only 0.5% of what they cost new. The real investment, though, turned out to be the six months it took to get them running, and to learn how to use them. Now, we can even do our own maintenance on them, which is not trivial. All this was a huge adventure, in itself, but invaluable in getting the Propeller's silicon perfected.

The Propeller was given the kind of thorough design treatment that almost no other chips receive today. It used to be that every chip was full-custom, and all of its transistors and wiring were designed by hand, for the point of application. As semiconductor technology shrunk, though, the prevailing design methodology shifted away from this kind of specialization, toward generalization and abstraction, so that designs of greater complexity could be practically realized. The modern design methodology centers around hardware description languages, IP block reuse, and the automated placement and interconnection of potentially billions of gates. The end silicon result is invariably an incomprehensible rat's nest of wiring, standard cells, and IP blocks, usually none of which were designed by the engineers applying them. This methodology is certainly a boon for very complex designs, but it has become the standard approach for designing almost any chip containing logic today. The differences between the old and new methodologies can be accurately characterized by a software analogy: Imagine a program written entirely in assembly language. It takes a long time to write, but it is fast, compact, and reliable by virtue of its directness. Now imagine a program written in some high-level language which leverages objects acquired from elsewhere. It is relatively easy to write, but compiles into something big and slow, and may have some undesirable characteristics that are out of your control. For chips, the old method means small dies, high speed, low power, and exacting performance, whereas the modern method tends to generate bigger dies, lower speed, more heat, and sometimes bugs from IP which you have no control over. I'm sure you get the idea.

Most important:

So, all I've said so far amounts to just this: Through an exceptional effort, we made the Propeller as electrically robust and efficient as we could. This, still, is not the core quality issue, but a supporting one. The core quality of the Propeller really resides in its architecture. The architecture is what took the first six years of development to iron out, and the architecture is what engages people. All the effort that went into the silicon implementation was to insure that this core quality was ideally housed.

The story of the Propeller's architecture would be a book, in itself, but to get an idea of the plot, you can visit the Propeller discussion forum and witness the excitement of people doing things they never thought possible. They are finding the Propeller to be a great vehicle for invention and discovery, as well as the means to realize complex embedded systems that are not possible with any other chip. A few forum members have even said that the Propeller has drawn them back into software and electronics after long absences.

We will publish a datasheet soon with quite a bit of characterization data in it. It should give customers more confidence about using the chip, but for many it will mainly serve to validate what they already know from experience and readily attest to on the forum -- that the Propeller is tough, reliable, and low-power. It's no illusion, and no accident.

We plan on a very long sales life for the Propeller and we have no intention of diluting the concept with many slight variants, for which you'd inevitably be getting end-of-life notices for after a few years. This is good news for customers, because they are the ones who are going to be making investments in programming that will, in sum, dwarf the energy that we spent developing the Propeller. We made a platform that is, hopefully, deserving of their coming efforts.

Sincerely,

Chip Gracey
President
Parallax, Inc.

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