ADDRESS highnib

$0 $2 $4 $6 $8 $f

lownib rambank0

Table 33 - SX48/52 Mode Register

	SX48/52 MODE (m) Register and mov !r?, w					
	m	mov !ra, w	mov !rb, w	mov !rc, w	mov !rd, w	mov !re, w
$0	$00		read T1CPL	read T2PL		
$1	$01		read T1CPH	read T2CPH		
$2	$02		read T1R2CML	read T2R2CML		
$3	$03		read T1R2CMH	read T2R2CMH		
$4	$04		read T1R1CML	read T2R1CML		
$5	$05		read T1R1CMH	read T2R1CMH		
$6	$06		read T1CNTB	read T2CNTB		
$7	$07		read T1CNTA	read T2CNTA		
$8	$08		exchange CMP_B			
$9	$09		exchange WKPND_B			
$a	$0a		write WKED_B			
$b	$0b		write WKEN_B			
$c	$0c		read ST_B	read ST_C	read ST_D	read ST_E
$d	$0d	read LVL_A	read LVL_B	read LVL_C	read LVL_D	read LVL_E
$e	$0e	read PLP_A	read PLP_B	read PLP_C	read PLP_D	read PLP_E
$f	$0f	read TRIS_A	read TRIS_B	read TRIS_C	read TRIS_D	read TRIS_E
$0	$10		clear Timer 1	clear Timer 2		
$1	$11					
$2	$12		write T1R2CML	write T2R2CML		
$3	$13		write T1R2CMH	write T2R2CMH		
$4	$14		write T1R1CML	write T2R1CML		
$5	$15		write T1R1CMH	write T2R1CMH		
$6	$16		write T1CNTB	write T2CNTB		
$7	$17		write T1CNTA	write T2CNTA		
$8	$18		exchange CMP_B			
$9	$19		exchange WKPND_B			
$a	$1a		write WKED_B			
$b	$1b		write WKEN_B			
$c	$1c		write ST_B	write ST_C	write ST_D	write ST_E
$d	$1d	write LVL_A	write LVL_B	write LVL_C	write LVL_D	write LVL_E
$e	$1e	write PLP_A	write PLP_B	write PLP_C	write PLP_D	write PLP_E
$f	$1f	write TRIS_A	write TRIS_B	write TRIS_C	write TRIS_D	write TRIS_E

Abbreviations: T1CPH, T2CPH: Timer 1/2 capture, high byte. T1CPL, T2CPL: Timer 1/2 capture, low byte. T1R1CMH, T2R1CMH: Timer 1/2 register R1, high byte. T1R1CML, T2R1CML: Timer 1/2 register R1, low byte. T1R2CMH, T2R2CMH: Timer 1/2 register R2, high byte. T1R2CML, T2R2CML: Timer 1/2 register R2, low byte.