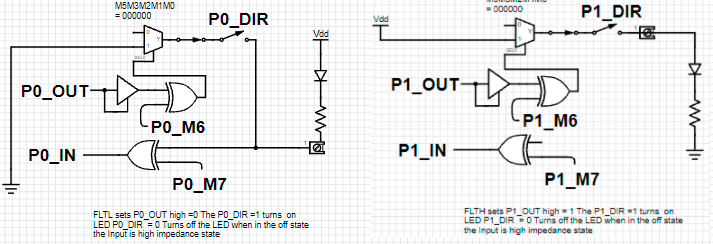
## 17.111) FLTx Out Bits of pins (365..372)

|  |  |
| --- | --- |
| FLTL {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = 0. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTH {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = 1. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTC {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = C. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTNC {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = !C. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTZ {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = Z. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTNZ {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = !Z. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTRND {#}D {WCZ} | OUT bits of pins D[10:6]+D[5:0]..D[5:0] = RNDs. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |
| FLTNOT {#}D {WCZ} | Toggle OUT bits of pins D[10:6]+D[5:0]..D[5:0]. DIR bits = 0. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. |



FLTL Float Low Source Load Sink Pin FLTH Float High Sink Load Source Pin

**Note:** Default Mode setting M7M6M5M4M3M2M1M0 =0000\_0000 M6 can invert the action Of OUTx and M7 can invert action of DIRx WRPIN command would be run to set Mode bits.

### 17.111.1) FLTL {#}D {WCZ} OUT bits of pins (365)

D[10:6]+D[5:0]..D[5:0] = 0. DIR bits = 0. (365) Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit. (365)

**Set** P0 FLTL Float Low Source Load Sink Pin. Resistor and diode tied Vdd.

**FLTL** output set Low would remain Low off and by switching the DIR=0 the pin goes into a high impedance state or generates sink signal when Pin DIR = 1.

#### 17.111.1\_Example\_WRD\_ FLTL {#}D {WCZ} OUT bits of pins

1) Set P0 FLTL read DIR P0 = 0

2) Read P0 input when DIR =0 TESTP #P0

3) Read DIRA and Read OUTA for #P0

4) Set DIR = 1 with DIRH #P0

5) Read P0 input when DIR =1 TESTP #P0

6) Set DIR = 0 with DIRL #P0

### 17.111.2) FLTH {#}D {WCZ} OUT bits of pins D[10:6]+D[5:0]..D[5:0] = 1. DIR bits = 0. (366)

Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.

**Set P1** FLTH Float High Sink Load Source Pin. Resistor and diode tied to GND

**FLTH** output set High would remain HIGH on and by switching the DIR =0 the pin goes into a high impedance state or generates source signal when Pin DIR =1

#### 17.111.2\_Example\_WRD\_ FLTH {#}D {WCZ} OUT bits of pins

1) Set P0 FLTH read DIR P0 = 0

2) Read P0 input when DIR =0 TESTP #P0

3) Read DIRA and Read OUTA for #P0

4) Set DIR = 1 with DIRH #P0

5) Read P0 input when DIR =1 TESTP #P0

6) Set DIR = 0 with DIRL #P0

### 17.111.3) FLTC {#}D {WCZ} OUT bits of pins D[10:6]+D[5:0]..D[5:0] = C. DIR bits = 0. (367)

Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.

**Set P0** FLTL Float Low Source Load Sink Pin. Resistor and diode tied Vdd.

**Set P1** FLTH Float High Sink Load Source Pin. Resistor and diode tied to GND

**FLTL** output set Low would remain Low off and by switching the DIR=0 the pin goes into a high impedance state or generates sink signal when Pin DIR = 1.

**FLTH** output set High would remain HIGH on and by switching the DIR =0 the pin goes into a high impedance state or generates source signal when Pin DIR =1

#### 17.111.3\_Example\_WRD\_ FLTC {#}D {WCZ} OUT bits of pins(367)

1) Set C= 0 MODC \_CLR WC

2) Set P0 FLTC read DIR P0 = 0 results In float low

3) Read P0 input when DIR =0 TESTP #P0

4) Set DIR = 1 with DIRL #P0

5) Read P0 input when DIR =1 TESTP #P0

6) Set C= 1 MODC \_SET WC

7) Set P1 FLTCL read DIR P0 = 0 reslults In float high

8) Read P1 input when DIR =0 TESTP #P0

9) Set DIR = 1 with DIRL #P1

10) Read P1 input when DIR =1 TESTP #P0

### 17.111.4)FLTNC {#}D {WCZ} OUT bits of pins D[10:6]+D[5:0]..D[5:0] = !C. DIR bits = 0.(368)

Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.

**Set P0** FLTL Float Low Source Load Sink Pin. Resistor and diode tied Vdd.

Set P1 FLTH Float High Sink Load Source Pin. Resistor and diode tied to GND

**FLTL** output set Low would remain Low off and by switching the DIR=0 the pin goes into a high impedance state or generates sink signal when Pin DIR = 1.

**FLTH** output set High would remain HIGH on and by switching the DIR =0 the pin goes into a high impedance state or generates source signal when Pin DIR =1

#### 17.111.4\_Example\_WRD\_ FLTNC {#}D {WCZ} OUT bits of Pins(367}}

1) Set C= 1 MODC \_CLR WC

2) Set P0 FLTNC read DIR P0 = 0 results In float low

3) Read P0 input when DIR =0 TESTP #P0

4) Set DIR = 1 with DIRL #P0

5) Read P0 input when DIR =1 TESTP #P0

6) Set C= 0 MODC \_SET WC

7) Set P1 FLTNCL read DIR P0 = 0 reslults In float high

8) Read P1 input when DIR =0 TESTP #P0

9) Set DIR = 1 with DIRL #P1

10) Read P1 input when DIR =1 TESTP #P0

### 17.111.5) FLTZ {#}D {WCZ} OUT bits of pins D[10:6]+D[5:0]..D[5:0] = Z. DIR bits = 0. (369)

Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.

**Set P0** FLTL Float Low Source Load Sink Pin. Resistor and diode tied Vdd.

**Set P1** FLTH Float High Sink Load Source Pin. Resistor and diode tied to GND

**FLTL** output set Low would remain Low off and by switching the DIR=0 the pin goes into a high impedance state or generates sink signal when Pin DIR = 1.

**FLTH** output set High would remain HIGH on and by switching the DIR =0 the pin goes into a high impedance state or generates source signal when Pin DIR =1

#### 17.111.5\_Example\_WRD\_ FLTZC {#}D {WCZ} OUT bits of Pins(369}}

1) Set Z= 0 MODZ \_CLR WZ

2) Set P0 FLTZ read DIR P0 = 0 results In float low

3) Read P0 input when DIR =0 TESTP #P0

4) Set DIR = 1 with DIRL #P0

5) Read P0 input when DIR =1 TESTP #P0

6) Set Z= 1 MODZ \_SET WZ

7) Set P1 FLTZ read DIR P0 = 0 reslults In float high

8) Read P1 input when DIR =0 TESTP #P0

9) Set DIR = 1 with DIRL #P1

10) Read P1 input when DIR =1 TESTP #P0

### 17.111.6) FLTNZ {#}D {WCZ} OUT bits of pins D[10:6]+D[5:0]..D[5:0] = !Z. DIR bits = 0. (370)

Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.

**Set P0** FLTL Float Low Source Load Sink Pin. Resistor and diode tied Vdd.

**Set P1** FLTH Float High Sink Load Source Pin. Resistor and diode tied to GND

**FLTL** output set Low would remain Low off and by switching the DIR=0 the pin goes into a high impedance state or generates sink signal when Pin DIR = 1.

**FLTH** output set High would remain HIGH on and by switching the DIR =0 the pin goes into a high impedance state or generates source signal when Pin DIR =1

#### 17.111.6\_Example\_WRD\_ FLTNZ {#}D {WCZ} OUT bits of pins(370)

1) Set Z= 1 MODZ \_CLR WZ

2) Set P0 FLTNZ read DIR P0 = 0 results In float low

3) Read P0 input when DIR =0 TESTP #P0

4) Set DIR = 1 with DIRL #P0

5) Read P0 input when DIR =1 TESTP #P0

6) Set Z= 0 MODZ \_SET WZ

7) Set P1 FLTNZ read DIR P0 = 0 reslults In float high

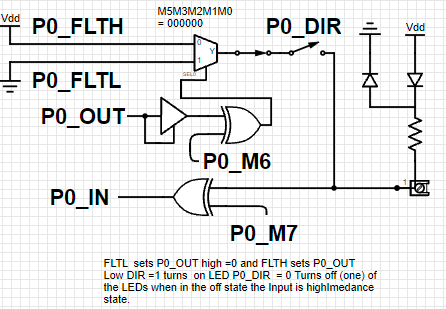
8) Read P1 input when DIR =0 TESTP #P0

9) Set DIR = 1 with DIRL #P1

10) Read P1 input when DIR =1 TESTP #P0

### 17.111.7) FLTRND {#}D {WCZ} OUT bits of pins D[10:6]+D[5:0]..D[5:0] = RNDs. DIR bits = 0 (371)

. Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.



#### 17.111.7\_Example\_WRD\_FLTRND {#}D {WCZ} OUT bits of pins (371)

1) Set P0 FLTRND read DIR P0 = 0 results In P0\_FLTH or P0\_FLTL

2) Read P0 input when DIR =0 TESTP #P0

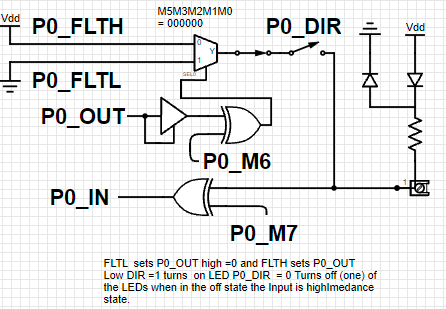
3) Set DIR = 1 DRH #P0

4) Read P0 input when DIR =1 TESTP #P0

5) Repeat

### 17.111.8) FLTNOT {#}D {WCZ} Toggle OUT bits of pins D[10:6]+D[5:0]..D[5:0]. DIR bits = 0. (372)

Wraps within OUTA/OUTB. Prior SETQ overrides D[10:6]. C,Z = OUT bit.



#### 17.111.8\_Example\_WRD\_ FLTNOT {#}D {WCZ} Toggle OUT bits of pins (372)

1) Set P0 FLTNOT read DIR P0 = 0 results In float low

2) Read P0 input when DIR =0 TESTP #P0

3) Set DIR = 1 DRH #P0

4) Read P0 input when DIR =1 TESTP #P0

5) Repeat