project-board®

1 DIGIT COUNTER

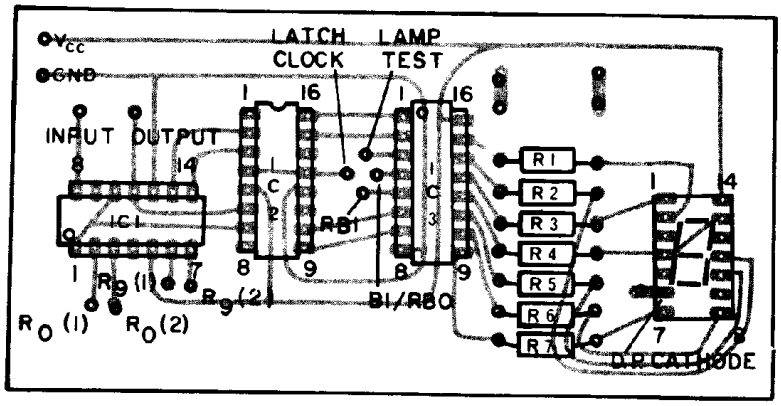
This package contains a complete printed circuit board – ready for parts to be added. To construct this Project Board you'll need the following parts:

PARTS LIST

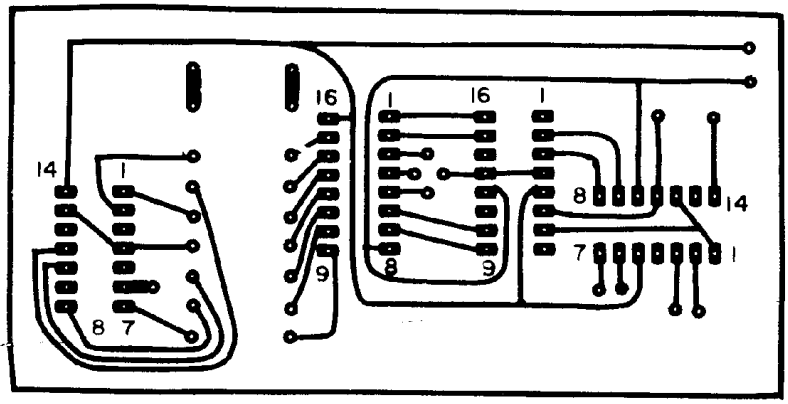
Symbol	Description	Quantity	Radio Shack Cat. No.
IC-1	RS7490 Decade Counter	1	276-1808
IC-2	RS7475 Four-Bit Latch	1	276-1806
IC-3	RS7446 BCD to 7-Segment Decoder/Driver	1	276-1805
R-1 thru R-7	150 ohm, ½ Watt Carbon Composition Resistor	7 pcs	271-000 (4 pkgs)
	7-Segment LED Readout	1	276-053
	14-Pin IC Socket	2	276-027
	16-Pin IC Socket	2	276-030

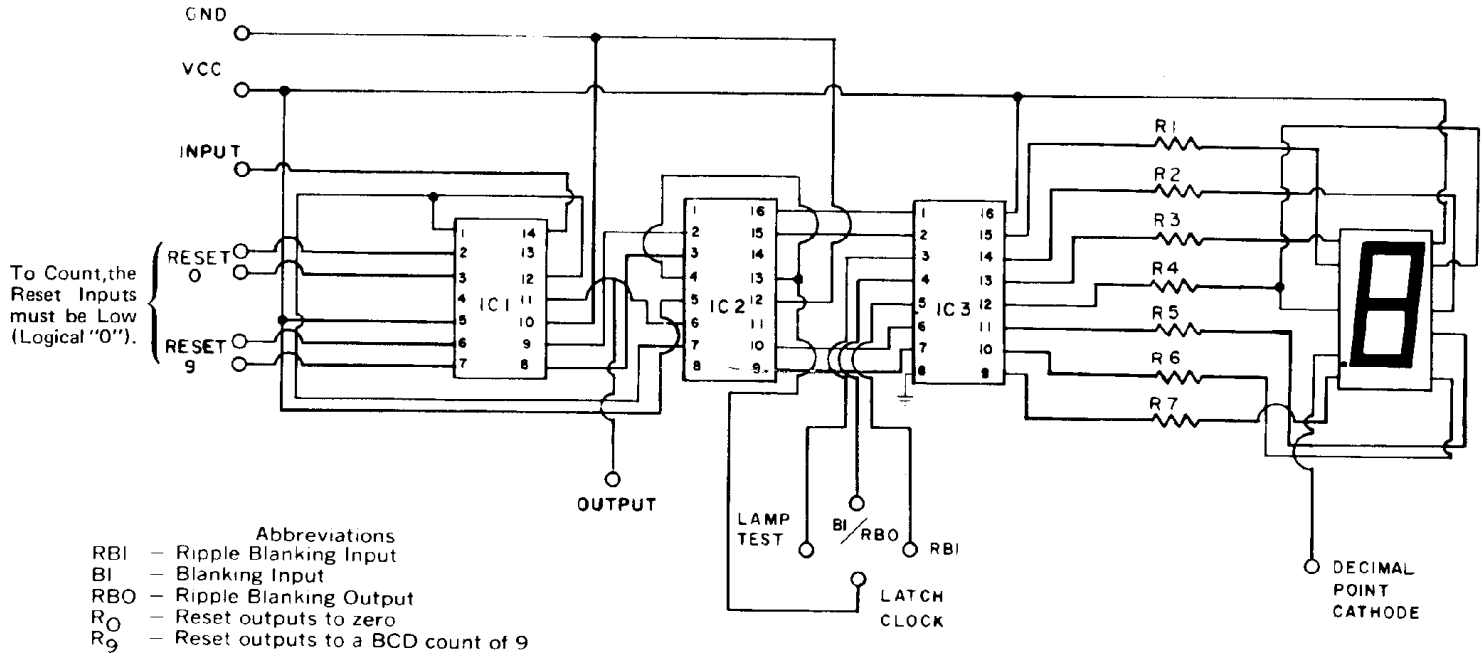
Plus appropriate tools and solder. Also, you may want to purchase a suitable chassis or cabinet for permanent installation and make external connections for inputs and outputs.

TOP VIEW OF PC BOARD



FOIL VIEW OF PC BOARD





Abbreviations
RBI – Ripple Blanking Input
BI – Blanking Input
RBO – Ripple Blanking Output
R_0 – Reset outputs to zero
R_9 – Reset outputs to a BCD count of 9

SCHEMATIC

HOW THE 1 DIGIT COUNTER WORKS

IC-1 is used in this application as a Binary Coded Decimal decade counter. To operate in the 10 count mode, both 0 and 9 resets must be low (0).

The counter will count the pulses applied to the input of IC-1.

To return all outputs to 0, both resets must be high (1).
To return all outputs to 9, both resets must be high (1).

Supply voltage can be a battery or a low voltage power supply, such as Radio Shack Catalog Number 277-102.
NOTE: All inputs should not be over +5 volts.

With the Latch Clock – IC-2 – high (1), the pulses provided through IC-1 will be counted normally on the LED readout. When the Latch Clock goes low (0), the number showing on the LED is held stationary until the Latch Clock goes back to high (1).

To test the 7-segment LED readout, the Lamp Test must be low (0); all seven segments will then light.

When a low (0) is applied to BI, all LED segments will be blanked. Going back to a high (1) at this time will relight the segments, again giving a visual display.

If it is desired to have the digit "zero" blanked, RBI must be low (0).

To light the decimal point, a 150 ohm, ½ Watt, resistor must be added between V_{CC} and the D.P. cathode.

Recommended Operating Conditions:

Supply Voltage	4.75V - 5.25V
Input Voltage	5V
Supply Current	32mA (typ)
Logic 1 input Voltage	2V (min)
Logic 0 Input Voltage	0.8V (max)
Logic 1 Output Voltage	2.4V (min)
Logic 0 Output Voltage	0.4V (max)
Average Power Dissipation	160mW

You may wish to use this kit in other types of digital applications. You should also be aware that other components (and Project Boards, such as our 5-Volt Regulated Power Supply, Radio Shack Catalog Number 277-102) may be used to build these other projects.

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External gate doubles counter speed

by Jeffrey Mattox
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The counting rate of a standard synchronous up/down binary or decade counter can be doubled without altering the clock frequency. A single external gate does the trick for the count-up or the count-down mode.

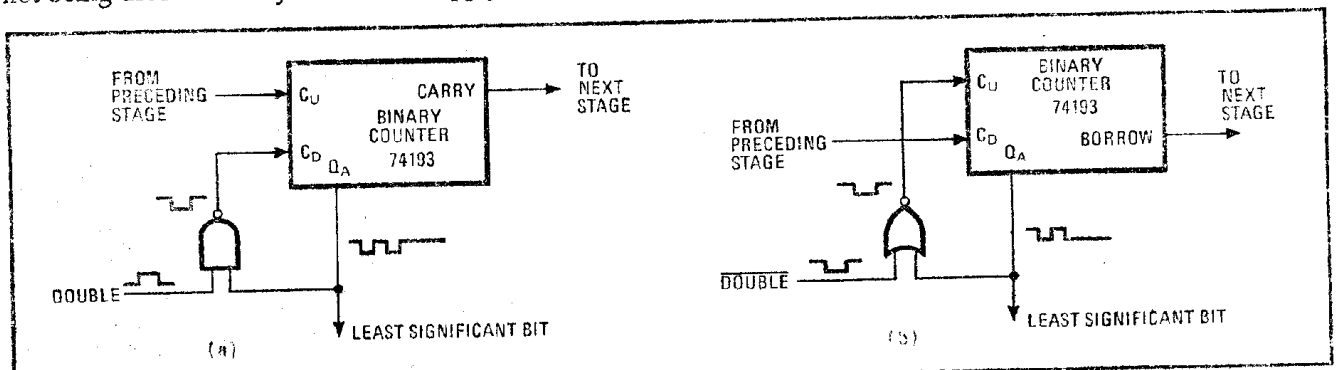
The ability to double the counting rate is useful for applications where a counter must be advanced at twice the normal rate, as in racing the digits to set a digital-clock stage. The extra gate can also be used to halve the counting rate, depending on the logic level of the controlling signal.

Both the decade counter (for example, a type 74192) and the binary counter (for example, a type 74193) have two clock lines—one for the count-up mode, and the other for the count-down mode. The clock input that is not being used is usually tied to the supply line. For either type of counter, there is a counting flip-flop for each output bit.

By sensing the counter's least significant output bit and lowering the alternate-clock input at the proper time, the least significant bit is kept static, and the second counter flip-flop receives all the primary clock pulses. In addition, the state of the least significant bit locks out the alternate-clock input from the other counting flip-flops. For an up-counter, the least significant bit must be high; for a down-counter, it must be low.

The circuit of (a) shows a type 74193 binary counter connected for the count-up mode. The alternate-clock input, in this case the count-down input (C_D), is controlled by a NAND gate. When the DOUBLE input goes high, the C_D input is brought low as soon as the least significant bit is high. The least significant bit remains high until the DOUBLE input returns to the low level. Meanwhile, the count frequency appears to double.

The circuit of (b) is for the count-down mode. It is similar to the one for the count-up mode, but an OR gate is used instead and the DOUBLE control signal must be inverted. The CARRY and BORROW outputs of the counter operate normally so that the doubled counting rate may be carried to the next stage. □



Twice as fast. External gate can double or halve the counting rate of either a decade or binary up/down counter, depending on the logic level of the control signal. The actual clock frequency remains the same. Here, the operating speed of a binary counter is doubled for both the count-up mode (a) and the count-down mode (b). The counter's unused alternate-clock input goes to the controlling logic signal.

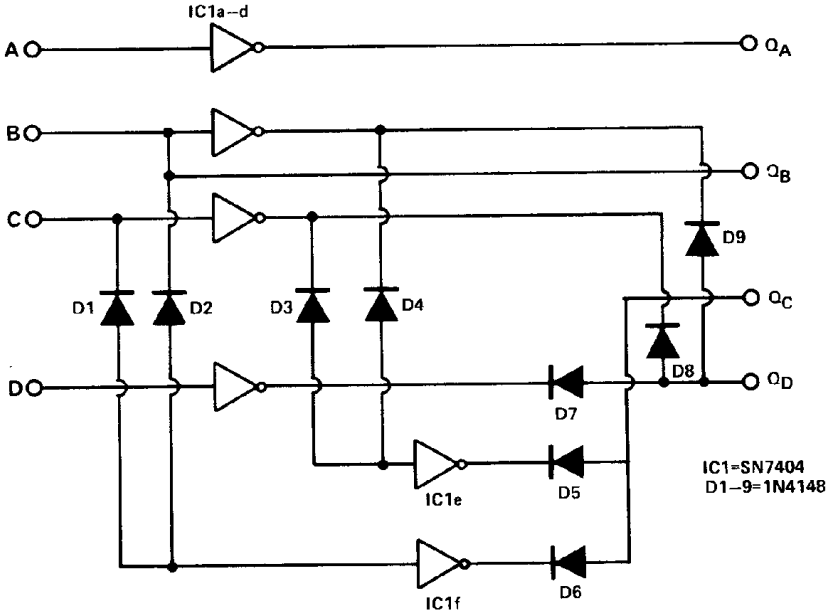
Cheapo Down Counter

AF Bush

This circuit, when presented with a 4 bit binary number in the range 0000–1001 will present the nines complement of that number at the output.

Connecting the circuit between a 7490 and a 7447, will, instead of the usual up count, provide a display which counts down from nine.

This provides a useful alternative to the expensive 74192 when only a down count is required.



BCD COUNT	INPUTS D	C	B	A	OUTPUTS Q_D	Q_C	Q_B	Q_A	COMPL–EMENT
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

$Q_A=\overline{A}$
$Q_B=B$
$Q_C=(\overline{B}\cdot\overline{C})\cdot(\overline{B}\cdot\overline{C})$
$Q_D=B\cdot\overline{C}\cdot D$

Divide-by-N counter generates square-wave output for odd N

by Steve Lieske
Hewlett Packard Co., Boise, Idaho

An extremely flexible digital frequency divider can be built using only two presettable synchronous counters and three NAND gates. The circuit allows the duty cycle of its output to be controlled to within one half-cycle of the input frequency. This capability is useful in many timing and control applications. For example, in dividing down a high-speed clock, the output duty cycle can be selected to optimize system timing considerations, such as propagation delay or data-setup time. It can also be used in control circuits to generate timing windows.

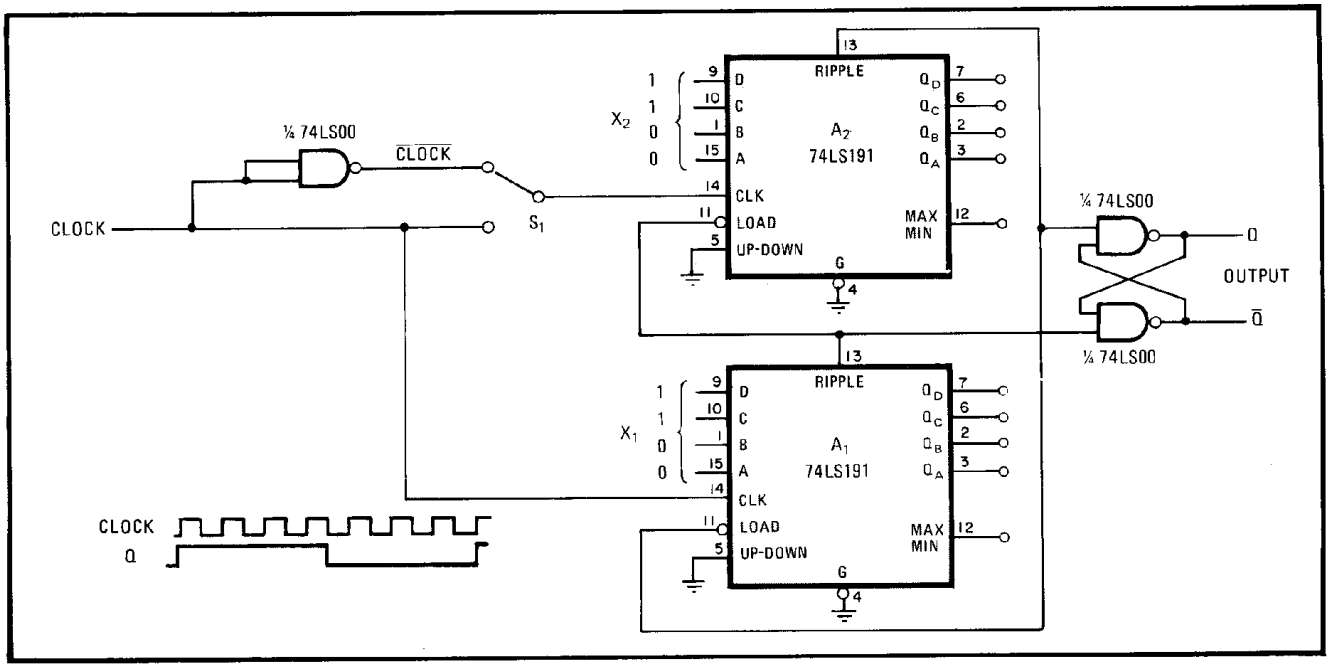
The 74LS191 counters A_1 and A_2, each programmed by the data at preset inputs X_1 and X_2, control the on and off time of the output cycle, respectively. When A_1 counts from its preset value to the counter's maximum value of 15, its ripple output goes low, setting the Q output of the two-gate, 74LS00 flip-flop to logic 0. A_2 is then asynchronously loaded with the X_2 data and counts from that point to 15. When A_2 overflows, its ripple output sets the flip-flop high, A_1 is loaded with X_1, and the cycle repeats.

If Q is to be asserted for an odd number of half cycles, A_1 and A_2 must be clocked on opposite edges (which produces a square-wave output when N is odd). If Q is asserted for an even number of cycles, the counters are clocked in phase. S_1 and the 74LS00 NAND gate at the input allow selection of either option.

The timing diagram at the bottom of the figure shows a square-wave output for a divide-by-seven counter. In this application, X_1 and X_2 are programmed so that the number 12 is loaded into their respective counters, as shown. Generally, the number that presets the counters will be equal to $15-N/2$, taken to the nearest integer.

N is limited to a minimum value of 1. In this circuit, it may assume a maxiumum value of 14. For greater frequency division, additional counters must be cascaded. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



Adjustable duty cycle. A_1 and A_2 in divide-by-N counter control on and off time of output cycle, respectively. X_1 and X_2 inputs determine N value, preset counters to $15-N/2$. Square-wave output for odd N is achieved by advancing counters on opposite edges of clock.

Up/down counter processes data over single channel

by N. Bhaskara Rao
U. V. C. E., Department of Electrical Engineering, Bangalore, India

Two inputs are normally required for incrementing and decrementing an up/down counter—a count-up command line and a count-down line. But commands can be sent and received over a single channel if they are first multiplexed. Shown here is a transmitter-receiver pair for the one-channel system, which is particularly cost-effective over long distances.

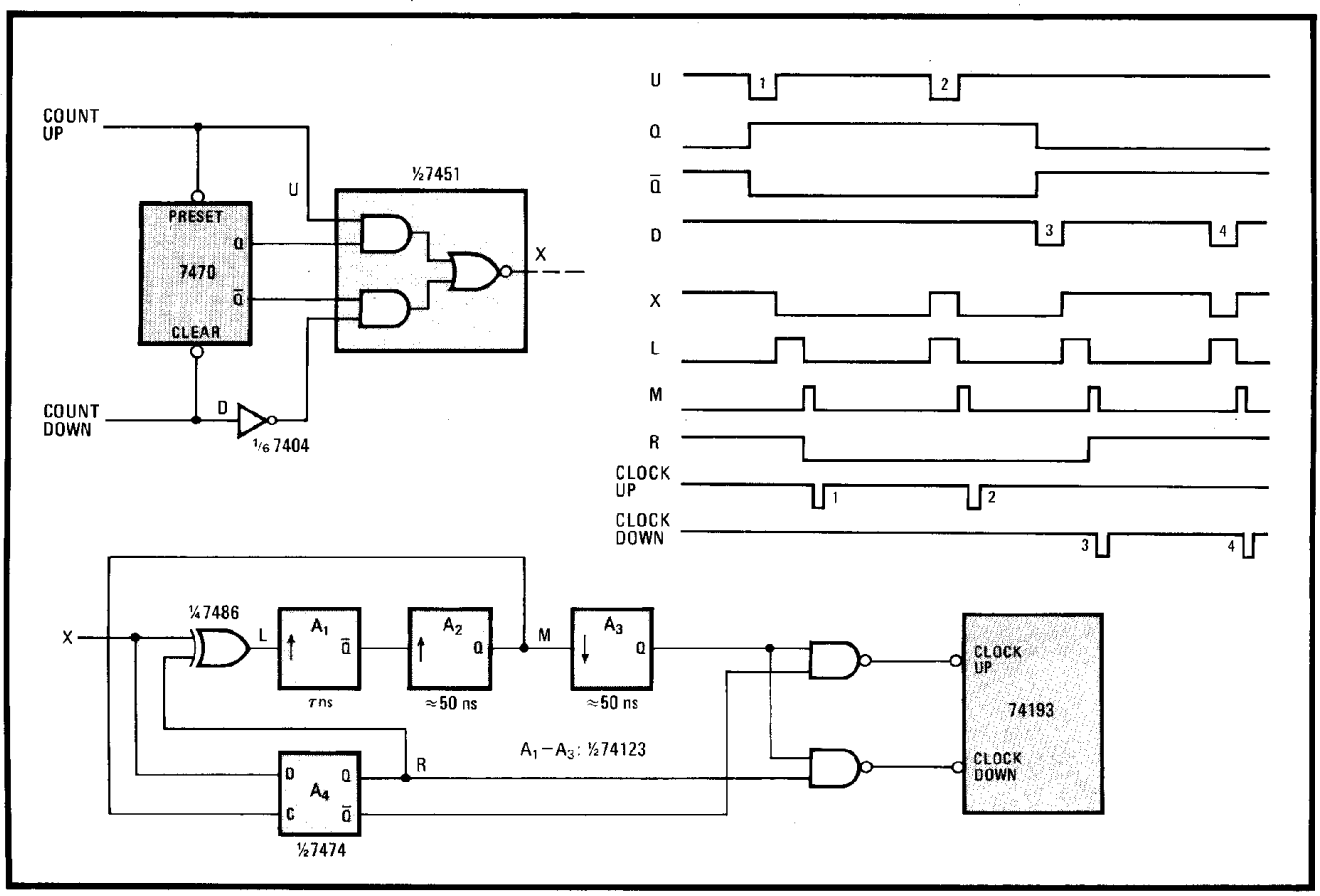
At the sending end, it can be seen that $\bar{x} = QU + \bar{Q}D$, where x represents the transmitted signal, U is the count-up variable, and D is the count-down variable. It is assumed that the width of the U and D pulses is not more than a few hundred nanoseconds, and that the frequencies of U and D are relatively low.

When negative-going count-up pulses appear on the U line, the 7470 flip-flop is preset to Q = 1 and so x = $\bar{U}$ thereafter. Thus x moves from logic 1 to logic 0 on the trailing edge of the count-up command.

Similarly, a count-down command clears the 7470 and so x = D. Thus x moves from logic 0 to logic 1 on the trailing edge of the down command. The timing diagram details transmitter operation.

The receiver determines if variations in x are due to changes in U or D by using an indirect and inexpensive phase-locking scheme. Transitions in x are introduced at the input of the 7486 exclusive-OR gate. Feedback loop A_1, A_2, and A_4 acts to bring point L high, regardless of whether the transition is positive- or negative-going. One-shot A_1, having a set delay time, τ, slightly greater than the width of the U and D command pulses at the transmitter, then triggers one-shot A_2. By this time, x has stabilized, so that a logic 0 (U pulse) or a logic 1 (D pulse) is clocked into A_4, thus bringing point L low τ nanoseconds after it goes high.

Meanwhile, one-shot A_3 is fired, and the active contents of A_4 are transferred to either the clock-up or the clock-down port of the 74193. The receiver's timing diagram should be inspected to clarify operation. □



Self-synchronous. Flip-flop and gates pack count-up and count-down commands on a single data line for transmission over long distances (top). Receiver (bottom) senses polarity of pulses, without using complicated synchronous detectors, to increment or decrement up/down counter. Three one-shots provide superior operation as compared to detection schemes employing sequential logic.