Choosing discrete transceivers for USB apps

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The integration of USB transceivers into ASICs or power-management ICs (PMICs) has been an industry trend in recent years, resulting in a limited opportunity for discrete PHY transceivers. With surging demand for high-technology consumer products, OEMs and reference-design houses must balance the high cost of chipsets and innovation with consumers' clamor for low-cost products. Several discrete transceivers are available, but the need to differentiate has led to product variations and, consequently, a lot of confusion. In some cases, an exact replacement device may not be available and electrical characteristics may have to be traded off. While cost is an important factor, performance should not be compromised.

Today, selection of discrete transceivers often depends on ESD capability, integrated pull-up resistors and I/O host configuration (differential or single-ended). With many applications sharing D+/D- cable signal lines, there is a need to understand discrete-transceiver functionality in both disable and sharing modes. Transceivers must be compatible with baseband or application processor I/O configurations.

In 1997, the discrete USB1.1 transceivers had no integrated regulator or additional low-voltage host supply ($1.65 \le V_{CCio} \le 3.6$ V). The design was a discrete way of providing a single supply to the transceiver ($3.0 \le V_{CC} \le 3.6$ V). As it gained popularity, the 2.7V type was recognized for offering multiple supplies, allowing the integrated regulator transceiver to penetrate the market. **Figure 1** illustrates the architecture of the two devices. The USB1T1103 uses I/O pins interfacing with the host versus the traditional USB1.1 transceiver. For the USB1T11A type architecture, a designer must ensure that there is a way to turn off the supply to 1.5k to meet the USB 2.0 specification. This is often overlooked when a product is subjected to USB-IF1 compliance testing.

Initial considerations when

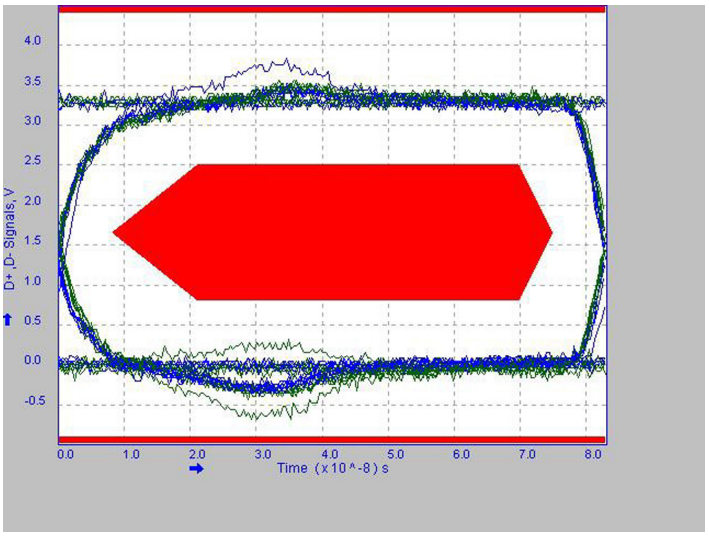

Figure 2: By increasing R_S, it can easily be proven that the eye is not violated with Edge rates as high as 25ns.

Key features of discrete transceivers

	Integrated regulator/ interface supply (V_{reg} / V_{ccio})	ASIC side interface (V_{po}/V_{mo} /V_p/V_m)	Mode (Diff/SE)	Speed	V_{bus} monitor	Sharing mode	Disable mode
USB1T11A	No	Separate	Selectable	FS/LS	No	No	No
USB1T1103	Yes	I/O	Differential	FS	Yes	Yes	Yes
USB1T1104	Yes	Separate	Selectable	FS	Yes	Yes	Yes
USB1T1105A	Yes	Separate	Selectable	FS/LS	No	Yes	Yes

Table 1: Some key differences between discrete transceivers available may be common across IC vendors.

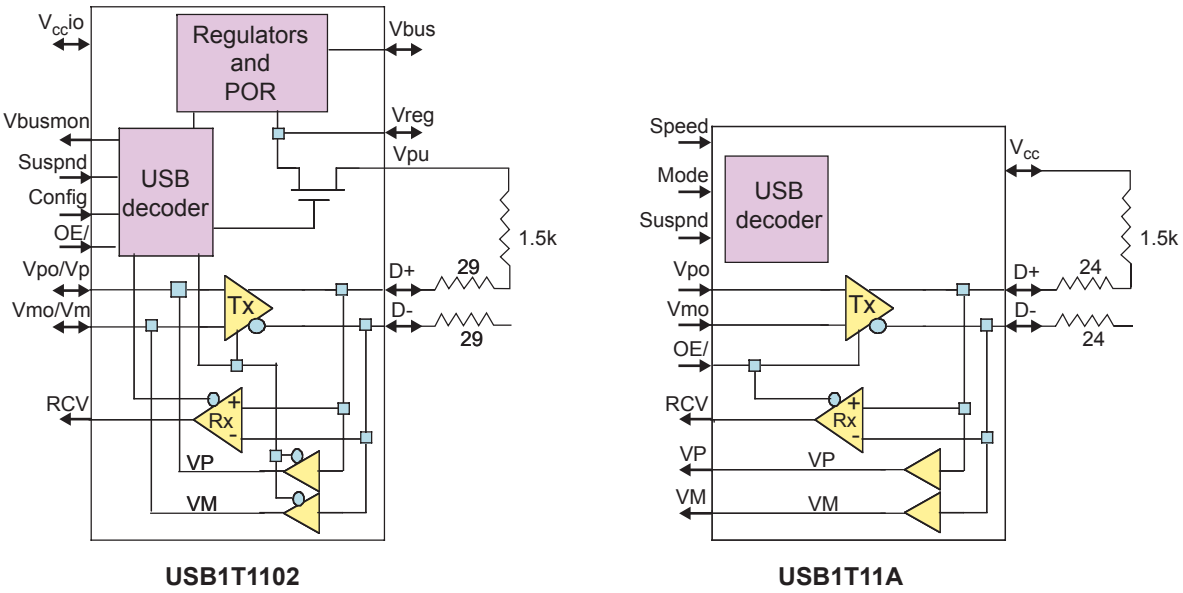

Figure 1: Features touted by IC vendors include ESD to ± 15kV, enumeration pin and integrated 1.5kΩ pull-up.

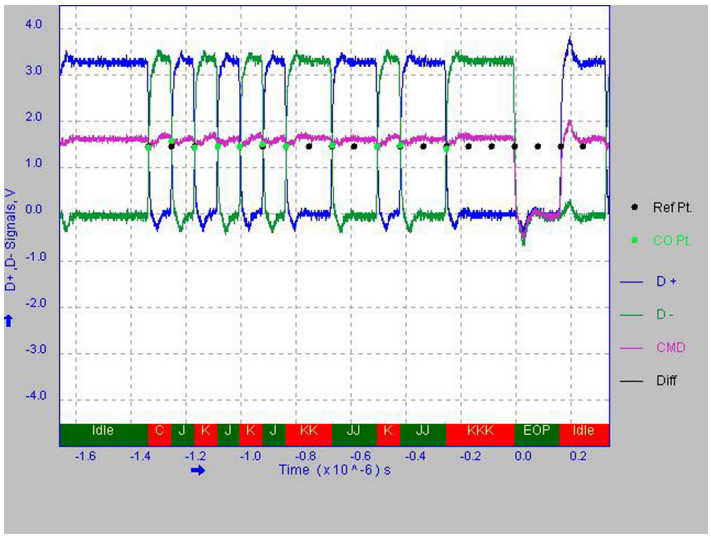

Figure 3: Packet diagram for FSC USB1T1103 with R_S=30Ω, 1m cable, Tier 6.

selecting a USB transceiver include whether I/O or separate host inputs and outputs are preferred; FS or FS/LS driver capability; single-ended or differential host interface; and separate V_{CC} io and V_{bus} monitoring capability. Typically the choice for I/O configuration is determined by the application or baseband processor used by the reference design. Other features touted by IC vendors are ESD to ± 15kV, enumeration pin (configuration in **Figure 1**) and integrated 1.5kΩ pull-up. In ultraportable designs, battery life is critical–thus, it is important to fully understand potential current consumption during suspend, disable and sharing modes.

Disable mode puts the interface between the transceiver and the baseband or processor in high impedance. Sharing mode, on the other hand, can disconnect the V_{bus}/V_{reg} supplies such that the D+/D- signal lines are shared by another function within the product. The USB transceiver driver enters a high-impedance state in this mode.

Table 1 highlights some of the key differences between discrete transceivers available, which may be common across IC vendors.

In addition to the interface characteristics, there are subtle differences in transceivers' integrated 1.5 kΩ pull-up resistors, enumeration pin (under software control) that disconnect the 3.3V supply from the pull-up, latched RCV data during SEO event and series resistor for USB data line driver impedance.

ESD components

Every IC vendor specifies a series resistor different from those used by its competitors since it is a function of its process technology and output buffer design structure. This practice may pose problems, particularly when manufacturers seek a second source device or choose to replace a current vendor. In a well-designed application, conforming to USB 2.0 specifications and design guidelines may have less impact than what the manufacturer perceives. If a slight increase in edge rates is acceptable, the lower resistor is used as the manufacturing insert. Typically, the lower the R_s on the datasheet, the higher the silicon driver impedance becomes, which in turn shows the potential for a smaller NMOS pulldown (lower capacitance) and slightly lower drive source/sink capability of transceiver output structures.

Having chosen the R_s resistor for the transceiver output, external ESD or choke filter components are added on the D+/D- pins. There is much confusion about which ESD rating to target. Many engineers will simply respond to the value of ESD on the datasheet (8kV vs. 15kV) without understanding exactly how that ESD specification was characterized. In some cases, extra capacitance (typically 4.7µF) is added, cutting the edge of the ESD test pulse. It is thus important to check the test schematic on the specific IC manufacturer datasheet. The USB1T1103, for example, is 15kV (HBM Mil 883E -contact) for D+/D- with no extra capacitance. If the designer specifies the use of additional EMI and ESD components, the series resistance of the common mode chokes must be taken into account. This resistance, often 4-8Ω, has to be accounted for and R_s may need to be modified to meet the USB2.0 driver impedance specifications. In the case of the ESD external components, it is also important to understand the capacitance characteristics to ensure that USB2.0 requirements are met and that the ESD immunity is modified by this capacitance.

	Driver impedance		Series resistor
	Min.	Max.	
USB1T11A	4	20	24
USB1T1103	7	16	27
USB1T1104	1	11	33
USB1T1105A	1	11	33

Table 2: Discrete transceiver output impedance and series resistance.

Edge rates

Another aspect of USB design that is often misinterpreted during product design is the USB legacy edge rates and their matching tolerance. These are specified into a lumped load, not a distributed load, hub or gold tree. Some customers have created their own internal QA environment guidelines, requiring correlation between edge rate, edge-rate matching and EMI compliance based on proven design practices for shielding and specific test environments. These guidelines obviously do not guarantee USB-IF compliance. Hence, when a product is due for release and commercial compliance software indicates non-conformity to the specification (e.g. 20ns for FS), it is important to understand the differences between the specification and the system environment when interpreting results. Absolute measurement values for rise and fall times are only valuable for reference and comparison, since it is the eye mask that is critical. Failing the eye in the current USB-IF compliance testing for FS/LS applications spells more problems for the product. It typically indicates poor hub design, mismatched PCB characteristics for D+/D- signal lines or excessive capacitance/resistance to the USB2.0 specification.

For example, when tested in a hub containing uncertified Gold Tree devices, it is highly possible to measure 19-25ns rise times. But when validated in a characterization test fixture (lumped 50pF load), measurements of 8-11ns may be common. Upon seeing 19-25ns measurements, one is led to believe that the silicon is defective; but with problem solving, one can lay the blame on excessive hub (or peripheral) capacitance, poor PCB design, a noise filter external device with very high series resistance/capacitance or incorrect series resistor.

The current USB-IF compliance testing reports on the eye diagram, with rise/fall times considered as informational. By increasing R_s, it can easily be proved that the eye is not violated with edge rates as high as 25ns. Failure to meet these Edge-rate criteria does not necessarily mean that a product will not function in a USB system. Conformity with these criteria, however, boosts consumer confidence in a product and guarantees USB-IF compliance from a certified test lab.

Figures 2 and **3** depict the eye diagram and packet waveform for a prototype product using a discrete transceiver (FSC USB1T1103) with a 30Ω series resistor, measured at Tier 6 using the Tektronics TDSUSB2 software and test jig.

In choosing the best discrete USB transceiver, it is important to understand the following: subtle features of the individual transceiver relative to power supply configurations; output states when in sharing mode; default application processor output states (pulled high, pulled low, programmable, external resistors); series resistor recommended by the silicon vendor; and external ESD or EMI filter component impact on the application environment. By recognizing the origins and definitions of legacy specifications and observing the recommended "good USB design guidelines", manufacturers can design USB-IF compliant products using discrete transceivers from different silicon vendors on their approved vendor list.

To get optimal performance, the designer must fully understand the various aspects of the USB 2.0 environment and its interaction with non-USB related components, and the relative trade-offs for consideration. In the case of ESD immunity, the designer must know the exact test setup and how the device was characterized.