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Lattice Semiconductor MachXO3 FPGA Family

Media FAQ

Q: What is Lattice Announcing?

A: The MachXO3™ FPGA family. This is a new family designed to solve bridging and I/O expansion requirements. The MachXO3 FPGA family provides instant-on, non-volatile, small-footprint FPGAs that use advanced package technology to lower cost and provide the highest I/O density in packages as small as 2.5x2.5mm.

Q: Why is the MachXO3 FPGA family being announced now?

A: Engagements with customer promoting the benefits of the MachXO3 FPGA family are underway now and public information is being made available so designers can take advantage of the new capabilities to evaluate and solve their product challenges.

Q: When will devices be available in distribution and supported in software?

A: Diamond® Software support will be available in December and first production devices will ship shortly thereafter. Early access software will be provided to customers who join the early access program.

Q: What is the call to action for customers?

A: Customers can go to the [Lattice Web Site](#), learn about the MachXO3 family and sign up for the early access program as well as get priority for first production devices which will be available at the end of the year.

Q: What are the MachXO3 FPGAS family's key markets and applications?

A: Consumer, automotive, compute, Industrial, storage markets, as well as wireless and wired communications infrastructure.

The MachXO3 FPGA family is designed to provide designers with options for bridging, I/O expansion, and implementing programmable control. The second page of the press release provides more details about the types of applications the MachXO3 FPGA family supports.

Q: What details are being given to customers now?

A: Details of the family including, logic cell density (640-to-22K), I/O (up to 540), 3.125Gbps SERDES capabilities, DSP, on-chip regulators, power consumption (as low as 50mW static), details of new advanced packaging technology, and integrated support for MIPI, PCIe, and GbE so customers can begin their designs now.

Q: Is MachXO3 pin compatible with MachXO2™?

A: One of the key capabilities in the new MachXO3 family is the ability for customers to migrate from MachXO2 to MachXO3 when new capabilities are needed to enable their design. For key package and logic densities, devices that are pin compatible are available along with guidelines for proper board layout.

Q. Will there be an evaluation kit for the MachXO3 FPGA family?

A. Yes, evaluation kits along with reference designs that showcase the features and capabilities in MachXO3 FPGAs will be available after production devices are available.

Q. Will the IP and Reference Designs for the MachXO™ and MachXO2 families work with the MachXO3 FPGA family?

A. Yes. Existing reference designs targeting MachXO and MachXO2 as well as IP will be ported over to the MachXO3 family. Similar to pin compatibility we are enabling customers to easily leverage the MachXO3 family's features and capabilities for next generation systems.

Q: What packaging will be available for MachXO3 devices?

A: The MachXO3 family leverages the most advanced Wirebond and Flipchip technology to deliver devices with up to 540 I/O and integrated 3.125Gbps SERDES optimized in 0.5mm, and 0.8mm pitch packages to simplify manufacturing. The MachXO3 family also leverages advanced Wafer Level Chip Scale Packaging technology to deliver devices as small as 2.5X2.5mm that support high performance interfaces such as MIPI.

Q: What is wafer level chip scale packaging?

A: This is a key differentiator for Lattice Semiconductor. Wafer-level chip-scale packages (WLCSP) are an advanced package style in which the semiconductor integrated circuit (IC) is mounted directly to the printed circuit board (PCB), face-down, by way of solder balls that are attached directly to the IC without the need for an interposer or wirebonds. This enables the use of a smaller solder ball diameter and tighter ball pitch, as well as a shorter electrical path between the IC and PCB, resulting in improved electrical and thermal performance as well as dramatically lower assembly costs.

Q: Is the MachXO3 FPGA family flash based and does it use multi-die packaging?

A: The MachXO3 FPGA family leverages non-volatile configuration technology acquired through Lattice's acquisition of Silicon Blue. The technology has been successful with our iCE40 family and Lattice is taking the next steps to apply it to our product portfolio.

Q: How does the MachXO3 FPGA family compare to the MachXO and MachXO2 families?

A: The new MachXO3 FGPA family carries forward the non-volatile benefits of the two earlier families, which also include on-chip memory, remote field upgrades, low-power sleep mode, LVDS and other features.

MachXO3 devices come with hardened DSP and 3.125Gbps SERDES capabilities, smaller packaging, higher density of I/O and logic cells, as well as hard and soft IP support for MIPI, PCIe, GbE and other emerging connectivity interfaces.

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Q: How does the MachXO3 family differ from iCE40 or ECP3 families?

A: The iCE40 family is a much smaller device with capabilities optimized for small mobile devices such as smart phones. ECP3 devices are much higher in density and are optimized for applications requiring high-data throughput.

Q: Why would customers choose MachXO3 FPGAs over existing Lattice products, or competitive solutions?

A: The MachXO3 family offers the lowest-cost per I/O of any FPGA on the market today and further distinguishes itself with on-chip 3.125 Gbps SERDES capabilities, as well as IP resources for bridging emerging interfaces such as MIPI, PCIe, GbE.

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