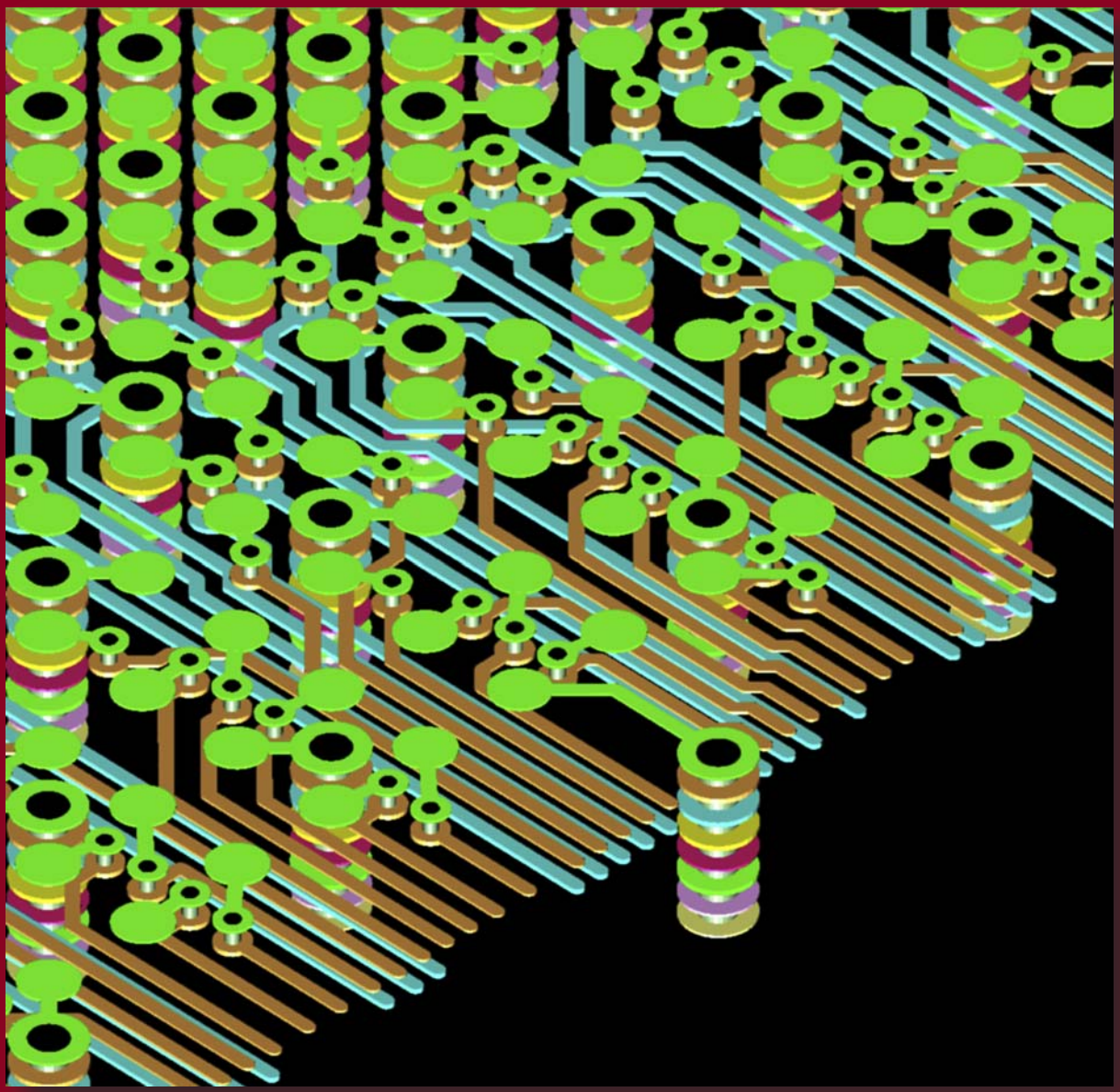
BGA Breakouts and Routing

Second edition



Mentor Graphics®

Charles Pfeil

BGA Breakouts and Routing

Effective Design Methods for Very Large BGAs

Second Edition
Version 5.0

Charles Pfeil

8/26/2008

Very large BGAs, over 1500 pins, present a unique challenge for routing on a printed circuit board. Often just routing out of the BGA is the primary contributor to the number of layers required for routing. This book presents a number of studies and solutions for addressing these challenges.

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Table of Contents

Preface – Second Edition

This new edition includes updates throughout the book with greater details, new methods, and clearer figures. It also has an additional chapter called “Software for Generating BGA Fanouts”. This chapter describes how to use new software in Mentor Graphics Expedition PCB and BoardStationXE to automatically generate efficient fanouts patterns for large dense BGAs.

Chapter One - Introduction

This book is for PCB designers who are designing boards with multiple very large Ball Grid Array (BGA) packages. It explores the impact of dense BGAs with high pin-count on PCB design and provides solutions for the inherent design challenges. Though you may not yet have been confronted with the difficulties of routing BGAs and the impact on fabrication costs and signal integrity, this book will reveal these potential pitfalls as well as methods to mitigate these problems.

There are volumes of information about BGA package technology that look at the device from all aspects including materials, thermal characteristics, assembly methods, reliability, and electrical performance; yet little guidance is available regarding effective PCB design methods.

The BGA is the most popular packaging option at this time for large pin count devices. Used for many circuit technologies including FPGA, SoC, SiP and ASIC, the BGA provides a cost-effective and reliable method to mount the device on a printed circuit board. There are many benefits to using this package; however, its greatest asset - the ability to provide an extremely dense array of thousands of pins - also turns out to be a tremendous problem for PCB design.

The BGA density and pin count continues to increase; yet, the ability to effectively design with these devices has not kept pace. Fortunately significant advancements in PCB fabrication technology have enabled further miniaturization in the manufacturing process. These improvements along with new software and design methods specifically for BGAs provide a means to successfully design using these devices.

The intent with this book is to provide PCB designers with knowledge and proven techniques that may be used to overcome the challenges presented by current and future BGA devices. These techniques have been developed

over the last 18 months and have come from extensive evaluation of various BGA packages and real PCB designs.

Expedition PCB

All the figures showing PCB design graphics are screen captures from Mentor Graphics Expedition™ PCB. The cover image was created using the prototype Expedition PCB 3D Viewer. The fanouts were created using the existing fanout and copy trace routines, and the escape traces were mostly added using prototype automatic routing software. These capabilities and more related to BGA breakouts and routing are available in the 2007.3 release of Mentor's Expedition PCB and Board Station® XE suite of tools.

Figures

There are more than a hundred figures in this book showing details about BGA breakouts. I encourage you to study them with the intent of finding techniques and tricks that will help you route these challenging devices. With all the variables involved in routing of large BGAs, my specific examples may not map directly to your experiences; however, you should be able to discover principles that can, at a minimum, give you some new ideas that will enable greater route density, a reduction in layer count and help bring your products to market faster.

Definitions

These definitions are in the context of BGA breakouts and routing.

Breakout - The combination of fanouts and escape traces, which allow routing out of the BGA pin array to the perimeter of the device prior to general routing of the PCB. See figures 1-1 and 1-2.

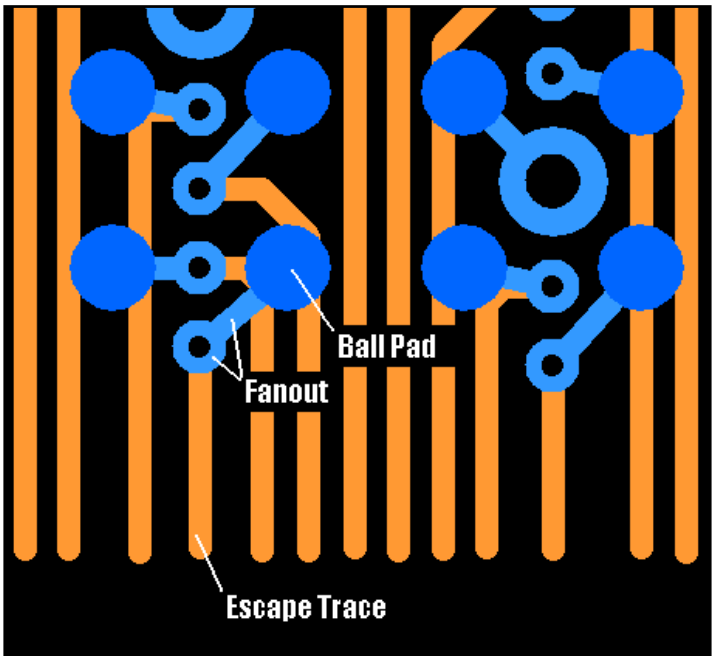


Figure 1-1: Breakout definition

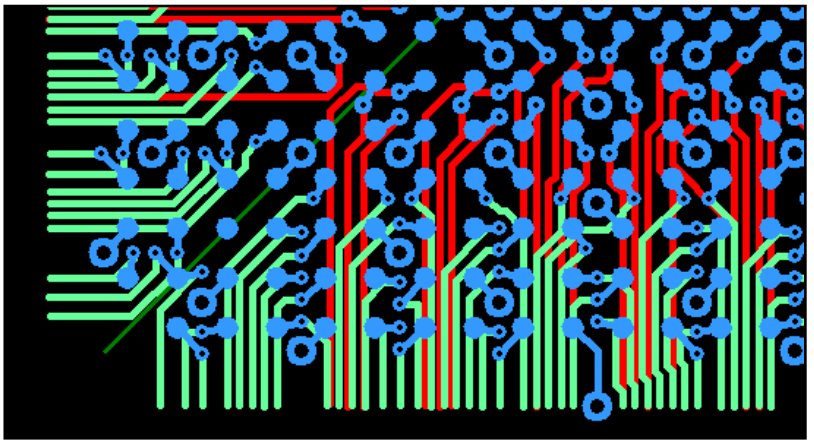


Figure 1-2: Breakout example

Fanout Pattern – When adding fanouts to the BGA, enabling routing on the inner layers, the pattern may vary considerably depending on the layer stackup, via model, and pin density. The pattern may range from simple quadrant-matrix to a set of complex alternating arrangements. Using the appropriate fanout pattern will make a significant difference on the success of breakout and routing of the BGA.

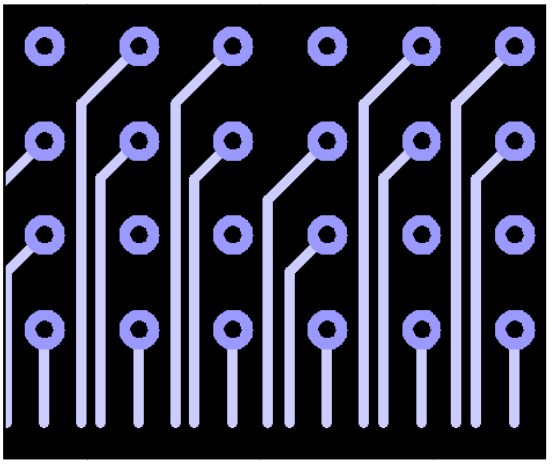


Figure 1-3: Simple matrix fanout pattern

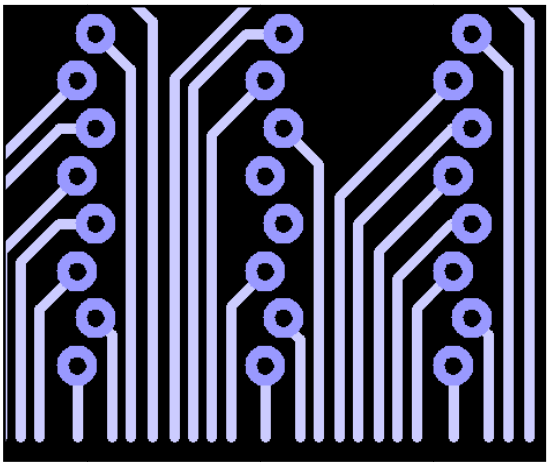


Figure 1-4: Shifted fanouts with more space for escape traces

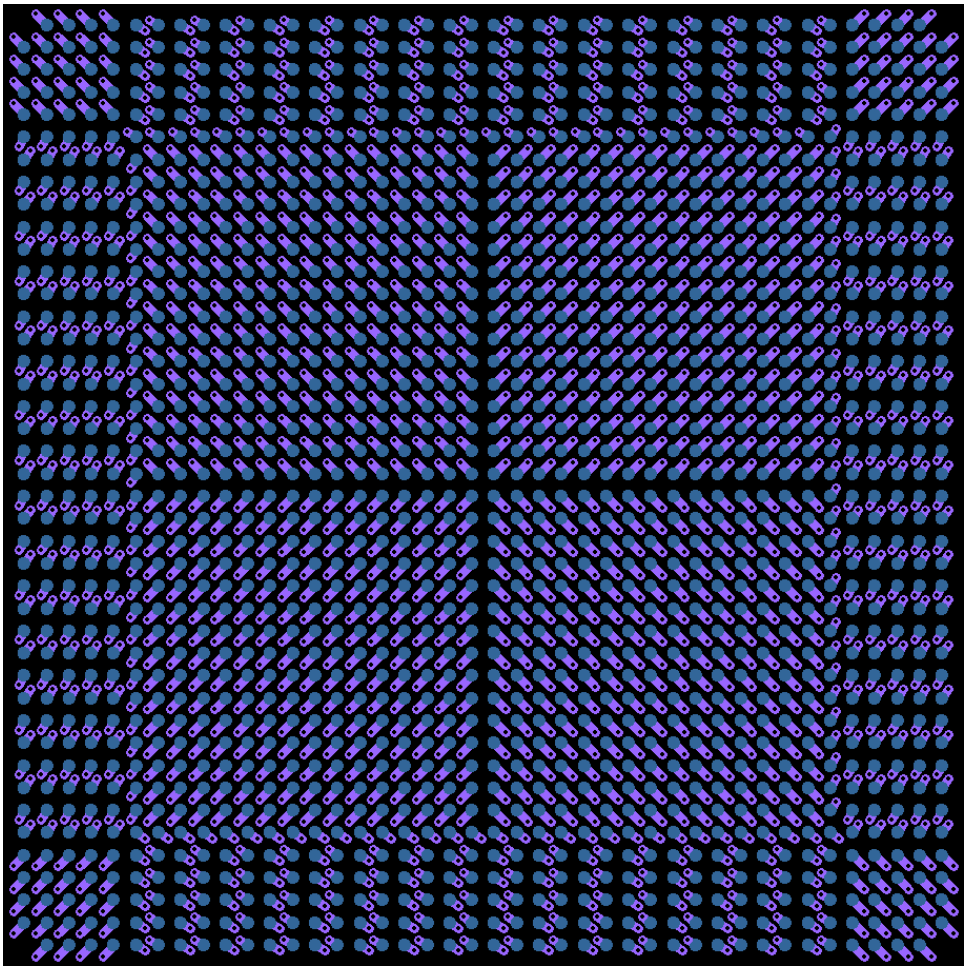


Figure 1-5: Multiple fanout patterns using blind, buried and through vias

Via Types

Through-Via – A via that extends from the top to the bottom of the board.

Through-vias are usually mechanically drilled and require an aspect ratio of 10/1 (length to hole diameter) for acceptable yields – often an aspect ratio of 8/1 is defined as the goal. It is usually larger than any other type of via, and as such, restricts routing space compared to smaller via types.

Blind-Via – A via that begins on an outer layer and ends on an inner layer.

Usually it will span 2-3 layers; however, there are no layer span restrictions except for those imposed by keeping the aspect ratio below 1/1 (length to hole diameter). The term is used to describe vias that extend from an outer layer to an inner layer in a sequentially laminated stackup (simply called blind-vias) and an HDI buildup stackup (called blind micro-vias).

Buried-Via – This type of via starts and ends on an inner layer.

The buried-via is used in combination with blind-vias in a sequentially laminated stackup, and micro-vias in an HDI buildup stackup.

Micro-Via – This via has a hole diameter less than or equal to 0.15mm (6^{th}).

Generally it is laser drilled. Micro-vias may be a blind-via or buried-via and are used in HDI stackups.

Any Layer-Via – These are short micro-vias that individually span only a pair of layers and are stacked together to result in a span between any two layers.

Stackup Types

There many different stackups using different via spans, via types, layer counts, and materials. Most stackups in production fall into these categories: laminated with through-vias, laminated with blind and buried-

vias, and HDI buildup with micro-vias. The most common stackups are discussed in terms of route density, cost, signal integrity, and power integrity in Chapter 3, “Layer Stackups”.

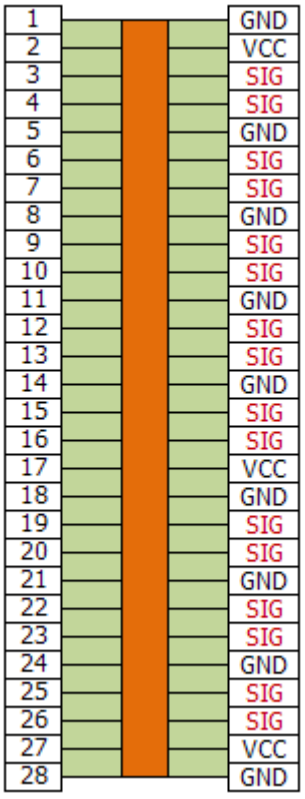


Figure 1-6: Laminated with through-vias

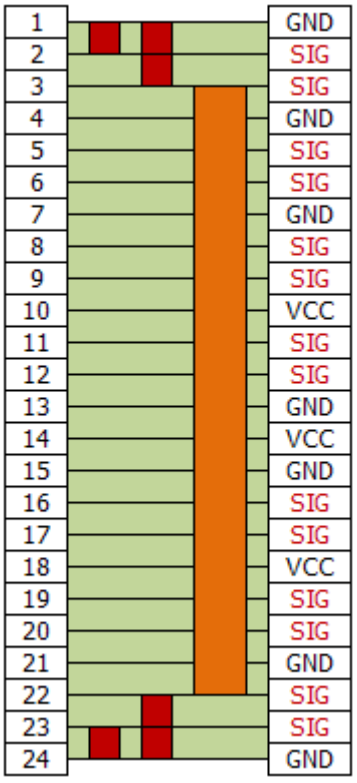


Figure 1-7: Laminated with blind and buried-vias
Red = Blind-via, Orange = Buried-via

HDI Buildup with Micro-Vias – There are many variations of HDI of which here are a few:

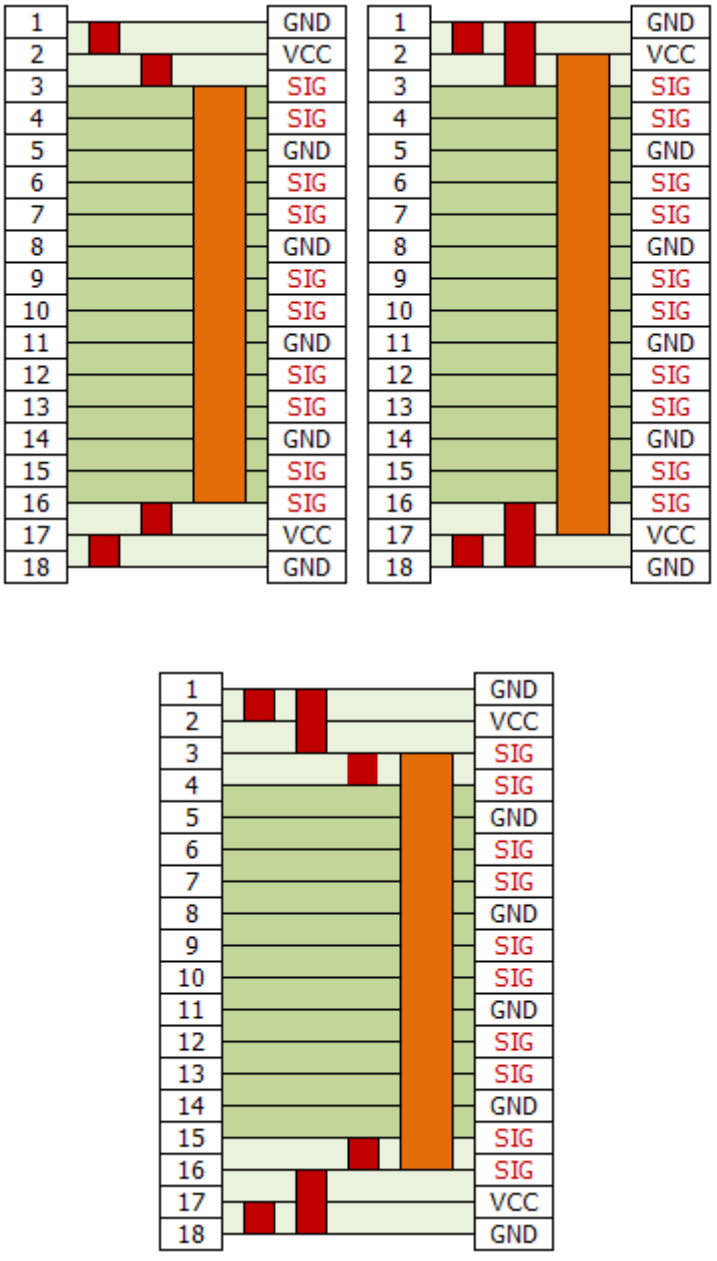


Figure 1-8: HDI Variations
Red = Micro-via, Orange = Buried-via

NSEW Breakout – North, South, East, and West routing of the escape traces. This means the escape traces are routed in all four directions on the same layer.

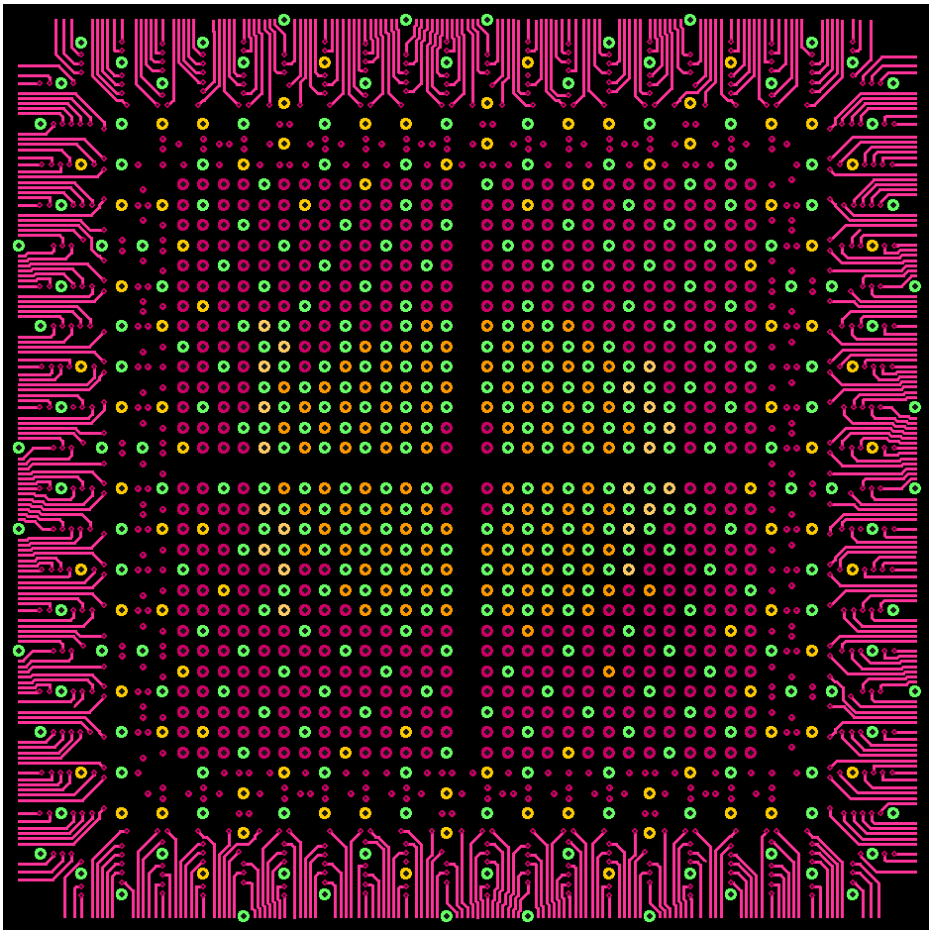


Figure 1-9: NSEW escape traces

Layer Biased Breakout – The escape traces are routed in the direction of the layer bias as opposed to NSEW routing. Escape traces are also routed in the direction of the connection according to the layer bias.

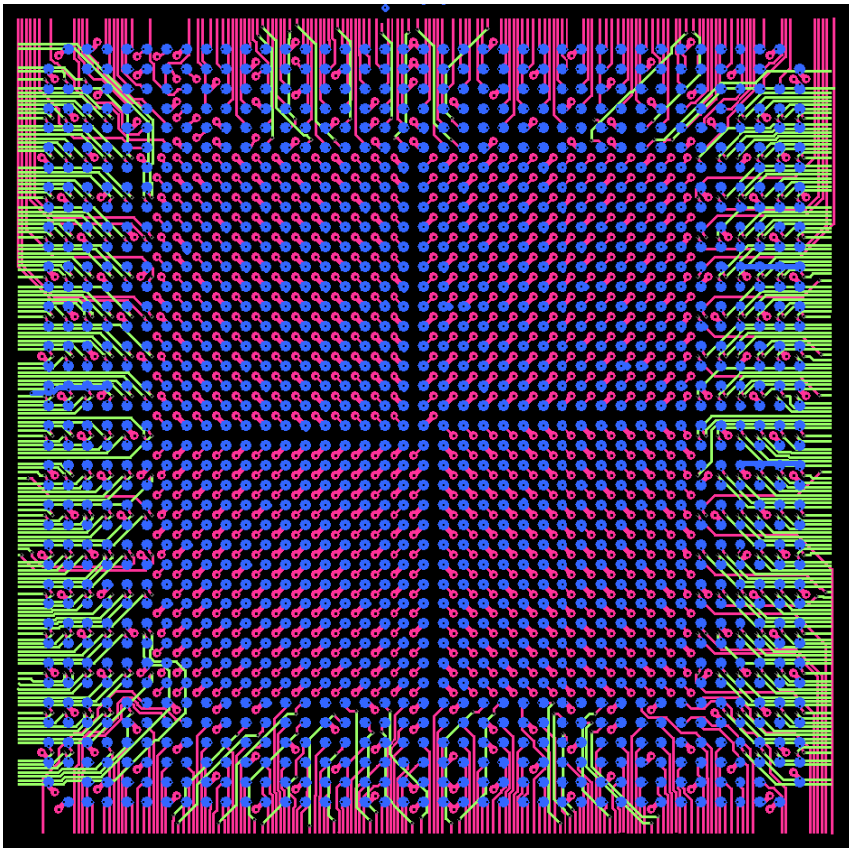


Figure 1-10: Layer biased breakouts

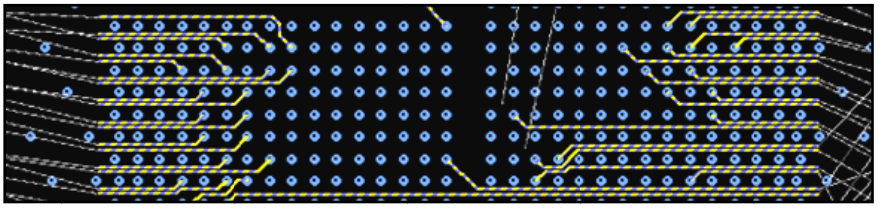


Figure 1-11: Layer biased breakouts with escapes in direction of netlines

The Problem

The increasing pin-count and decreasing pin pitch of BGAs amplify already difficult design problems. Maintaining signal integrity at high performance levels and reducing fabrication costs are arguably the two most important requirements. Unfortunately, these requirements are conflicting. Reducing crosstalk is generally accomplished by increasing the space between conductors which can increase layer count, plus routing dense BGA packages require smaller design rules and more layers. Smaller features and increasing layers contribute significantly to board cost. This is nothing new; yet further miniaturization of BGA packages will make it even more difficult to maintain performance and cost goals.

Many PCB designers who are designing with large pin-count BGAs (over 1500 pins) claim that the breakout of the device is the greatest contributor to increased number of PCB layers. An effective breakout solution will provide the foundation for layer reduction. I use the phrase “BGA breakout” to describe the method of applying a fanout solution and routing escape traces from those fanouts to the perimeter of the device prior to general routing of the PCB.

Why have breakouts? Why not just route the device without breakouts? The answer is simple. If the BGA device has too many pins in a dense array, the only way to minimize the number of layers is to utilize all the available space inside the component area with a pattern of fanouts and breakout traces. Routing such a device without an effective pattern will certainly waste space and require more layers.

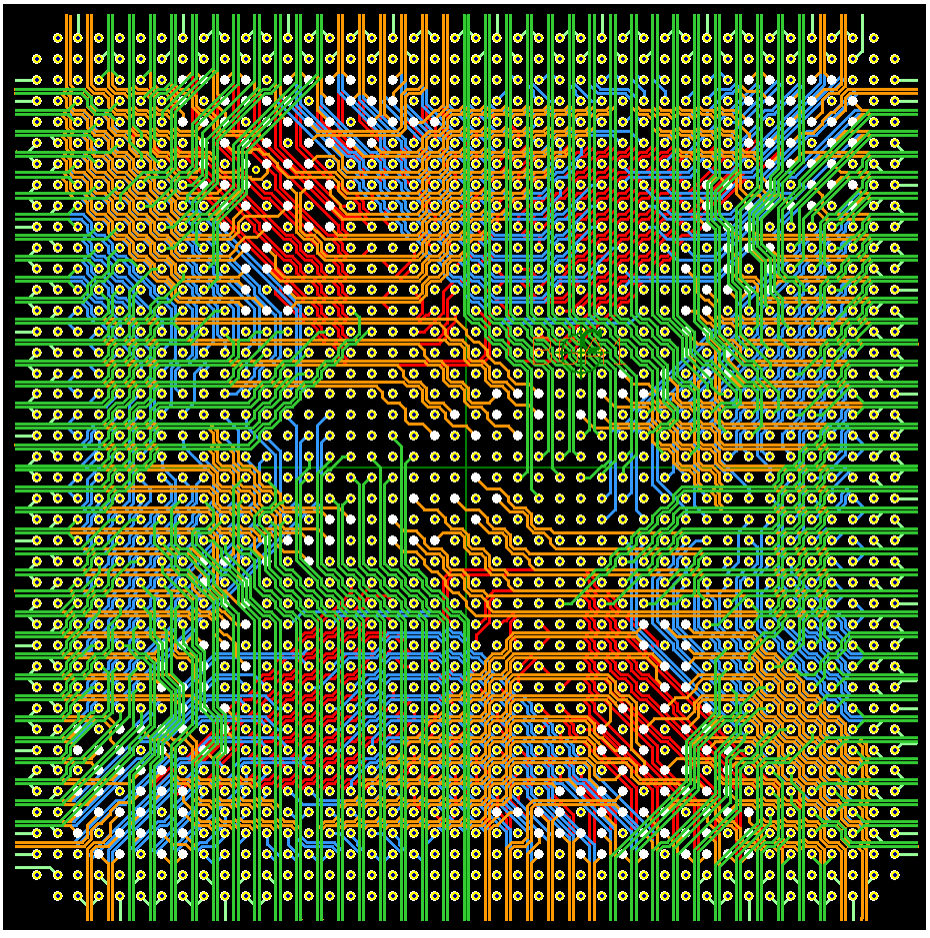


Figure 1-12: BGA breakout - 1760 Pins, 1mm pitch, fanout vias, and traces on multiple layers

Not all BGAs present a routing challenge. Low pin-count devices (less than 800 pins), even with a pin-pitch of less than 0.8 mm, do not present a significant breakout problem and are usually routed without a breakout method. This means the pins are generally accessible and can be routed with a reasonable number of layers. The high pin-count devices (over 1500 pins) with a pin-pitch of 1mm or less require a strategy for getting the traces out of the array. Without a breakout strategy, the layer count will be excessive thus affecting the fabrication cost and reliability of the PCB.

Additional factors complicate the breakout process. To attain the performance and cost goals, these items must be defined and managed properly and in concert with each other.

- Layer Stackup
- Via Models
- Design Rules
- Signal Integrity
- Power Integrity

Layer Stackup - Early in the design process, the layer stackup will be defined. If the board has large and dense BGAs, High Density Interconnect (HDI) with a laminated core and buildup layers may be required. There are many different options using various materials and processes. Cost and reliability are usually the primary factors in determining the stackup and you will have to balance the tradeoff between layer count and fabrication processes to reach your goals.

Via Models - Within the context of any given layer stackup, you have many options regarding via models. The decision on which type of via to use (thru, laminated blind and buried or HDI micro vias) will likely be driven by the density of the board and the BGA packages. There are also options regarding vias inside pads and stacking that affect cost. In addition to this, board fabricators tend to focus on a limited set of processes thereby limiting your choice of vendors, depending on the technology you desire. From the design point of view, choosing the appropriate via models directly impacts the route-ability of the board.

Design Rules - PCB fabricators continue to find methods that allow for further miniaturization and increased reliability. The design rules have to balance the tradeoffs between cost, signal integrity, and route-ability.

Signal Integrity - Although the fabricators continue to improve their processes and produce reliable boards with smaller and features and clearances, maintaining signal integrity at high performance levels usually

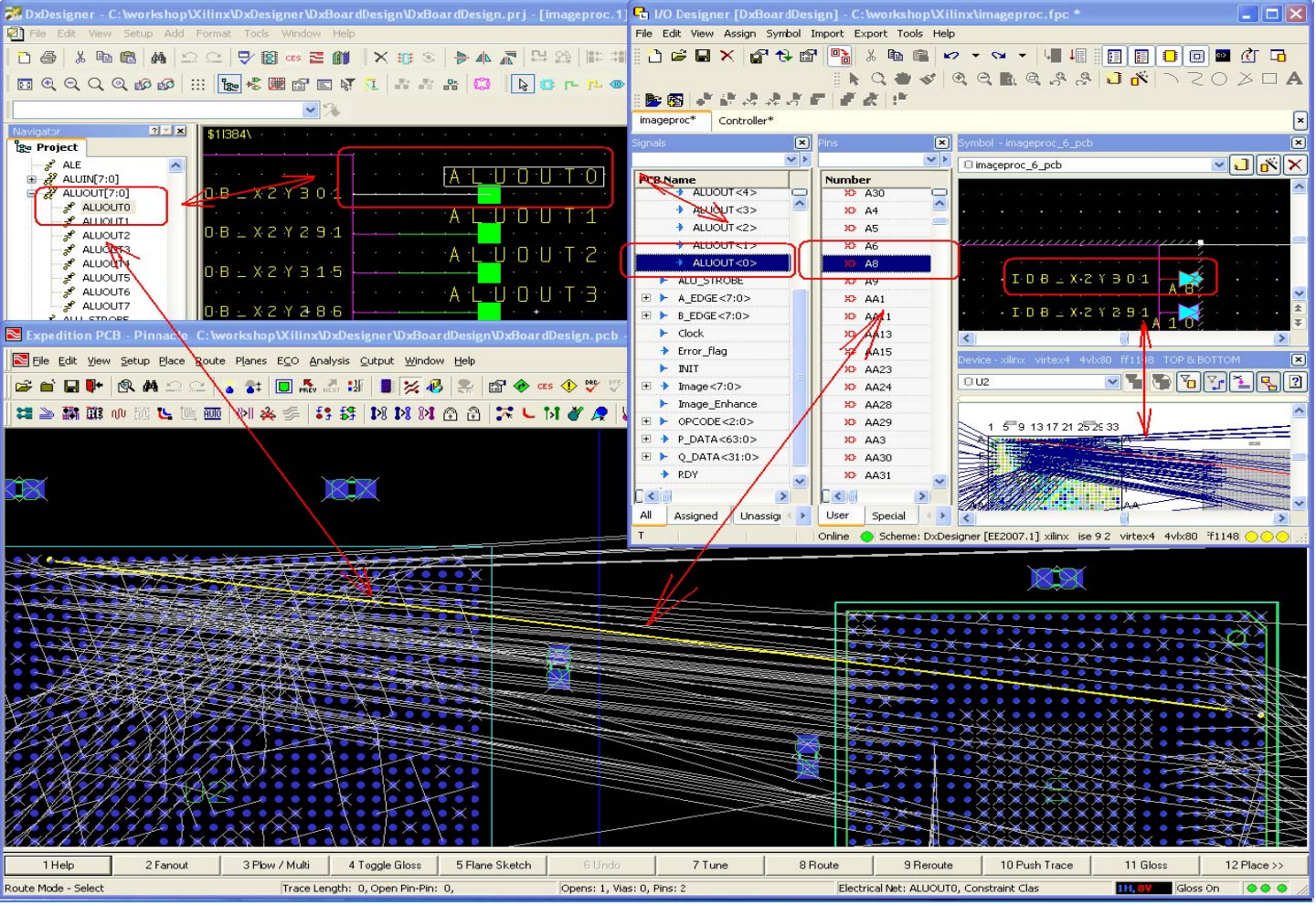
requires greater spacing between critical nets, especially to manage crosstalk effects at higher speeds. This conflict is exasperated with high pin-count and dense BGAs.

Choosing appropriate layer stackups and via models will not only improve route-ability but signal integrity as well.

Power Integrity - Managing power distribution effectively for large pin-count BGAs is a challenge and is significantly impacted by the layer stackup. There are methods that can minimize the number decoupling capacitors required, thereby increasing the space available for signal routing.

Solutions

Because of the high number of variables with any PCB design, it is not possible to have a single BGA breakout solution for all situations. It is possible however, to develop solutions within reasonable sets of variables. This book offers principles for breakouts that may be applied as appropriate within the constraints of your own designs. It is my hope that in addition to finding useful ideas and methods herein, your imagination will be stirred to discover unique solutions.



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Chapter Two - BGA Packages

The good news is that BGA technology enables high pin-count FPGAs, ASICs, and connectors to be packaged with a very high density array of pins. The bad news is that finer pin pitches and increased pin counts are making these devices even more difficult to route. The requirement to miniaturize while increasing functionality is the most significant constant that drives change in our industry.

High Pin Counts

The current crop of BGAs with less than a 1mm pitch are not yet pushing high pin-counts and as such they can be routed fairly easily The very high pin-counts can be found in the 1mm pitch packages today and at 0.8mm in the coming years. Figure 2-1 shows a very high pin-count BGA.

In Table 2-1, the highest pin-counts for various FPGA and ASIC packages are listed.

Company	Package	Pins
.5mm Pitch		
Amkor	fcCSP	180
Actel	CS281	281
.8mm Pitch		
Quicklogic	PT-280	280
Altera	DS-484UBGA05	484
1mm Pitch		
Actel	FBGA 1152	1152
Cypress Semi	51-85179	1152
eASIC	1152-FCBGA	1152
Intel	MCH	1300
AMI Semi	1704 FFBGA	1704
Lattice Semi	1704 fcBGA	1704
Xilinx	FF1760	1760
Altera	DS-1760FBGA	1760
NEC	FCBGA 1849	1849
Fujitsu	FC_BGA	2116
Toshiba	PBGA[FC]	2304
TI	GTM (N2377)	2377

Table 2-1: High pin counts by manufacturer

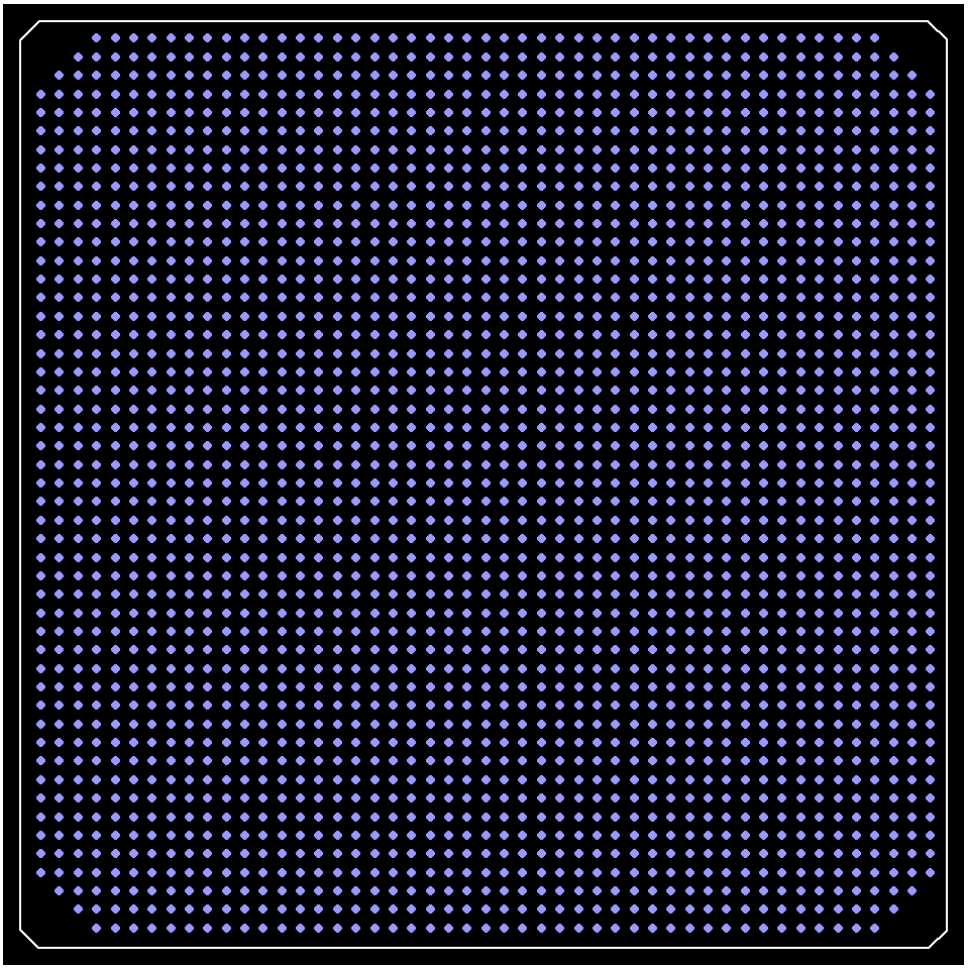


Figure 2-1: TI GTM (N2377) BGA with 2377 pins at 1mm pitch

You can immediately see that a BGA with over 2000 pins presents a daunting routing task. Of course some large percentage of the pins will be power and ground; but even figuring out a good fanout pattern for those pins so they don't block routing is a challenge. Even if 40% of the pins are for power distribution, potential for 1400 signal connections still exists.

Impact on Routing, Performance and Cost

Since the pin-counts on 0.8mm pitch BGAs is still reasonably low, the routing task is not too difficult. However there are some consequences:

- Differential Pairs – Unless the design rules in the device area are very small or innovative via patterns are used (to be described later in this book), the differential pairs must be split. Since these packages are still quite small, the split distance may not affect signal integrity.
- Potential Impedance Discontinuity – If the pin-pitch is 0.8mm or less, often a rule area is used to allow smaller trace widths and spacing within the BGA area. The width change on single-ended nets will cause an impedance discontinuity as will a change in the spacing and or trace widths of a differential pair. The question that must be answered for each design is if this change across the rule area causes any significant ringing.

For the 1mm pitch BGAs, I consider a pin-count over 1500 to be one threshold for difficult routing. In the context of laminated FR-4 boards with through-vias, the following are some of the potential problems:

- Layer Count – The sheer number of pins could require additional layers just to breakout the device. If you have multiple instances of BGAs over 1500 pins, then the route density will certainly force you to have more routing layers. Layer counts over 28 need thinner FR-4 dielectrics and de-lamination can occur at the lead-free assembly temperatures (at least 270º C).
- Via Aspect Ratio – Maintaining high fabrication yields and long-term reliability requires the via length-to-hole diameter ratio to be less than 10:1, preferably 8:1. Boards with over 28 layers make it difficult to keep the through-via size small enough to allow effective routing. As the via pad size increases, it is more likely the differential pairs will have to be split during the breakout as well.

- Nightmare of Circular Dependencies – High pin-counts dictate additional layers to route, additional layers require a larger via hole and pad size, and then larger vias reduce routing space, thus forcing additional layers. Once caught in this cycle, the best way to break out of it is to abandon through-vias and start using blind and buried-vias or HDI with applied dielectrics and micro-vias.

Greater than 2000 pins at 1mm pitch is a tipping point, especially if you have multiple instances of them on a single board as you might see in a network or emulation card. The layer count and via aspect ratio problems with laminated FR-4 boards will be even more severe with this many pins. When using blind and buried-vias or HDI micro-vias, effective fanout patterns can be used to increase route density from 24% to 36% with a corresponding layer reduction. Figure 2-2 shows increased route density on the first inner layer of a design when using blind-vias arranged in a pattern that allows for greater route density.

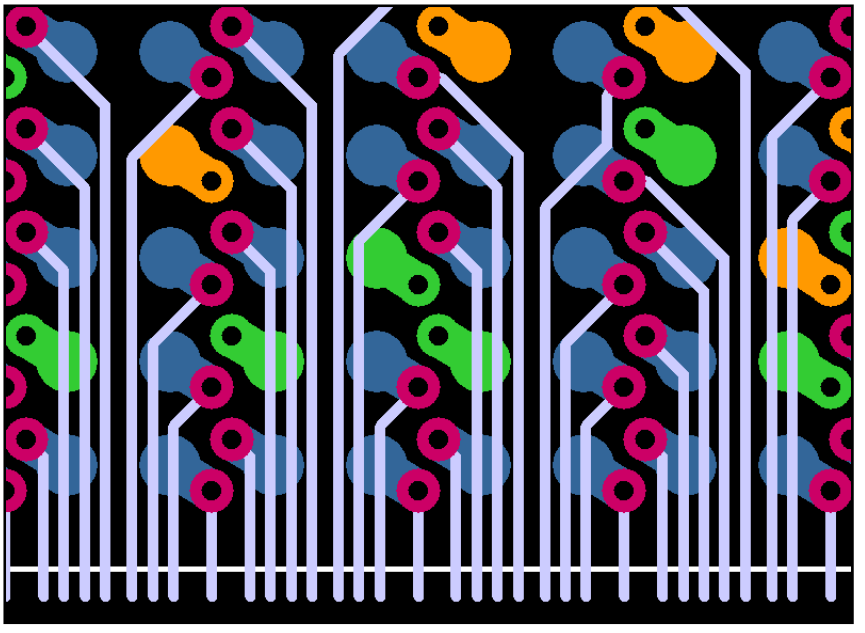


Figure 2-2: Effective fanout pattern

Off-Matrix Ball Pads

The Intel MCH (Memory Controller Hub) BGA package, which can have up to 1300 pins, is worthy of special mention. Figure 2-3 shows that the pins are positioned off the standard matrix making the routing difficult and depending on your design rules, it may require routing with any-angle traces. This is a newer package from Intel and gives us a view into the future — BGA routing isn't going to get easier anytime soon. Fortunately, PCB design software continues to be enhanced to keep pace with the evolving packaging methods.

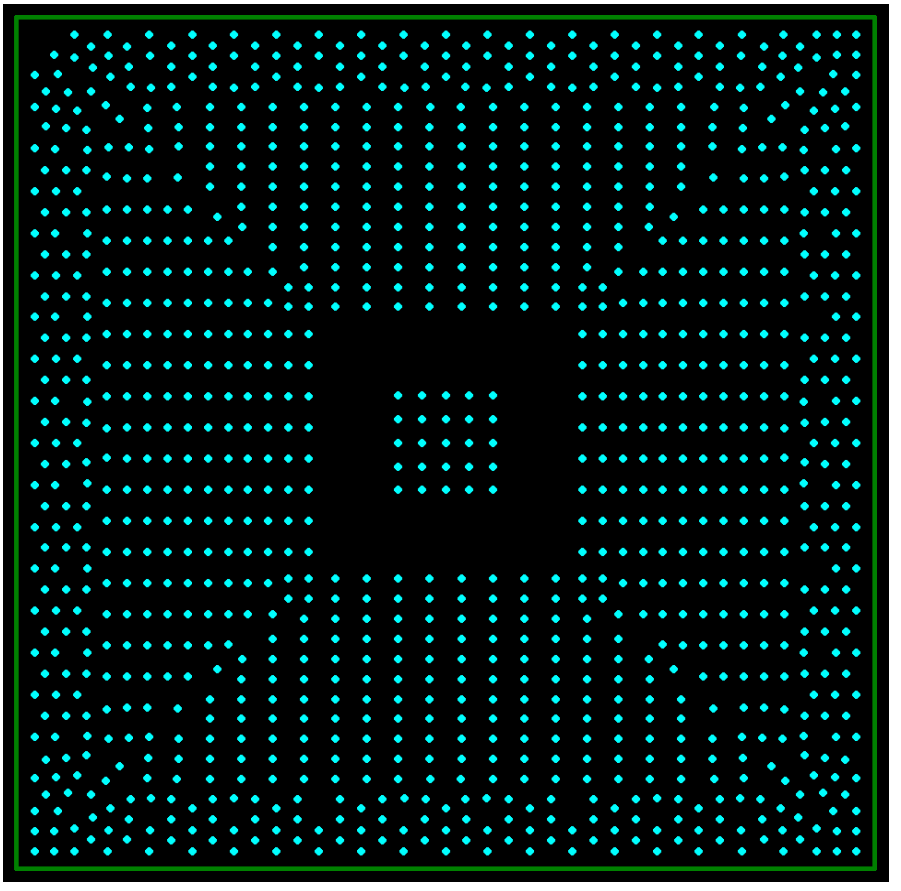


Figure 2-3: Intel MCH package

0.8mm Pin-Pitch

The next figure not a real device, it just shows what could be done at 0.8mm pin-pitch in the same size package as the current 1mm pitch Virtex-5. It could contain 3025 pins.

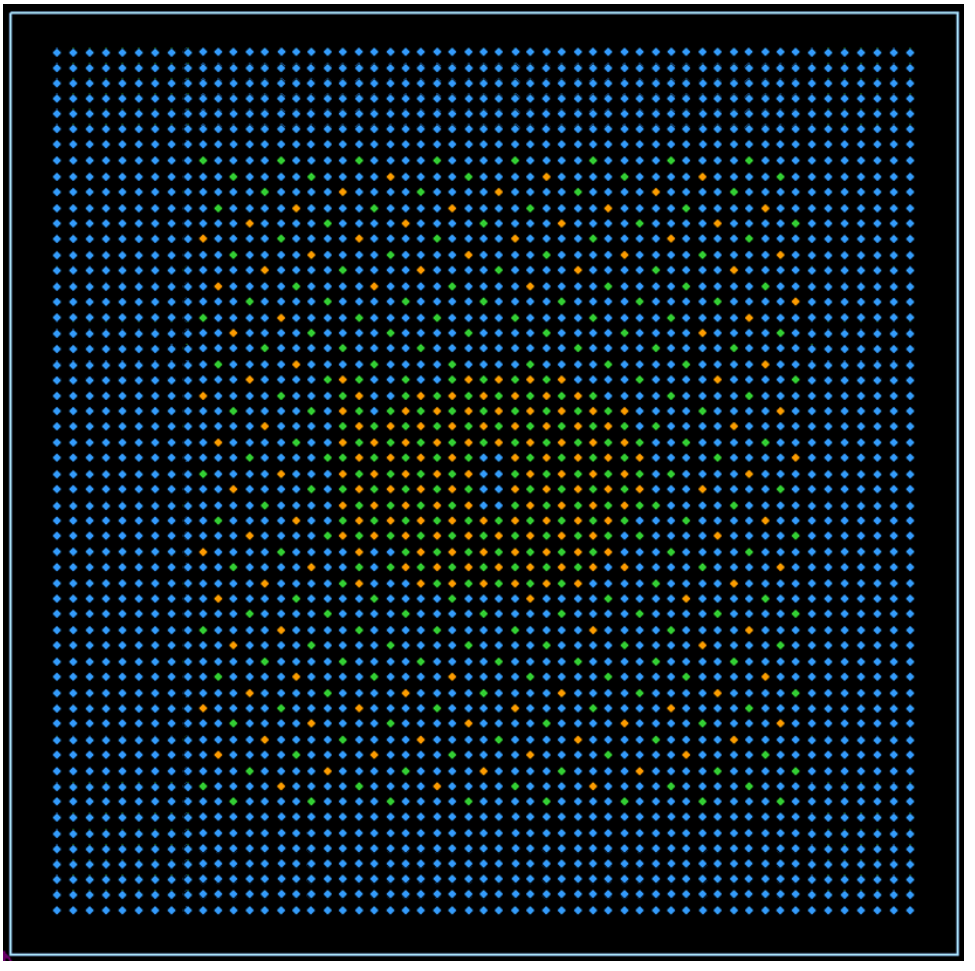
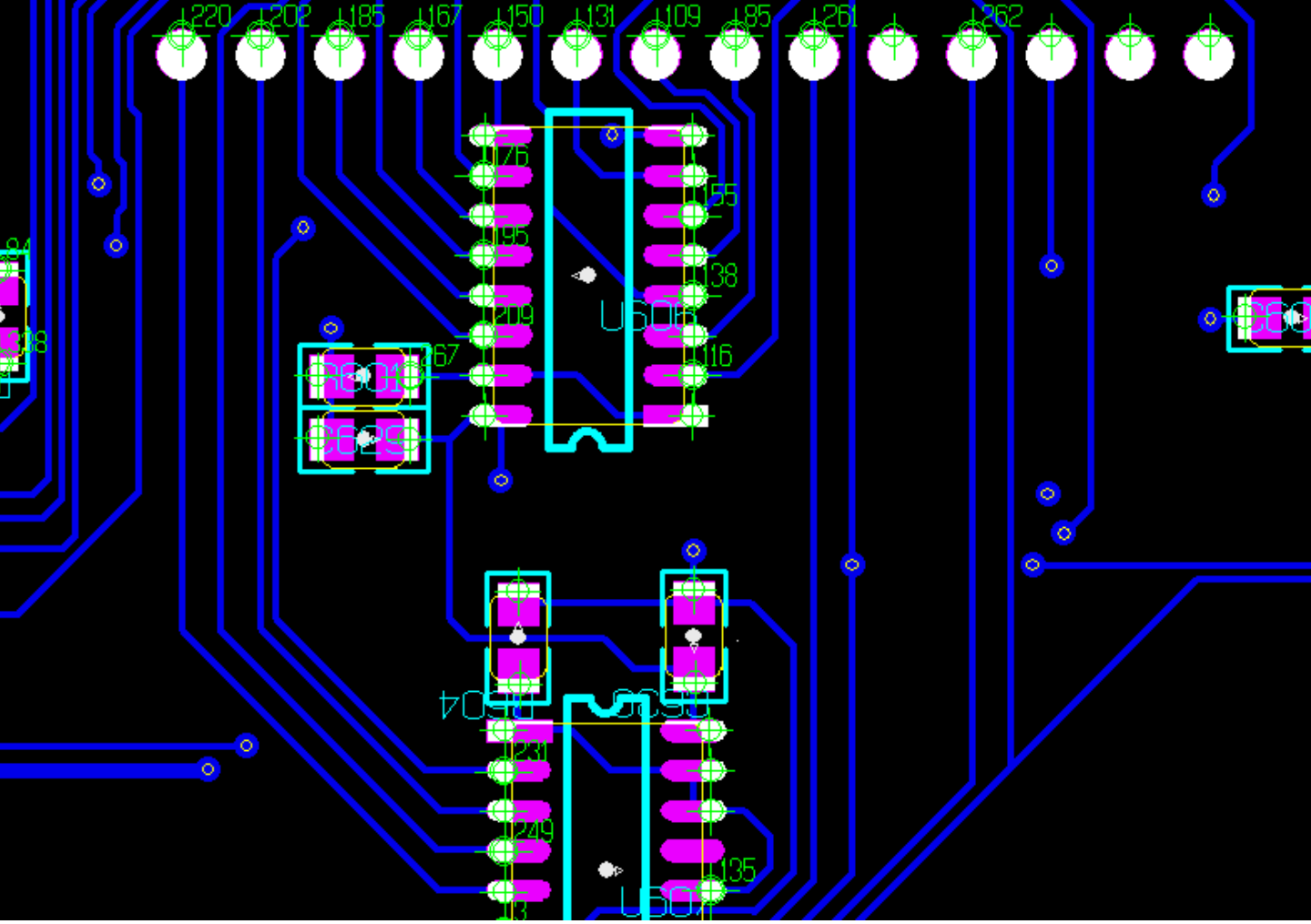


Figure 2-4: 3025 pins at 0.8mm pitch (not real)

If you took the TI GTM (N2377) package and packed the pins in at 0.8mm instead of 1mm, it could have 3721 pins.

The Near Future

In order to increase functionality and continue to miniaturize, more pins will be added into smaller packages. I predict within the next 3 years we will see an ASIC or FPGA package at 0.8mm pitch and more than 2000 pins. This type of device presents more than a threshold; it is a tipping point because it will require the use of HDI. Managing signal integrity, maintaining fabrication yields and low cost will simply be impossible with the standard through-via laminate. Within 5 years, use of this kind of package will be common.



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Chapter Three - HDI Layer Stackups

This chapter is intended to help designers who are creating large dense PCBs with multiple high pin-count BGAs and are finding standard laminate stackups inadequate to meet cost and performance goals. Maybe your laminate board has too many layers, or the feature sizes prevent effective breakout and routing of the BGAs. High Density Interconnect (HDI) stackups are a viable alternative and can provide lower cost with higher performance if designed properly.

From the information in this book, you should be able to determine which stackup methodology is best for your designs and why the alternatives may not be appropriate. If you just want to find out which stackups are recommended herein, you can just skip to the last section. However, to best understand the reasons why these stackups are recommended and the impact of choosing one of the alternatives, then it would be beneficial to read the whole chapter.

Defining the appropriate stackup should be considered as one of the most important aspects of initial design work. Since there are so many variables involved with stackups, this chapter will focus on stackups that enable effective board design with multiple large and dense BGAs. Typically this includes boards for the networking, computer, server and emulation marketplaces. It is assumed that even though handheld devices and consumer electronic products will likely have dense BGAs, it is unusual for them to have multiple instances exceeding 1500 pins and as such do not present the kind of design challenges being addressed in this book.

Fabrication Vendors

Stackups should be designed in conjunction with the fabrication vendor to minimize cost and meet signal integrity requirements. The board fabrication vendor ultimately builds a board that meets your requirements

for cost, reliability, overall thickness, and impedance control. There may be additional requirements related to plating and specific materials. As a general rule, the vendor will adjust all the stackup variables as needed during their process to meet your goals.

The most productive method is to collaborate with the vendor on a stackup prior to designing the board. That way, the fabricator will be able to make minimal adjustments to meet your goals.

A good example of these adjustments is impedance control. Regardless of how carefully the stackup is defined with trace widths, material choices, dielectric and copper thicknesses, the fabrication process is not so exact. Each vendor has different equipment and methods. The lamination process shrinks the dielectrics and materials may be changed if not in stock or readily available. The tolerances in all areas add up and ultimately a reliable vendor has to make the right combination of adjustments in-process so that when measuring impedance on the test coupon, it fulfills your spec. Trace widths and material thicknesses may change a little but if the measured impedance is within spec then it really doesn't matter what changes were made – as long as the other requirements are not fatally compromised of course.

If the initial stackup is not defined properly, minor acceptable adjustments by the fabrication vendor will not be adequate to fulfill your overall requirements. A wise and experienced vendor will not accept the risk of making major changes to the design data.

Dependencies

Unfortunately there are many dependencies, some of them circular when defining a stackup. The process of determining an effective stackup can be overwhelming. Forgive the next meandering and confusing paragraph, but it is a good example of the difficult process of deciding which variables need to be compromised or emphasized to reach your goals:

It is necessary to reduce the layer count to keep costs down. It is also required to have an adequate number of layers to route the board. On some of the largest PCBs, there are well over ten thousand nets to route. To control crosstalk, increase the spacing between traces which requires more layers. Also consider running the differential pairs together through the via array under the BGA, which means the via must be small enough to not only allow the diff pair to run together, but still space the traces far enough apart to attain the desired coupling. These traces also need to be the appropriate width in correlation to the thickness of the dielectrics and their material attributes to provide the desired impedance. But if you have too many layers, then the via needs to be bigger otherwise the aspect ratio of hole size to length becomes too great to drill with a good yield. If you make the via hole smaller, you can enable more dense routing but may sacrifice manufacturing yields. If you make the via hole larger, you may have to split the differential pairs through the via array and you will impact signal integrity and require more layers to breakout the BGA. If you have more layers, you will need an even larger via. These factors may require you to develop special fanout patterns in the context of the stackup to support the manufacturing, signal integrity and routing goals. This paragraph just touches a few of the dependencies; yet even so, it describes a daunting task.

Where do you begin? A number of example stackups will be presented with the advantages and disadvantages itemized along with a basic description of which via models, design rules work best. Some signal and power integrity concerns will also be discussed.

Overview of Stackup Types

In the context of boards that have high pin-count BGAs, there are three stackup types of interest:

1. **Standard Lamination with Through Vias**

   Advantages
   - Low cost (until layer count becomes too high)
   - Simple via models
   - Simple dielectrics – Primarily FR-4
   - Mature process, “everybody does it”
   - High reliability (until layer count becomes too high)

   Disadvantages
   - If layer count becomes too high
     - Fewer fabrication vendors can obtain good yields, costs skyrocket
     - Board can delaminate under high temperatures required for ROHS lead-free soldering
   - Via has to be large, reducing route-ability, increasing layers
   - Difficult to implement for BGA pin-pitches below 1mm
   - Through hole vias capacitively couple to every plane layer and signal losses increase with thickness
   - Long via stubs create impedance mismatches, reflections on single-ended nets
   - Large via pads often force differential pairs to be split under BGAs

   Notes
   - There are a number of tipping points where standard lamination with through vias is not viable
   - Once the board is over 28 layers, it becomes difficult to manufacture with acceptable yields and therefore can become cost prohibitive.
   - If the board is over 28 layers, the dielectrics can be so thin that de-lamination can occur under the higher temperatures required for lead-free soldering.
   - Generally when using a few BGAs with less than 1500 pins and a 1mm pin-pitch, the breakout and routing of these devices is feasible using through vias.

- However, if you have a large number these on a single design, then the route density may force the layer count up high enough to limit the effectiveness of this stackup.
- If you have multiple BGAs with over 1500 pins and 0.8mm pin-pitch (or less) it is likely that through vias will make it very difficult to route these devices.
- When the thickness of the board due to the number of layers forces the via to be so large that it inhibits route-ability.
- Via length to hole diameter should be <10x otherwise reliability declines significantly
- Pad diameter should be hole size plus 0.01 inch
- If the via pad is so large that it prevents differential pairs or multiple single-ended traces from being routed between the BGA via arrays, then more layers will be required to complete the routing.
- Vias can be shifted off the standard matrix under BGAs; however, with through vias, not much is gained.

2. Sequential Lamination with Blind and Buried Vias

Advantages

- Potentially shorter via stubs
- Fairly simple via models
- Generally smaller vias than required for through hole vias
    - Minimum size for mechanically drilled vias are the same as for standard laminate; however blind and buried vias will likely have a smaller aspect ratio enabling more use of minimum via hole size, which is 8th.
- Simple dielectrics – Primarily FR-4
- Effective use of blind and buried vias opens up routing channels, potential for fewer layers

Disadvantages

- Not a widely adopted process, more and more fabricators do HDI instead
- Minimum size for drilled vias is 8th

- Costs more than through hole laminated, yet minimum trace widths are still the same
- Practical reliability limits the number of sequential laminations to 2 or 3

Notes

- Sequentially laminated boards have the same tipping points as standard laminates; however, since the via length to hole size aspect ratio will be less and pad sizes can be smaller, route-ability improves and it is less likely that the design would exceed 28 layers.
- Since the feature sizes for traces can vias are still the same as with standard laminate, designing with multiple large BGAs of < 1mm is very difficult.

3. Buildup with Micro-Vias (HDI)

Advantages

- Smaller feature sizes for vias and traces enables higher density and fewer layers
- Effective use of micro-vias opens up routing channels, potential for fewer layers
- Only practical way to design with multiple large BGAs having <0.8 mm pitch
- Lowest cost for high density boards
- Improved signal and power integrity with appropriate stackup definition
- Materials do well in processes requiring ROHS
- Newer materials available with higher performance and lower costs, which are not suitable for standard or sequential lamination

Disadvantages

- Complex via models with many variations and still evolving
- Complex stackup definition
- Effective design methods on large dense designs have not been widely understood and documentation is sparse
- Predictive design guides and cost estimates not yet available

- Although HDI fabrication is pervasive in PAC Rim and China, North America slow to adopt

Notes

- HDI is the best alternative to high layer-count and expensive standard laminate or sequentially laminated boards.
- The trend is for higher pin-count and finer pin-pitch. The tipping point will occur when the >1500 pin BGAs use a .8mm pitch.
- The only way to effectively breakout and route multiple instances of these devices on a single board will be with the smaller HDI feature sizes.
- HDI currently dominates the fabrication technology for handheld and consumer electronics. For large board designs, it will continue to grow.

HDI Stackup Details

This section is provided as a reference describing the relevant HDI stackup information based on the Institute of Printed Circuits (IPC) standard.

In this section Types I, II, and III are described. Type III is the recommended configuration for large dense boards with multiple high pin-count BGAs.

IPC information that may be useful to you:

http://www.ipc.org

IPC/JPCA-2315
Design Guide for High Density Interconnects and Micro-vias

IPC/JPCA-4104
Specification for High Density Interconnect (HDI) and Microvia Materials

HDI Type I

This construction uses both micro-vias and through-vias in a structure consisting of a laminated core and a single micro-via layer on at least one side.

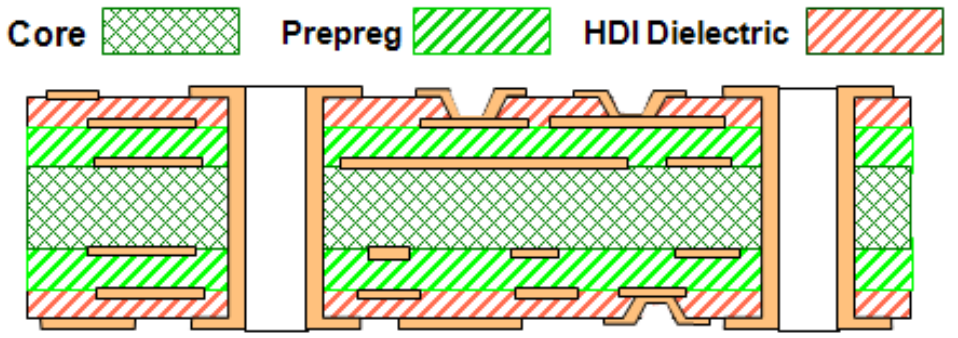


Figure 3-1: IPC HDI Type I

Notes

- The number of layers in the laminated core varies and is limited by two factors
    - The through-via should have an aspect ratio (total length to hole diameter) less than 10x to maintain reasonable reliability.
    - If the FR-4 dielectrics become too thin, they will delaminate under higher temperatures required for lead-free soldering.

Recommendations

- In the context of large dense boards with multiple high pin-count BGAs, this stackup will not be significantly better than laminate.
    - The through via pads will need to be large.
    - Using only a single micro-via layer will limit the ability to benefit from the smaller via and trace feature sizes.

HDI Type II

This construction uses micro-vias, buried-vias, and may have through-vias.

- There is a single micro-via layer on at least one side.
- Via holes are drilled in a laminated core and become buried when the dielectric material is added for the micro-vias.
- Micro-vias are staggered from other micro-vias and may be stacked or staggered relative to the buried vias.

Additional Notes

- See Type I note above on limiting the number of laminated core layers which applies to all variations of Type II through and buried vias.

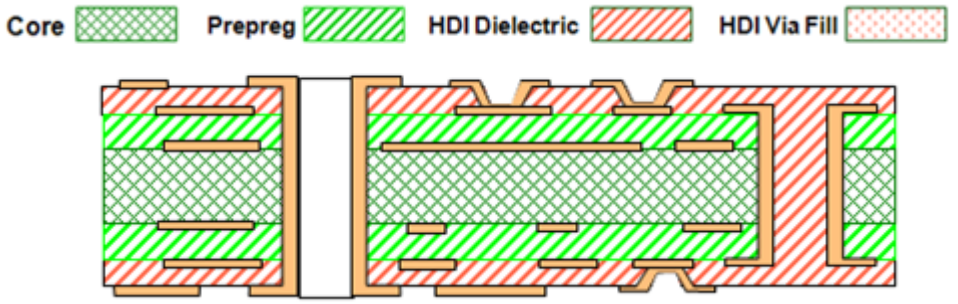


Figure 3-2: IPC Type II

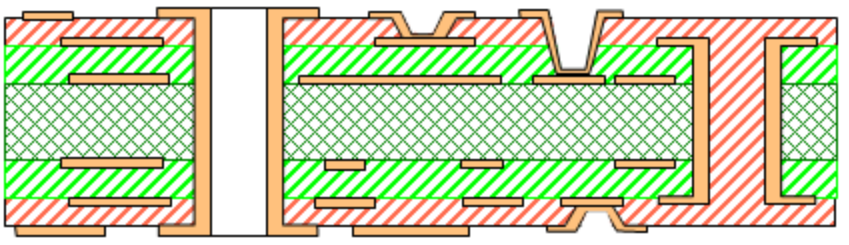


Figure 3-3: IPC Type II, variable-depth micro-vias

The variable-depth micro-vias can be in the form of skip-vias that connect only on the start and end layers.

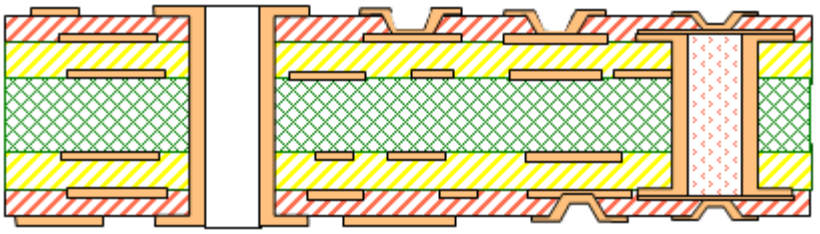


Figure 3-4: IPC Type II, stacked vias

Recommendations

- In the context of large dense boards with multiple high pin-count BGAs, this stackup is better than Type I; however, is not adequate for the more difficult designs.
    - Using buried vias instead of the through vias is a significant advantage.
    - Using only a single micro-via layer span will limit the ability to benefit from the smaller via and trace feature sizes.
    - The single micro-via layer span also restricts the viability of using the outer layers for a GND plane. Having only one buildup layer for routing traces isn't nearly as effective as two.

HDI Type III

This construction uses micro-vias, buried vias, and may have through vias.

- There are at least two micro-via layers on at least one side of the board.
- Via holes are drilled in a laminated core and become buried when the dielectric material is added for the micro-vias.
- Micro-vias may be staggered or stacked with themselves and the buried vias.

Additional Notes

- See Type I note above on limiting the number of laminated core layers which applies to all variations of Type III through and buried vias.

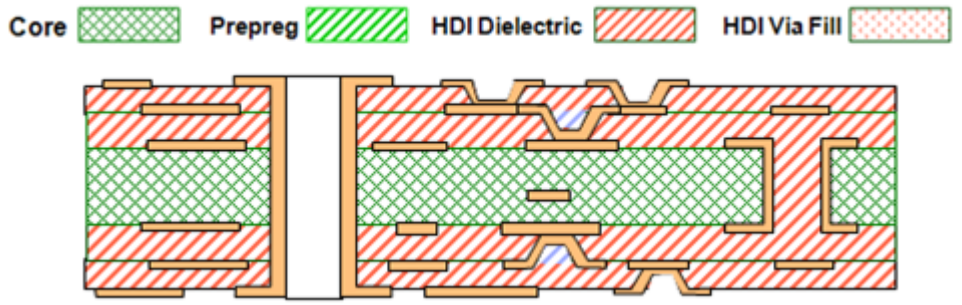


Figure 3-5: IPC Type III

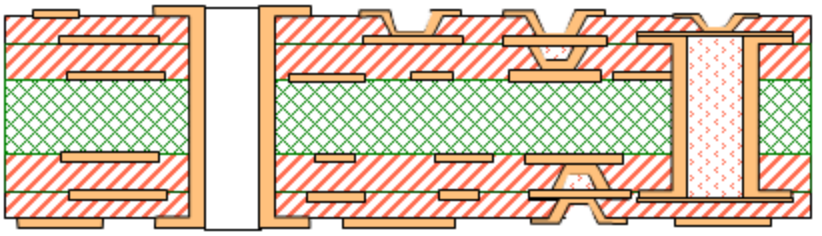


Figure 3-6: IPC Type III, stacked vias

Recommendations

- Type III HDI is the best stackup configuration for large dense boards with multiple high pin-count BGAs.
    - With two micro-via layers there is considerable routing area available using the smaller via and trace feature sizes.
    - Using the outer layers for a GND plane is feasible because there are still enough micro-via layers available for signal routing.
    - Using stacked vias will allow for greater route density; however, the cost will be higher.

HDI Type IV, V, VI

These additional HDI Types are defined in the IPC-2315 specification; however, they are not presented here simply because they are more expensive to fabricate and are probably not necessary for large dense PCBs with BGA breakout and routing challenges.

Via Models

HDI Type III accommodates numerous via models and spans. Ultimately the via model that suits your design best will be driven by finding the least expensive method that will still enable adequate route density within the constraints of signal integrity.

The graphic below represents some of the via models that may be used in HDI Type III.

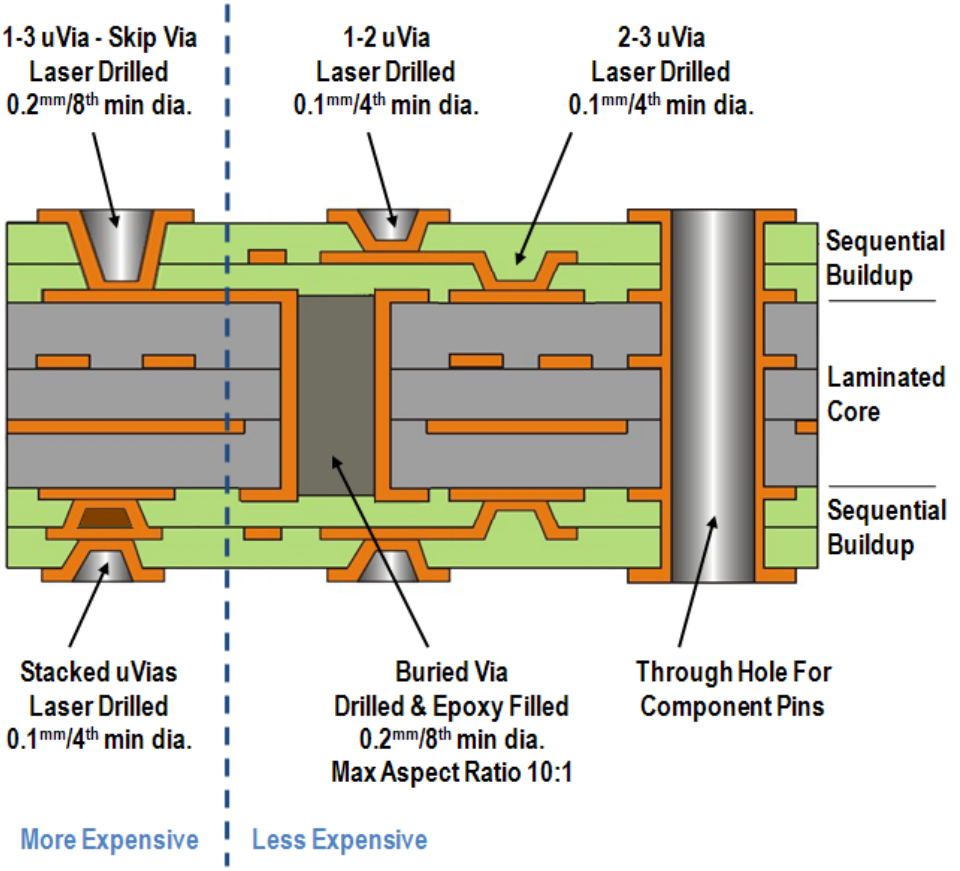


Figure 3-7: Type III via model examples

- Skip Vias – This via model is effective for transitioning layers (because it emulates the stacked via); however it is not as efficient as stacked vias for route space due to the fact that the minimum diameter is 8th.
- Buried-vias – As a general rule, all unused pads on the buried-vias should be removed. This will significantly reduce the crosstalk.
- Micro-via Pad Sizes – Although the pad size will vary by fabricator, using a pad .15mm (6th) larger than the hole is adequate.
- Via Aspect Ratio – Hole length to diameter: Micro-vias 5:1, buried-vias 10:1

Alternative Via Spans

- Extending Buried-Vias
  As shown below, you can extend the buried-via into the first micro-via layer. This method can eliminate one drilling setup step.

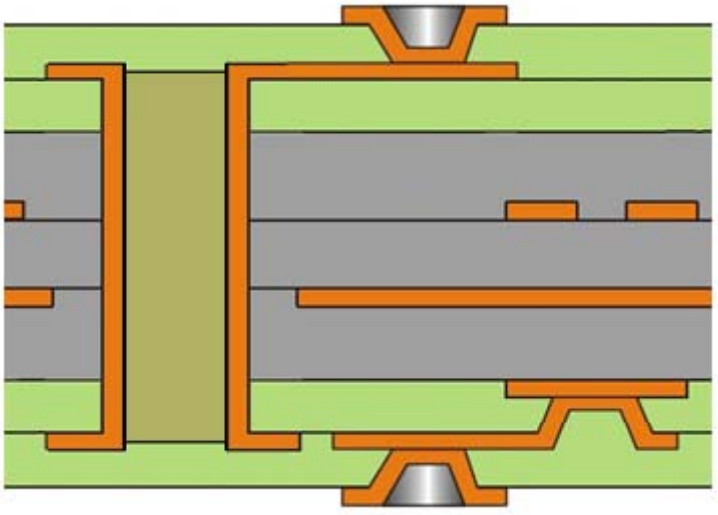


Figure 3-8: Extended buried-via

Advantages

- If you have power and ground nets that need to extend all the way through the board, using the extended buried-via requires less space.

Disadvantages

- Single-ended nets that use the extended blind via may suffer from additional via-stub effects; however, the additional stub length may be insignificant depending on the frequency.
- Depending on the fabricator, the cost of extending the buried-via may be slightly more than just having the buried-via in the laminated core.

- Stacking Micro-Vias and Buried-Vias
  As shown below, the micro-vias may be stacked with themselves and/or with the buried-vias.

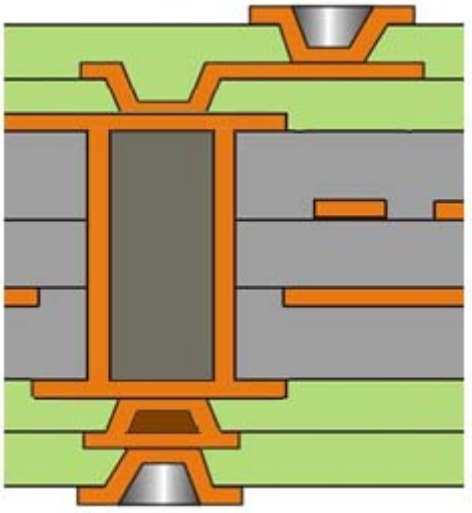


Figure 3-9: Stacked vias

Advantages

- If you have power and ground nets that need to extend all the way through the board, using the extended buried-via uses the minimum space.
- Using stacked vias enables the most flexible and efficient via configuration for routing.

Disadvantages

- Stacking vias generally costs more due to additional steps required to ensure a good connection between the vias.

Plane Layer Assignments

In the context of an HDI Type III stackup, location of the planes will impact your power distribution and integrity along with signal integrity. The

appropriate location of planes is a much deeper and more complicated subject than can be addressed in this book; however, certain methodologies are recognized as effective and will be described at a high level herein.

In the stackups shown, the number of layers in the laminated core is variable of course. Sixteen layers is just convenient for the purpose of showing plane layer assignments graphically.

- Outer Layer GND
  A stackup such as the one pictured is typical when GND is assigned to the outer layers.

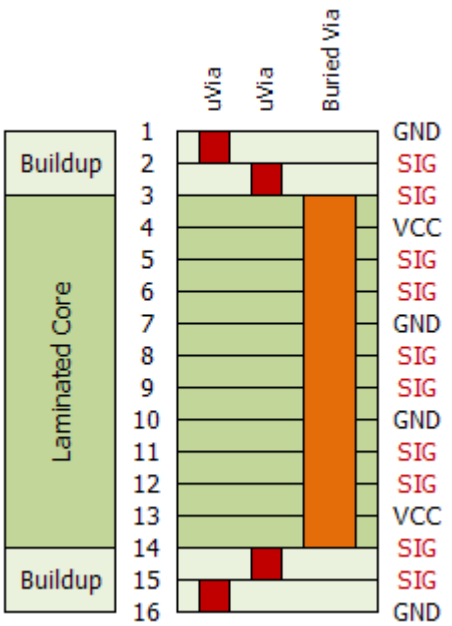


Figure 3-10: Outer layer GND

Advantages

- GND on the outer layers provide an excellent EMI shield.
- If the bypass capacitors for the BGA are placed on the same layer as the BGA, then you may minimize the number of vias

used for GND underneath the BGA. This will open routing channels which may be critical for an extremely dense board
- You may still want vias for some of the GND pins to improve the return paths

Disadvantages
- If the return paths are managed with a minimum number of GND vias, there really isn't a downside to using this method.
- It is often thought that using the outer layers for GND will limit the number of buildup (smaller features) layers for routing signals. Although this is true, it is also important to consider that controlling the signal integrity of those nets will be more difficult and burying the first GND plane in the laminate structure will result in the routing on the micro-via layers to not have a good reference plane.

- Outer Layer GND and VCC
  A stackup such as this one is typical when GND is assigned to the outer layers.

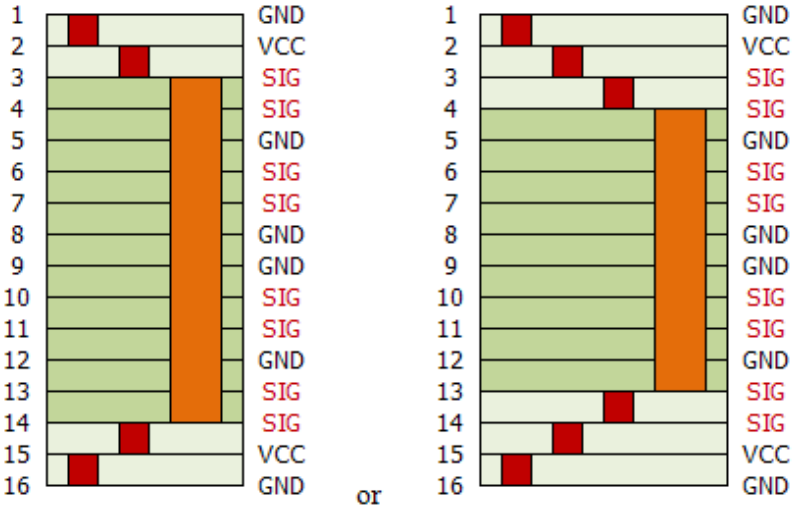


Figure 3-11: GND and VCC on outer layers

Advantages

This scheme has the same advantages as listed for "Outer Layer GND" plus these additional ones:

- The capacitive coupling between the GND and VCC layers will be excellent minimizing the bypass capacitors needed for the BGA (assuming you use a relatively thin dielectric - less than .05^{mm} or 2th).
- This is also an opportunity to use embedded capacitors and pull-up resistors effectively; resulting in opening up considerable routing space on the signal layers.

Disadvantages

- If the return paths are managed with a minimum number of GND vias, then there really isn't a downside to using this method.

Recommendations

- Using a skip-via or stacked-vias would be good for this kind of stackup if it can be cost justified.

- Split Planes

  Often large BGAs require multiple voltage supplies. You can use split planes or dedicated voltage layers for this power distribution. If this method is used, it is best to add a couple voltage supply layers in the center of the board surrounded by GND planes to avoid having signal layers affected by crossing the splits or different voltages.

Layer Count

The number of buildup and core layers required to route the board and fulfill the performance and signal integrity requirements will vary depending on the route density and manner in which you decide to manage the plane layer assignments. Determining the route density is a subject outside the scope of this book; however, as a general rule for large dense boards start with 8-10 signal layers and increase them as needed during the routing process.

Since the thickness of the laminated core will be limited by the aspect ratio of the buried via (10:1), work with your board fabricator to determine core and prepreg thicknesses. Doing this in conjunction with trying to minimize via pad size for routing will enable you to determine the high-end number of layers available in the laminated core.

Design Rules

Throughout this book, the minimum values for via hole and pad diameter as well as the aspect ratios have been described. These minimums are used as a guide to enable high yields. Minimum trace widths and clearances are based upon the fabricator's capabilities; however, they are more than likely to be set based on signal integrity requirements such as impedance control and minimizing crosstalk.

Fanout Patterns

The method used for fanout of BGAs is a subject of an entire chapter and can significantly contribute to the success or failure of the design. Here are some of the considerations:

- Via location relative to BGA pad
    - Adjacent (dog-bone)
    - Partial via-in-pad
    - Offset via-in-pad
    - Via-in-pad
- When using a combination of micro-vias and buried-vias, each via span can have its own pattern within the BGA and as such can affect the route-ability of the device.
    - Via-in-pad methods provide the greatest opportunity to increase route density.
    - Shifting and aligning the vias may be useful to improve route-ability.

- Using a complimentary patterns for the micro-vias and buried-vias can improve route-ability
- The goal should be to reduce the overall “effective” number of pins by the time you get to the laminated core, thus reducing the number of layers required to breakout and route the BGA.

Signal Integrity

This is a subject that has many dependencies, variables and thousands of articles. The desire here is to simply point out a few design methods related to large board HDI stackups that could positively affect signal integrity:

- Remove unused pads on buried vias to reduce crosstalk.
- Route the high-speed single-ended nets on the buildup layers closest to the component. The potential for via stub effects is eliminated because buried-vias are not used.
- Route differential pairs on the laminated core layers. The via stubs affect the differential pairs less than the single-ended nets and the crosstalk between the diff pair vias (if the unused pads are removed) is likely to be insignificant.
- A stripline configuration, where pairs of signal layers are sandwiched between plane layers, not only provides the best return paths but also reduce crosstalk. This supports the notion that using a ground plane on the outer layers is a good practice.

Recommended HDI Stackups

What are the best HDI stackups for BGA breakouts and routing? It depends on your priorities. The following stackups were analyzed for relative cost, route density, power integrity and signal integrity. The three are rated at the top with the priority given to route density with good power and signal integrity.

Stackup A

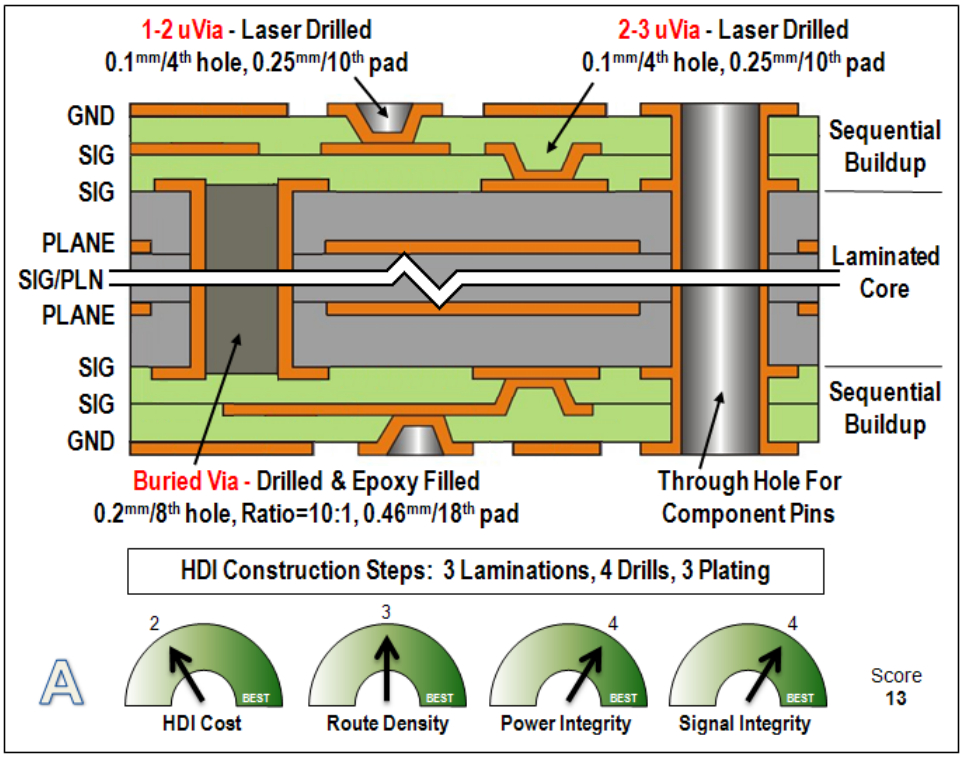


Figure 3-12: Stackup A

Stackup A Comments:

- Total score = 13
- This is a great average of the variables and a good stackup if you are starting out with HDI.
- The via models are simple and it won't be difficult to find vendors who can fabricate them.
- The ground plane on the outer layers provides a high rating for power and signal integrity.

Stackup B

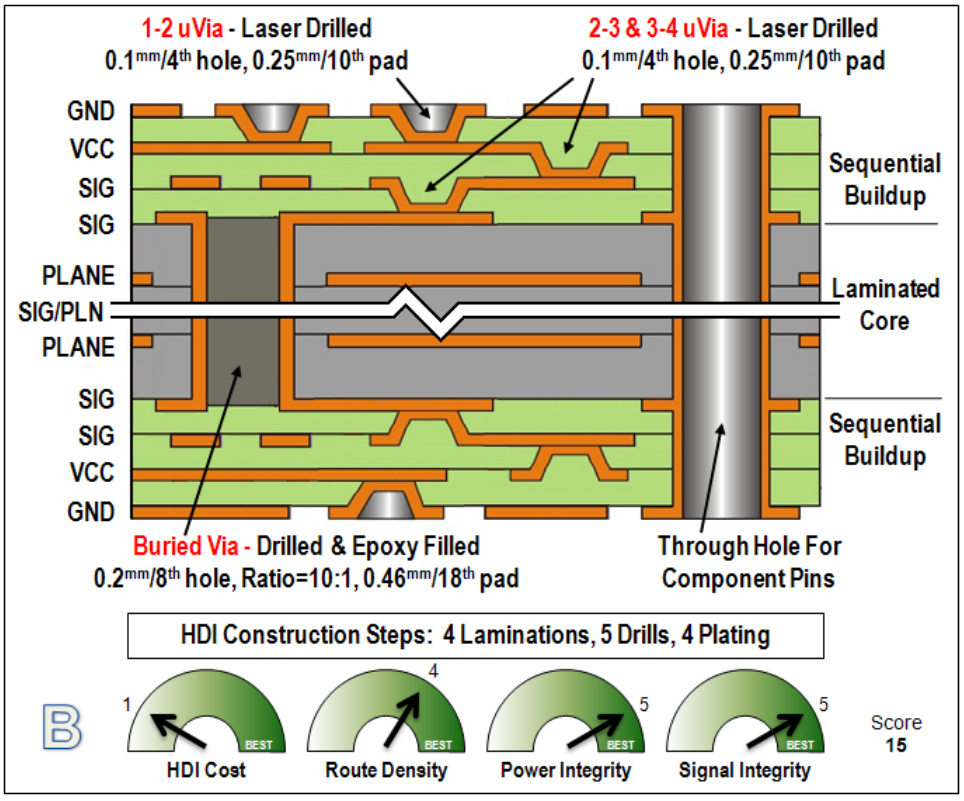


Figure 3-13: Stackup B

Stackup B Comments:

- Total score = 15
- The GND and VCC on the outer layers provide the best power and signal integrity.
- The additional buildup layer increases the cost (more laminations, drills, and plating steps) but also improves the route density as opposed to losing an HDI routing layer due to the VCC plane.
- The via models are simple and it won't be difficult to find vendors who can fabricate them.

Stackup C

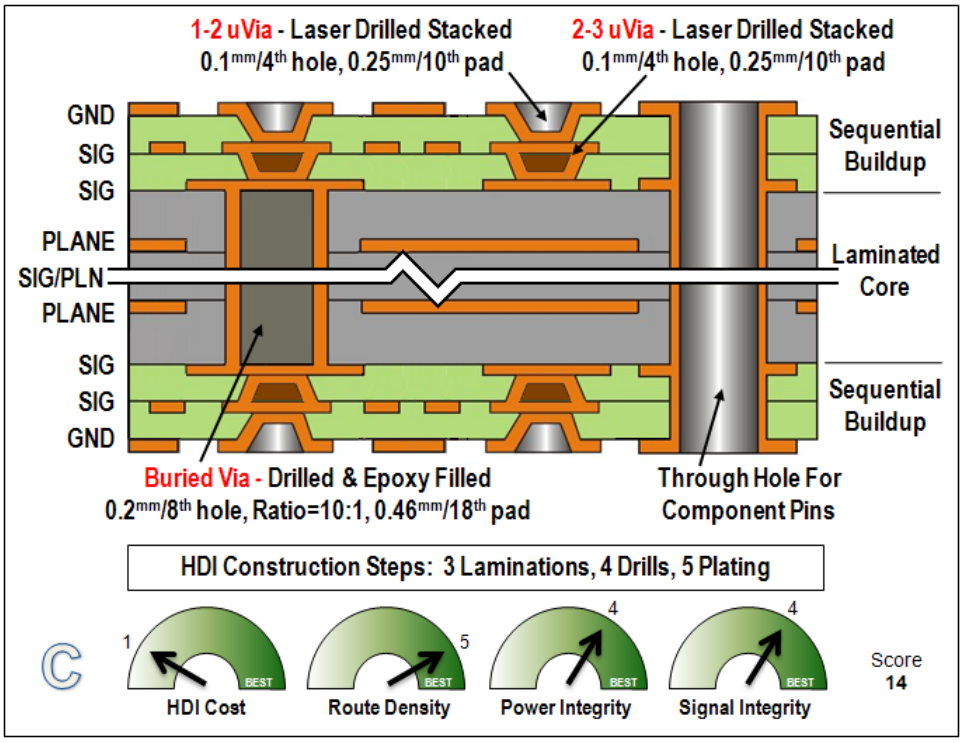


Figure 3-14: Stackup C

Stackup C Comments:

- Total score = 14
- The stacked vias enable the best route density but also increases the cost and may limit the number of vendors who can fabricate this stackup.
- The ground plane on the outer layers provides the high rating for power and signal integrity.

Secondary HDI Stackups

These stackups are useful in their own way depending on your priorities; but they not as good overall as the Top 3.

Stackup D

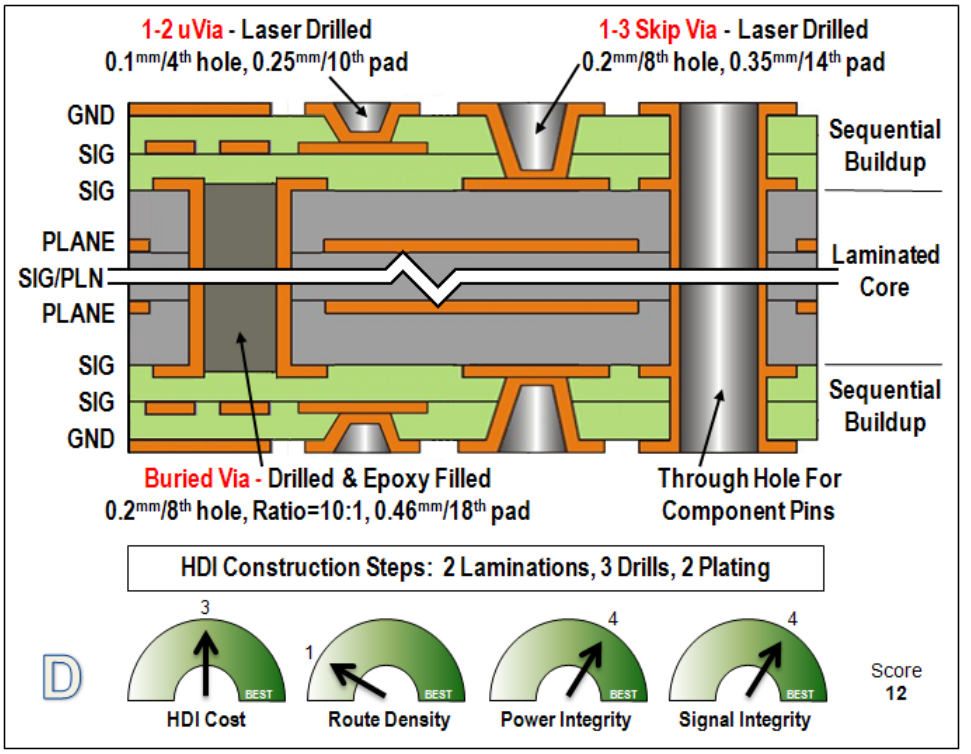


Figure 3-15: Stackup D

Stackup D Comments:

- Total score = 12
- The ground plane on the outer layers provides the high rating for power and signal integrity.
- The skip via reduces laminations and plating steps, which lowers cost; however, contributes to a relatively low route density.

Stackup E

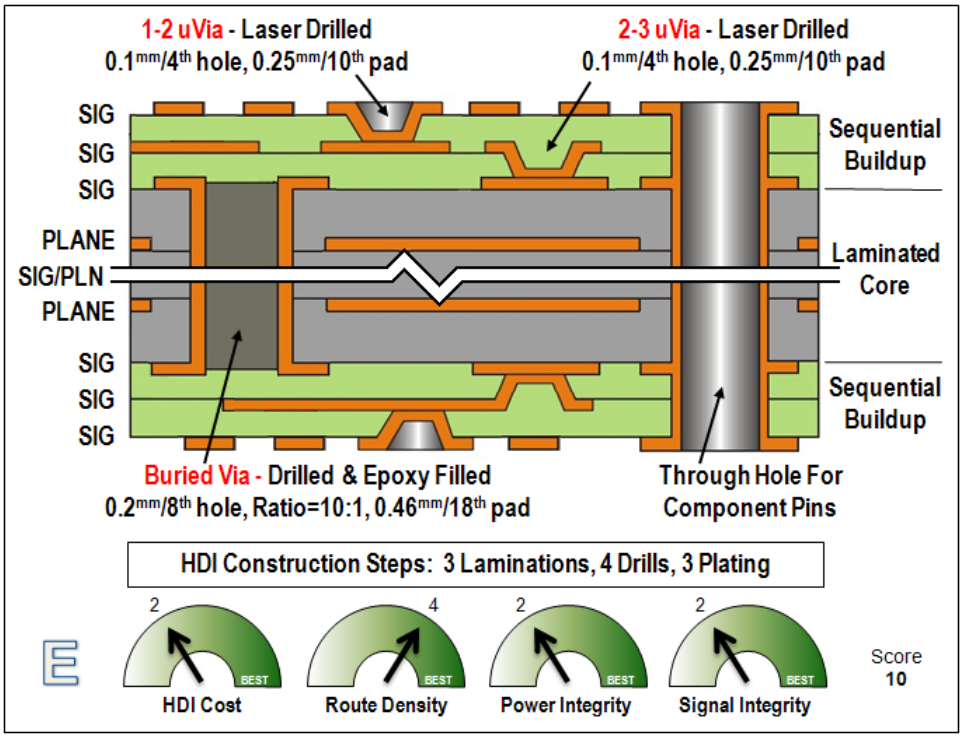


Figure 3-16: Stackup E

Stackup E Comments:

- Total score = 10
- The lack of a ground plane on the outer layers reduces power and signal integrity; however it does provide for improved route density assuming routing would be done on the outer layers.
- The via models are simple and it won't be difficult to find vendors who can fabricate them.

Stackup F

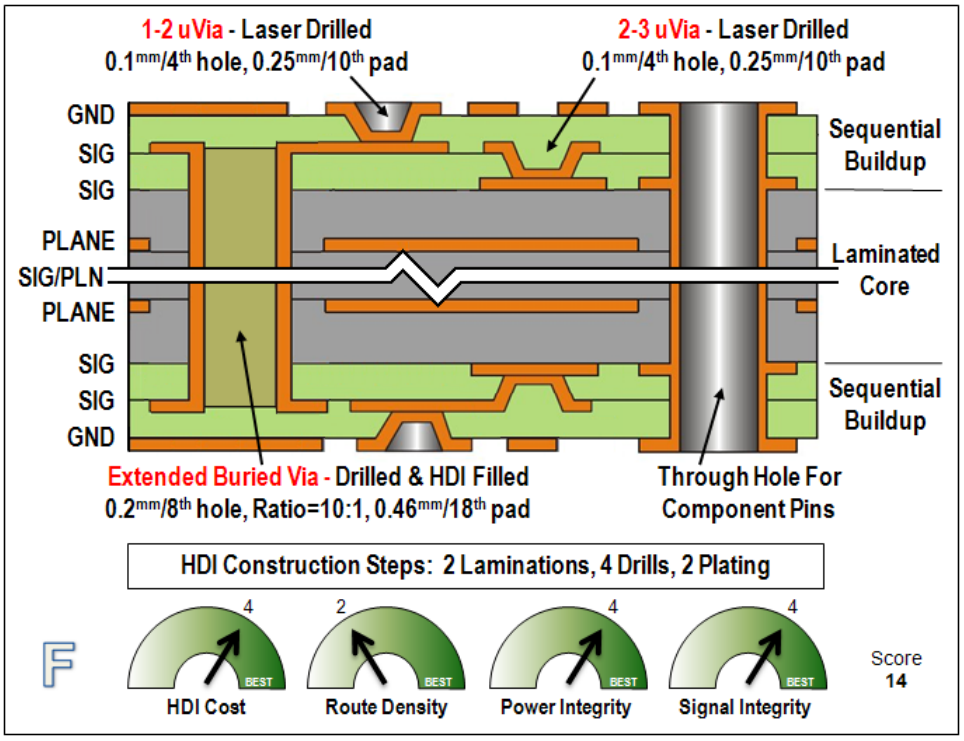


Figure 3-17: Stackup F

Stackup F Comments:

- Total score = 14
- The ground plane on the outer layers provides the high rating for power and signal integrity.
- The extended buried via reduces the lamination and plating steps which lowers cost; however it reduces route density.

Stackup G

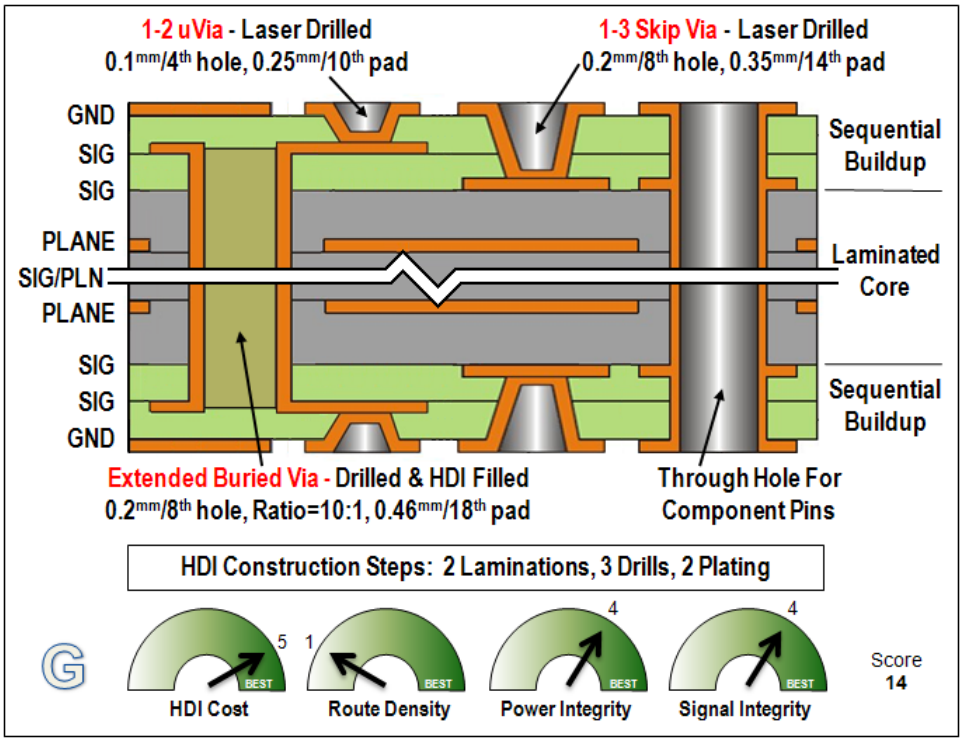


Figure 3-18: Stackup G

Stackup G Comments:

- Total score =14
- The ground plane on the outer layers provides the high rating for power and signal integrity.
- The extended buried via and the skip via reduces the lamination and plating steps which lowers cost; however it also reduces route density.

Any-Layer-Via Stackups

The any-layer-via stackup is an HDI variation that although currently expensive will become affordable over time and in my opinion provide the kind of stackup and via models that will be required for successful routing of very large and very fine-pitch BGAs. As you can see in Figure 3-19, vias can span any set of layers.

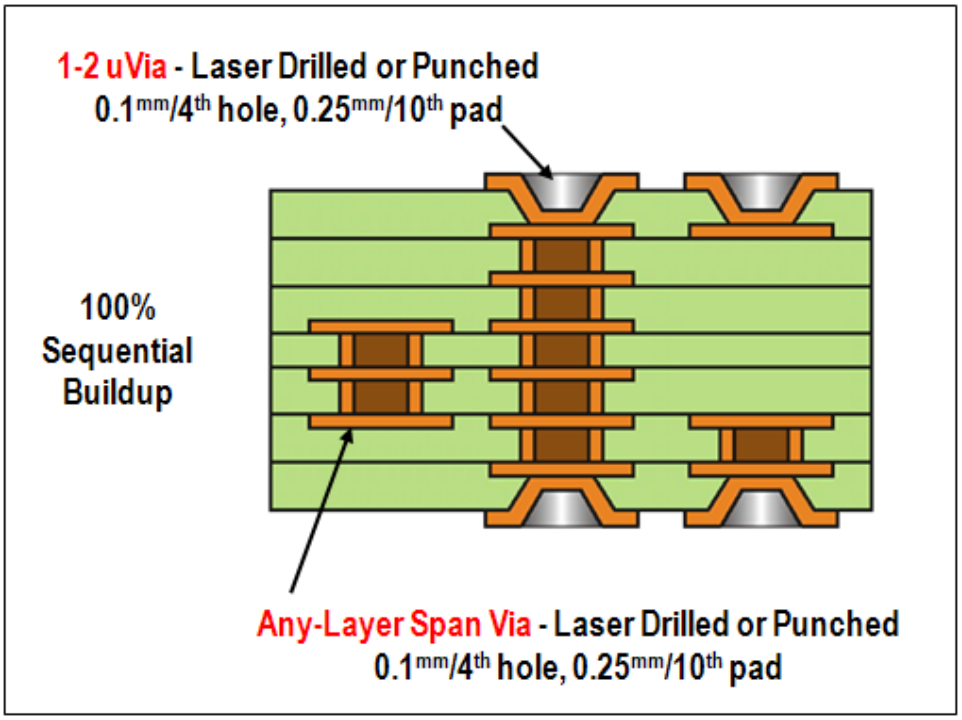


Figure 3-19: Any-layer-via stackup

The micro-vias are either punched or laser-drilled and are filled with a conductive material after each buildup stage in the metallization process to connect them. Although Matsushita Corporation originated the ALIVH (Any

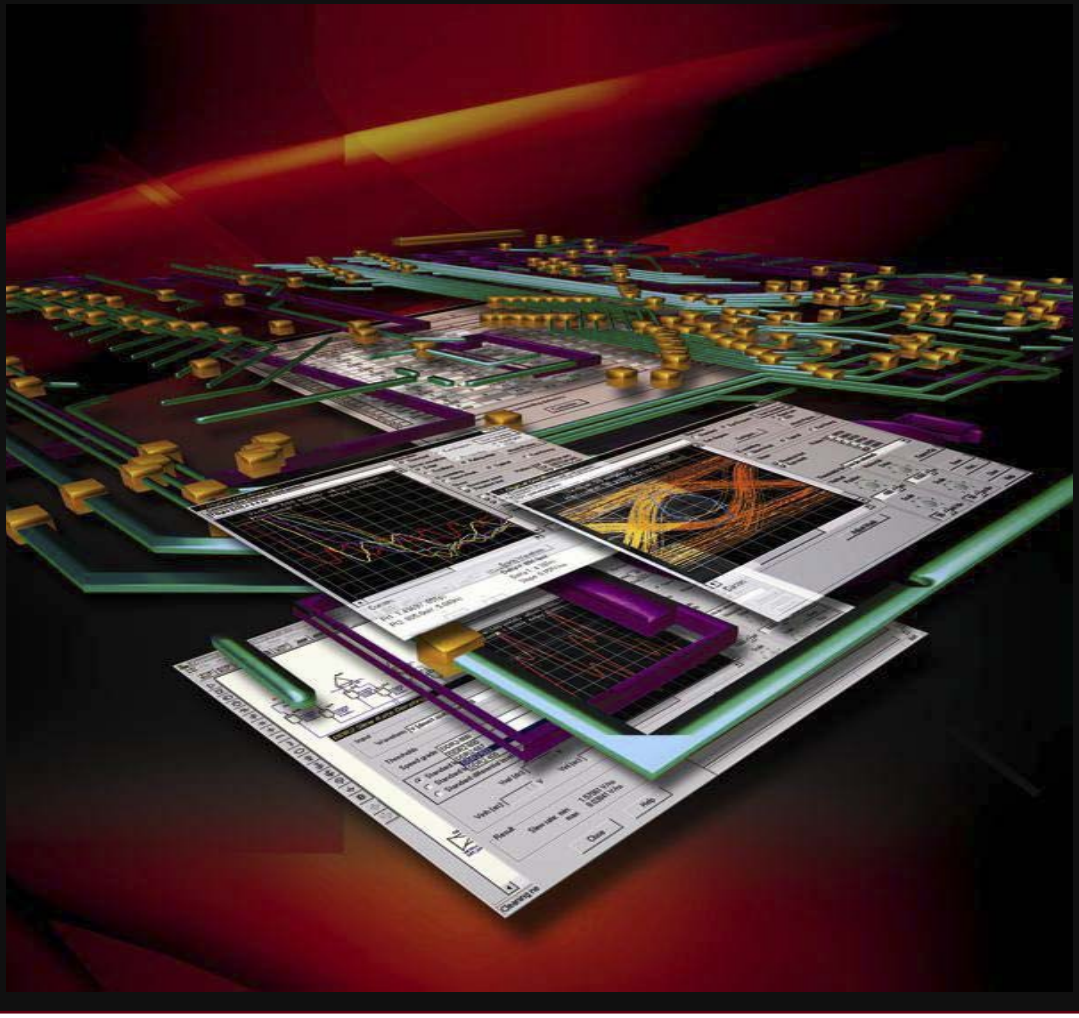
Layer Interstitial Via Holes) numerous other companies are developing new processes that allow for micro-vias to span any layers.

Chapter 6, “0.8mm Pitch BGA Tests”, applies the any-layer-via method and demonstrates the great advantages of this via model.

Summary

There are many variations available for HDI stackups. The one you choose to use will have to balance the cost, route density, signal and power, and integrity. New fabrication methodologies continue to evolve and within a few years you will have even more possibilities.

Happy Holden, PCB Technologist at Mentor Graphics, has written scores of articles and presentations on HDI. His body of work may be found at www.mentor.com/pcb and www.westwoodpcb.com. His expertise and knowledge is described in tremendous depth and will certainly provide great insight to HDI materials, best practices and the impact on signal and power integrity.



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Chapter Four - Fanout Patterns

The effectiveness of a fanout pattern on large BGAs contributes significantly to the route-ability of a design which impacts the layer count, which in turn affects the cost of the board fabrication. The fanout of a BGA is only a part of the routing solution, which also may include escape traces along with the general interconnect routing of the pins.

Since there are many variables involved in determining fanout patterns, such as layer stackup, via models, via spans, and design rules, this chapter will explore fanout patterns BGAs in the context of large, dense boards where minimizing layer count is important.

The goal of the BGA fanout effort should be to eliminate the BGA routing as the primary contributor to the number of layers while maintaining signal integrity and fabrication yield requirements. This chapter offers numerous ideas and methods that may or may not be useful in the context of your design requirements. Hopefully you will find some of them useful to reduce layer count, increase route density and meet your performance goals.

The method used for fanout of BGAs can significantly contribute to the success or failure of the design. Below are some of the considerations:

- Via location relative to BGA pad
    - Adjacent (dog-bone)
    - Partial via-in-pad
    - Offset via-in-pad
    - Via-in-pad
- When using a combination of micro-vias and buried-vias, each via span can have its own pattern within the BGA and as such can affect the route-ability of the device.
    - Via-in-pad methods provide a good opportunity to increase route density.
    - Shifting and aligning the vias is best way to improve route-ability.

- Using a complimentary patterns for the micro-vias and buried-vias can improve route-ability
- Goal should be to reduce the overall “effective” number of pins by the time you get to the laminated core, thus reducing the number of layers required to breakout and route the BGA.

Theoretical Breakout Methods

Numerous papers have been written about BGA breakouts, and nearly all of them take a theoretical approach. By “theoretical” I mean the BGA is analyzed outside the context of a real design, often with unrealistic assumptions about power and ground pin assignments, and with little or no regard for signal integrity requirements.

This kind of solution is more of a mathematical exercise in layer reduction as opposed to one that takes careful consideration of balancing the numerous real-world constraints. Unfortunately, reality requires much more than just a mathematical solution. BGAs with over 1500 pins are significantly affected by these additional factors that prevent theoretical solutions from being effective.

This section discusses BGA pin assignments, escape routing, as well as signal and power integrity because these factors affect the decisions about fanout patterns. Deriving fanout patterns in a theoretical realm can actually be fairly simple. Finding effective fanout patterns when all the design and packaging challenges must be considered is a much more difficult problem.

Distribution of Power and Ground Pins

Ideally, it would be nice to have power and ground pins only in the center of the BGA; however, power integrity requires they also be distributed among the signal pins. This distribution is rarely in organized columns and rows, which under some circumstances (HDI, blind and buried vias and a

stackup with power and ground on the outer layers) can open up considerable routing space.

Figure 4-1 shows an ideal distribution of ground pins (green). If the BGA could have the ground pins aligned in this way, and if the mount layer was a ground plane, room is made available on the inner routing layers.

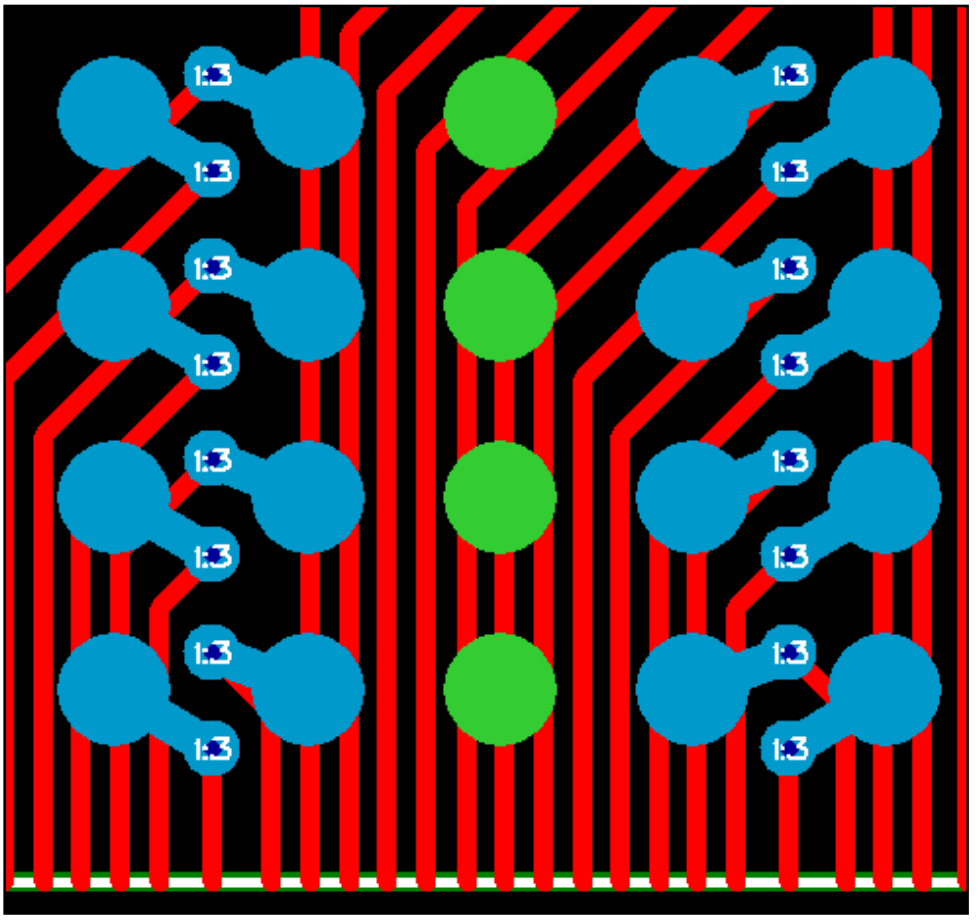


Figure 4-1: Alignment of ground pins

Yet, rarely are the power and ground pins aligned in such a way. In fact, most FPGA vendors sprinkle the power and ground pins or use some

pattern other than columns and rows. The purpose of distributing power and ground pins is to improve the power integrity. Xilinx often uses a "Sparse Chevron" pattern as shown in Figure 4-2. In this figure the ground pins are green and the power pins are brown.

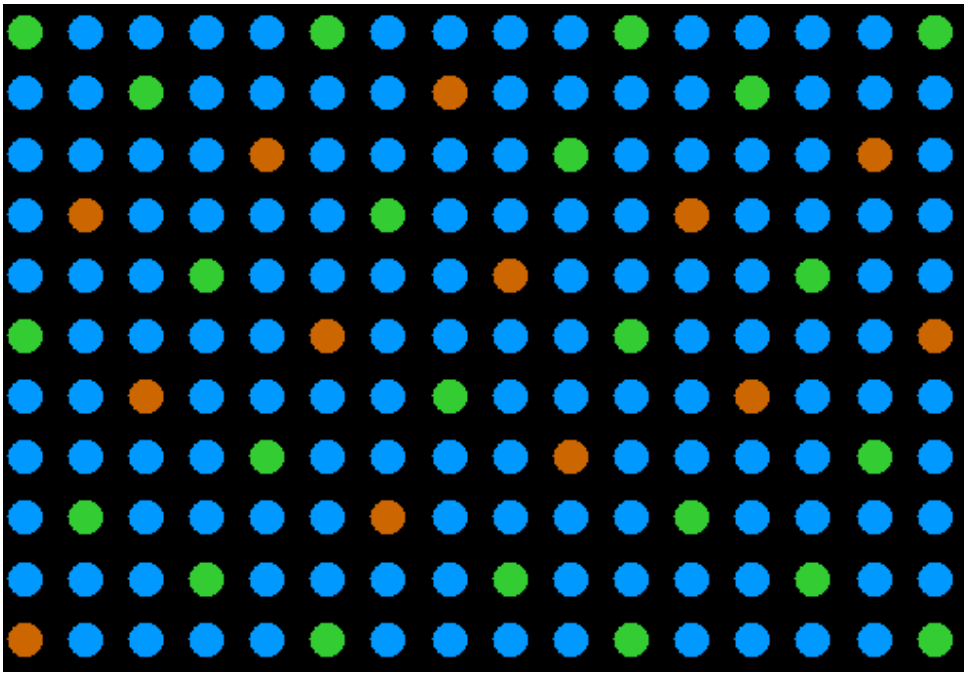


Figure 4-2: Xilinx Sparse Chevron pattern for power and ground pins

There may be some ASICs that have power and ground pins aligned in columns and rows, which indeed could help open up routing channels on inner layers and reduce layer count. However, such an ideal condition is not common and therefore effective fanout and routing solutions must find other ways to reduce the layer count.

Serial and Parallel Nets

Most large BGAs have a combination of serial and parallel nets which need to be routed as differential pairs and single-ended nets, respectively. Some FPGAs also allow for nets to be programmed as either serial or parallel.

These devices support multiple I/O standards ranging in performance that could require differential routing.

Differential pairs require different trace widths and spacing than single-ended nets to maintain the desired impedance and although it is possible to use the same spacing rules inside the BGA area, the impedance discontinuity may become significant in some high-speed circuits.

For example, it is common to have a target of 50Ω for single-ended nets and 100Ω for differential pairs. Of course the stackup thicknesses and materials will affect the impedance; yet it is common to see a 0.15mm (6th) for differential pair spacing while single-ended nets can have 0.1mm (4th). Actual trace widths and clearances will vary depending on the specific high-speed and fabrication requirements for each design.

If the fanouts are positioned such that differential pairs need to be split to maintain the trace width and clearance rules, that could also be a significant signal integrity problem. This is illustrated in Figure 4-3.

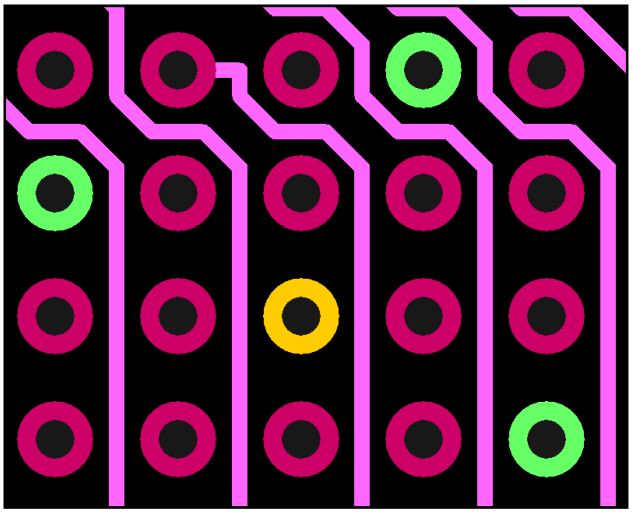


Figure 4-3: Splitting of differential pairs in BGA fanout via array

The point is that a theoretical fanout and breakout solution that does not take into consideration the potential for varied trace widths and clearances is not very useful. The problem becomes even more difficult when each I/O pin or bank of I/O pins may be programmed to require either differential pair or single-ended routing. An effective fanout solution that enables the most efficient escape routing needs to be flexible enough to support the trace width and clearance requirements for a potential mixture of serial and parallel.

Signal Integrity Concerns

Via Crosstalk Effects

BGA fanout vias have the potential for allowing significant crosstalk if the spacing between them is inadequate.

Conditions in which the crosstalk effects should be insignificant:

Differential pairs

- Fanout vias, when paired differentially, actually crosstalk very little with each other. That's because the differential signaling localizes the EM fields heavily within each via pair.
- Removing unused pads on through-vias and buried-vias is also recommended because they are a source of noise.

Micro-vias

- When using micro-vias with a span of 2 or 3 layers, the crosstalk potential between vias is much lower than in the case of through-vias or buried-vias.

Conditions that may enable significant crosstalk:

Fast single-ended nets

- When using through-vias or buried-vias for these nets, vias in close proximity will cause crosstalk.
- This can be mitigated by removing unused pads and back-drilling.

- Routing fast single-ended nets on buildup layers using micro-vias will also greatly reduce crosstalk.

Grounded Stitch Vias

A number of designers have recommended using grounded "stitch vias" near each fanout to provide a clean return path and to reduce crosstalk. Although this method indeed improves signal integrity, it is not a practical solution in the context of large BGAs. The addition of the stitch vias will take up far too much room and also add to the cost of the board fabrication due to the additional routing layers needed to route the device. If there are just a few nets of concern, stitch vias may be a solution. Adding stitch vias around 900 I/Os is not an effective solution. There are other, less expensive methods that can be applied to minimize crosstalk.

When deriving an effective fanout pattern, potential crosstalk between the vias must be considered and managed. Simply spacing them far apart may well eliminate the crosstalk. However, the impact on layer count may be a larger negative. Crosstalk is one of many design problems that needs to be appropriately managed. Maintaining via crosstalk noise below acceptable thresholds as opposed to trying to completely eliminate the effects can enable other goals (such as lowering cost and increasing reliability) to be attained.

Minimizing the Variables

Since there are so many variables such as the stackup, via models and design rules, along with power and signal integrity requirements; it is quite easy to become overwhelmed with the number of possible fanout patterns and not understand their impact on the overall design. There are some principles, however, that can help you choose the appropriate fanout patterns for your particular design.

BGA Pin Count

< 800
If the number of pins is fewer than 800, the routing of the BGA does not impact the layer count and the routing challenges will be found elsewhere in the design.

800-1500
Within the range of 800-1500 pins there is a potential that routing of the BGA (especially if there are multiple instances on the board) could present a challenge and therefore the fanout patterns should be carefully determined.

>1500
When one or more BGAs in a design have greater than 1500 pins, the routing of these BGAs becomes the most significant contributor to the number of layers in the design and consequently the cost of the board is impacted. An effective set of fanout patterns will likely enable reduction of layer count and board cost.

This document presents fanout patterns for multiple BGAs with >1500 pins that may be effective for your particular design.

Design Rules

The design rules used for the fanout patterns will be as listed in these tables:

		mm	mils	Lead Free (mm)
1 mm Pitch BGA	Micro-Via Pad / Hole	0.25/0.10	10/4	
	Blind-Via Pad / Hole	0.45/0.20	18/8	
	Buried-Via Pad / Hole	0.45/0.20	18/8	
	Through-Via Pad / Hole	0.50/0.25	20/10	
	Ball Pad	0.62	25	.30-.40
	Trace Width	0.10	4	
	Diff Pair Clearance	0.15	6	
	Trace-Trace Clearance	0.10	4	
	Via-Trace Clearance	0.10	4	
	Via-Pad Clearance	0.10	4	

Table 4-1: Design rules for 1mm pin pitch

		mm	mils	Lead Free (mm)
0.8 mm Pitch BGA	Micro-Via Pad	0.20	8	
	Blind-Via Pad	0.30	12	
	Buried-Via Pad	0.40	16	
	Through-Via Pad	0.45	18	
	Ball Pad	0.50	20	.30-.40
	Trace Width	0.08	3	
	Diff Pair Clearance	0.12	5	
	Trace-Trace Clearance	0.08	3	
	Via-Trace Clearance	0.08	3	
	Via-Pad Clearance	0.08	3	

Table 4-2: Design rules for 0.8mm pin pitch

BGA Ball Pads

The size of the ball pad varies depending on the soldering process and if lead-free solder is being used. Since lead-free solder does not spread like

leaded solder, the ball pad sizes are generally more effective if they are smaller.

In the context of fanout patterns, the size of the ball pad does not have much impact since the gains in space for routing will be generally attained on the inner layers. A smaller ball pad will enable greater coverage of a ground plane; whereas a larger ball pad enables more flexibility regarding the location of a via-in-pad.

Via Hole Sizes
The via hole size for buried and through vias will need to maintain an aspect ratio less than 10:1 (board thickness to hole size). If the aspect ratio is larger, the fabrication yield will be significantly reduced and consequently the cost of the board will rise.

Via Models and Stackups
Fanout patterns using these via models will be addressed.

- Through-vias in a laminated design
- Blind and buried vias in a laminated design
- Micro-vias and buried vias in a number of HDI configurations (laminated core with build-up layers)

Fanout Pattern Goals and Approach

In the context of large BGAs, effective fanout patterns can reduce layer count, improve signal and power integrity, and contribute to board reliability. If the BGA is not large (less than 1500 pins) the device can usually be routed within the same number of layers needed for general routing of the board.

When determining a specific fanout patterns, the available via spans are the most significant variable and we shall start there.

Teardrops and Etch Traps

In these examples, please ignore the fact that some of the traces create etch traps with the vias. Usually these etch traps will be eliminated with teardrops; however, teardrops were not added to these figures so that the fanout-via positions would be more visible.

Through-Vias

When using through vias, there are not too many options due to the large 0.5mm via pad relative to the 1mm ball pitch. Either a “Quadrant Dog-Bone” or “Via-in-Pad” method is appropriate.

Power, Ground and Unused Pins

One method proposed to increase route channels on inner layers is to not use fanout vias when possible for power, ground and unused pins. When using through-vias there is very little benefit to not adding fanout vias for the 30-50% of the BGA pins will likely be assigned to power, ground or unused.

As mentioned previously, the power and ground pins will be assigned to the center of the device and distributed among the other pins; and it is highly unlikely they will be distributed in nice columns and rows. Unused pins will not likely be in convenient rows and columns either.

When using through-vias for fanouts, rather than trying to gain a few route channels by eliminating connections to the planes, it is best to gain the power integrity benefits by adding fanouts for all power and ground pins.

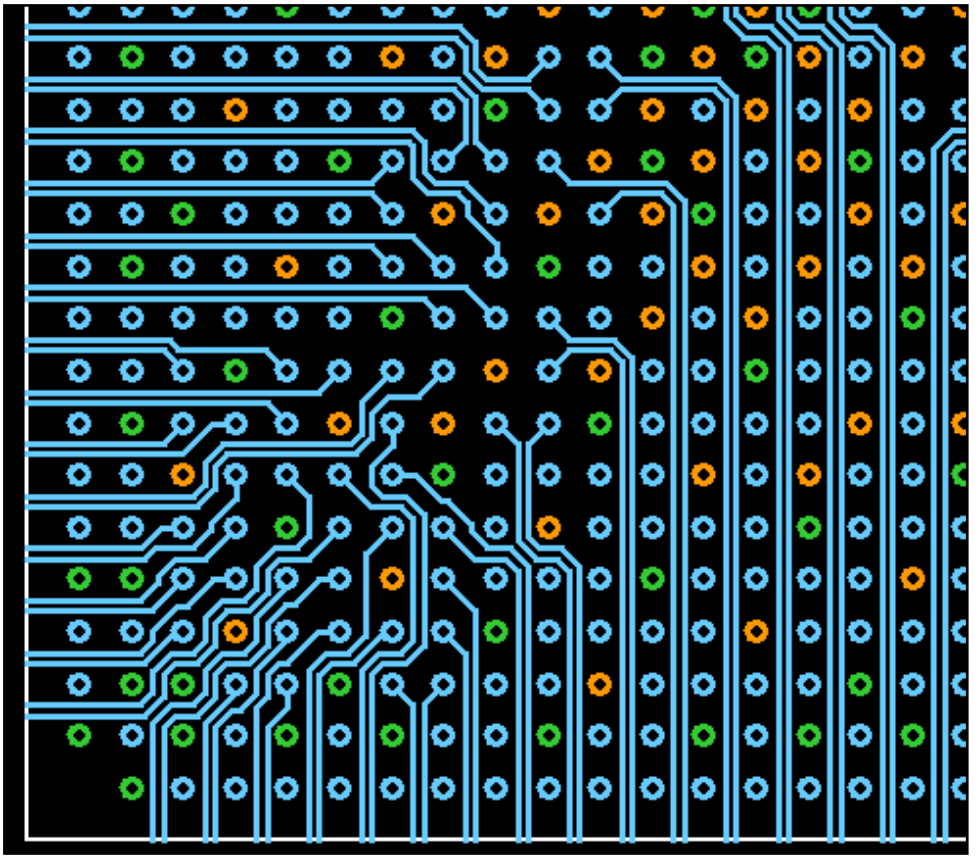


Figure 4-4: Xilinx Virtex-4 with power (orange) and ground (green) vias

It is clear that the vias for power and ground are scattered such that even if they were all removed, little would be gained. The outer perimeter of through-vias dictates how much space is available for routing, and at least in the case of the Virtex-4, few of them are assigned to power and ground.

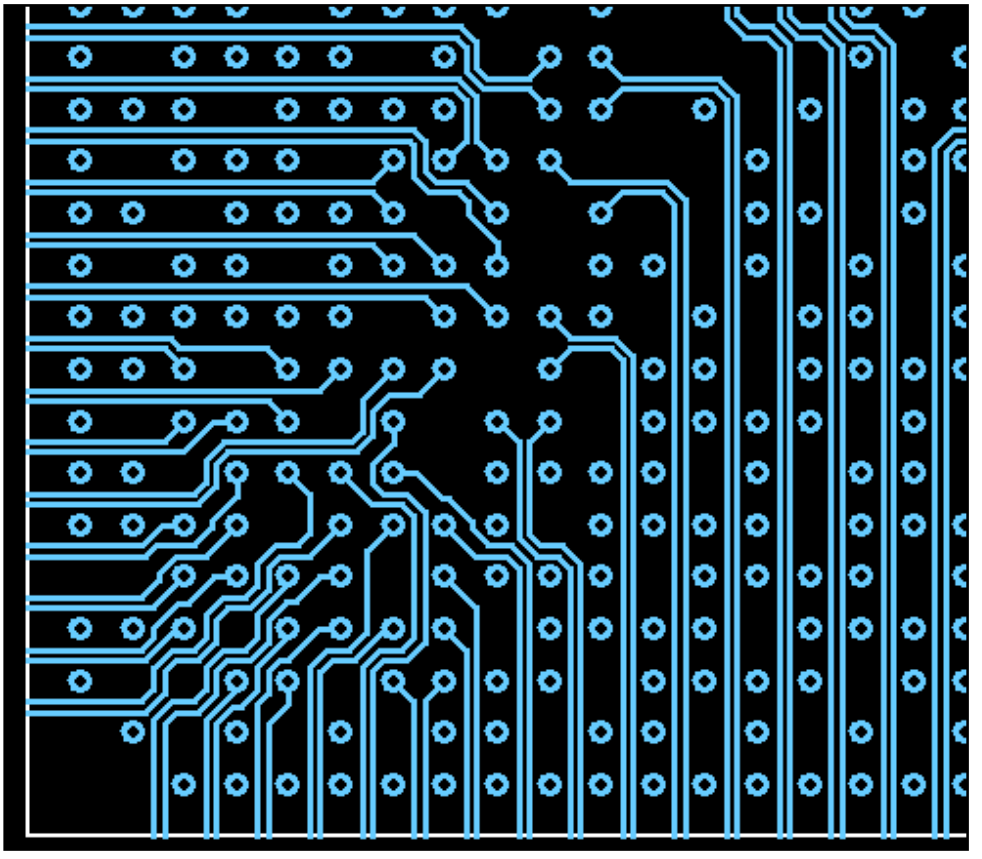


Figure 4-5: Xilinx Virtex-4 with power and ground vias removed.

In figure 4-5, few additional route channels are opened by removing the through vias for GND.

If an ASIC can be packaged to provide adequate power integrity and have the power and ground pins aligned in such a manner to open up route channels (by not using fanout vias) that would be a good circumstance; yet, it is likely to be a rare condition.

Quadrant Dog-Bone

This fanout pattern has the fanout vias spaced in the center between the ball pads and angled in one of four directions. See Figures 4-6 and 4-7.

Advantages (Over Via-in-Pad)

- Opens up additional routing channels in the center row and column. However, there is room for two or three more routes which is very unlikely to contribute to reducing layer count. See Figure 4-8.
- On the side of the board opposite the BGA mount, the column and row channel is a convenient place to add capacitors and pull-up resistors.
- Lower cost and less risk of soldering problems related to the via-in-pad.

Disadvantages (Over Via-in-Pad)

- If you have a ground or power plane on the BGA mount side, the fanout via pads prevent a continuous plane fill under the BGA.

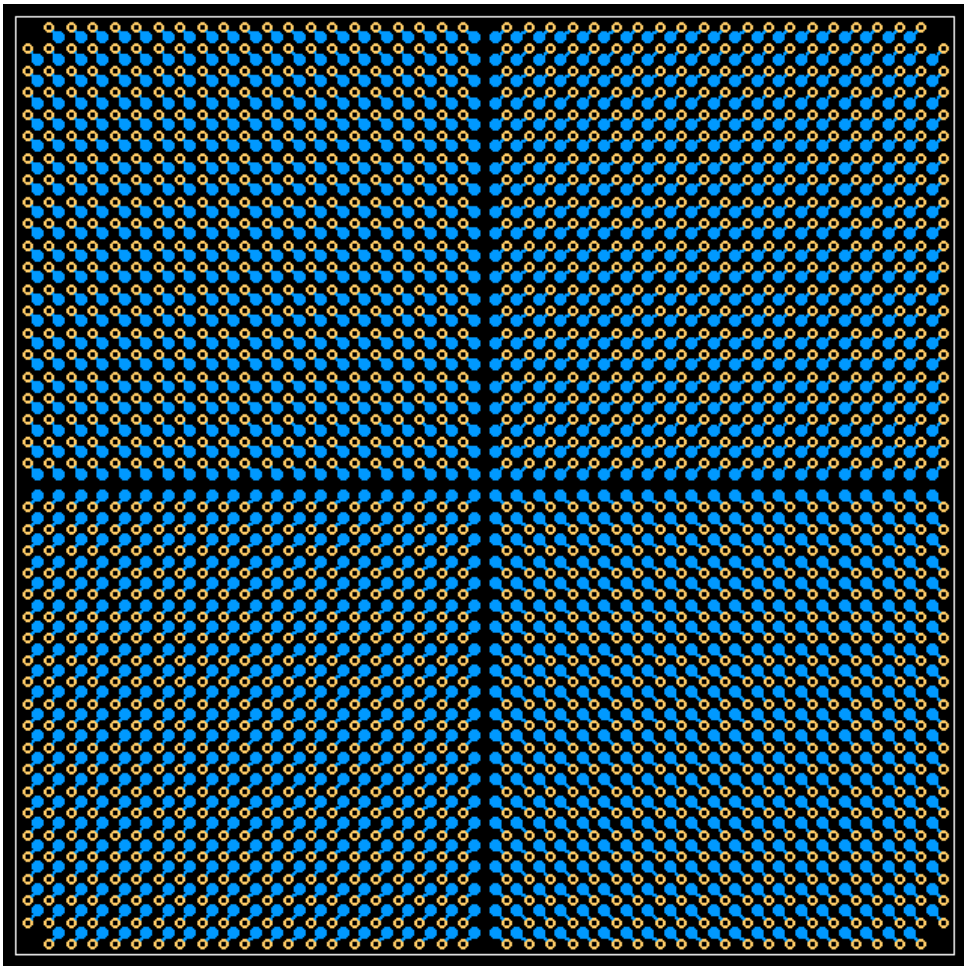


Figure 4-6: Quadrant dog-bone pattern

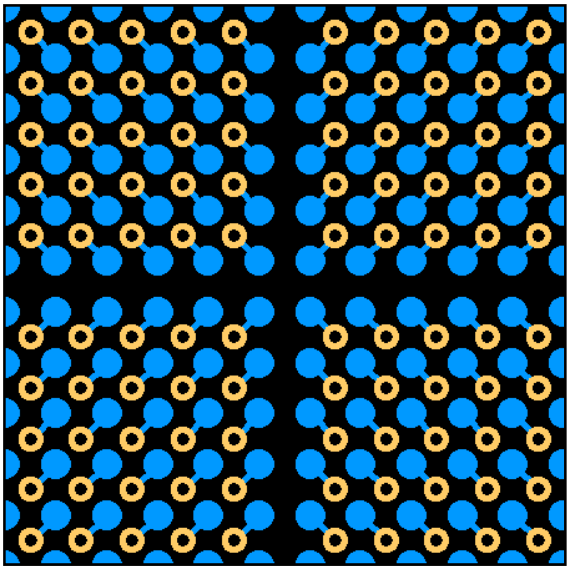


Figure 4-7: Quadrant dog-bone pattern detail

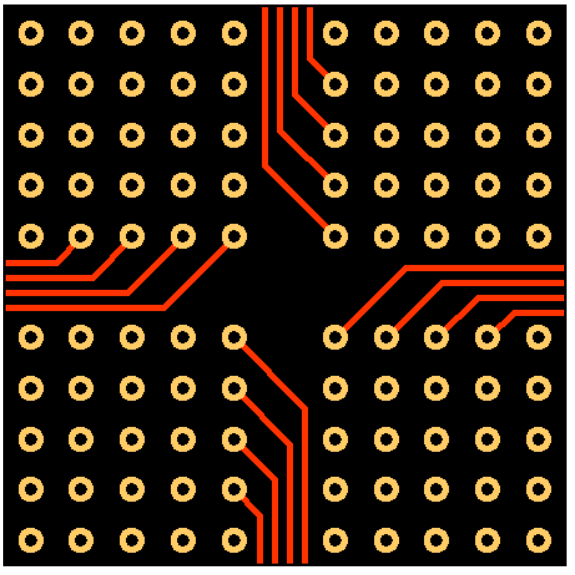


Figure 4-8: Quadrant dog-bone pattern with additional route channels

Shifting Through-Vias

Placing the fanout via anywhere but in the center of the ball pad array has a relatively small benefit to routing because there is so little wiggle-room. The benefit depends on the design rules. You could move the vias off-center a little to form columns and rows, but for every additional route channel opened on one side, it will close a route channel on the other side – the net result will be the same number of route channels (or possibly even less) across the entire BGA.

However, if the design rules are such that differential pairs cannot be routed together between the through-vias, and a little more space is required to enable it, then shifting the through-vias only slightly might make sense.

In Figures 4-9 and 4-10, note that by shifting the vias to the left on one column and to the right on the next column, you can gain 0.17mm in one and lose 0.17mm in the other. These values could be greater or smaller depending on your ball pad size and clearance rules. This method could be useful if you have some critical signals that require greater spacing within the BGA breakout area. For example, when routing a diff pair on inner layers, the clearance between the compliments can be increased from 0.44mm to 0.61mm and still maintain a 0.1mm clearance to the via pads.

Another reason for shifting through-vias while using Quad Dog-Bone patterns is to maximize the amount of plane fill on the mount layer. Again, the benefit is dependent on the design rules.

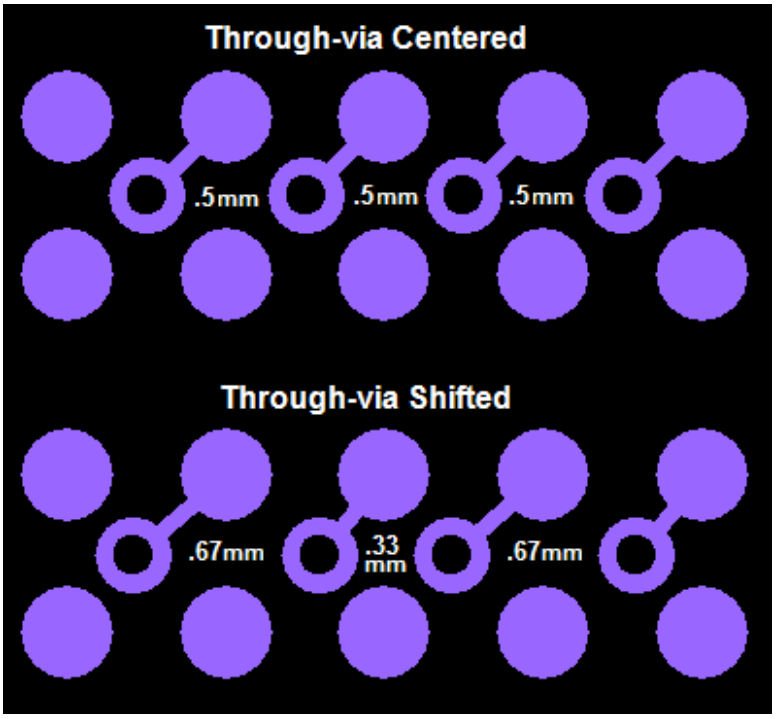


Figure 4-9: Through-vias shifted

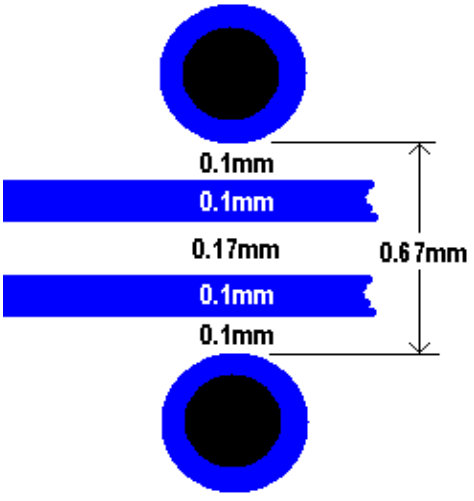


Figure 4-10: Shifted vias additional route space

Pushing Perimeter Fanouts

Another method that applies to all BGAs that use through-vias is to push the fanouts out and away from the perimeter of the ball pads. This technique allows for an extra two rows of I/Os to be routed on the first signal layer. In most cases, this will result in a reduction of one signal layer for escaping the BGA. One signal layer may not sound like much, but depending on your situation it may actually mean you can reduce the stackup by two signal layers just because the symmetry of the stackup require two layers to be added together.

Figures 4-11 through 4-13 illustrate this technique of pushing the fanouts out and away from the perimeter. The intent was to move the vias far enough out so that three traces could be routed between them on the diagonal. In the middle of the BGA, I used a simple matrix dog-bone pattern that opens up the route channels in the center rows and columns.

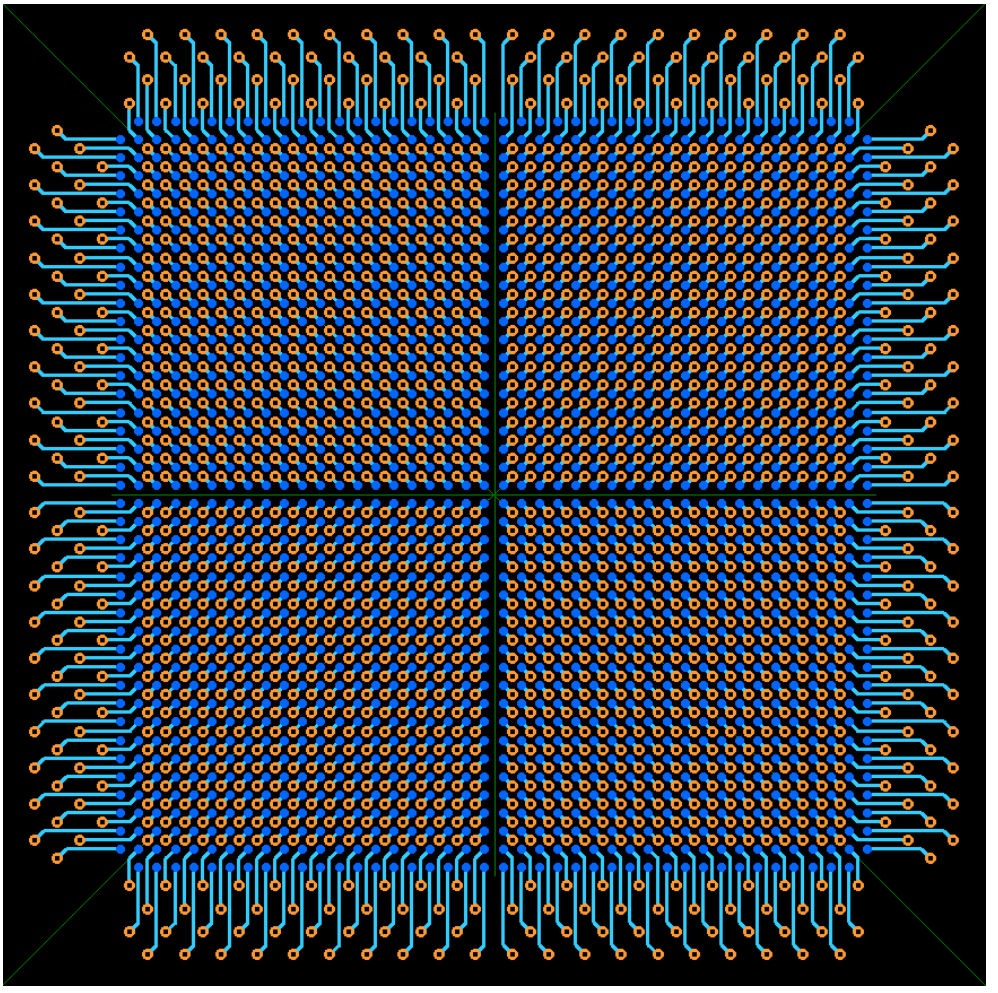


Figure 4-11: Pushing fanouts away from perimeter

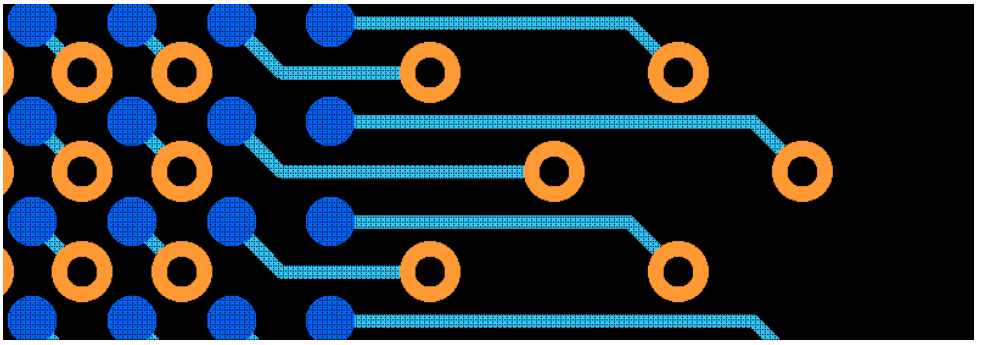


Figure 4-12: Top layer detail

Figure 4-13: Layer 2 detail

Via-in-Pad

This pattern is quite simple, add a through-via in the center of each of the desired BGA ball pads. See Figures 4-14 and 4-15.

Advantages (Over Quadrant Dog-Bone)

- If you have a ground or power plane on the BGA mount side, the fanout via pads allow a continuous plane fill under the BGA. See Figure 4-16.
- If you do not use the mount layer for a plane, then you have an additional routing layer for the BGA - albeit a surface layer which is not recommended for high-speed nets.

Disadvantages (Over Quadrant Dog-Bone)

- There are no additional route channels in the center column and row.
- There is less room for capacitors and resistors on the opposite side under the BGA since the fanout via array is full. If the BGA has unused pins and you do not add fanout vias for them; there will be some room in those locations for components.
- There will be a slightly higher cost for filling the vias and ensuring a smooth surface for the soldering of the ball pads.
- There is some risk of BGA soldering problems (de-lamination or pop-corning) with via-in-pad while using lead-free solder. An experienced assembly company should be able to manage this risk and make it a non-issue.

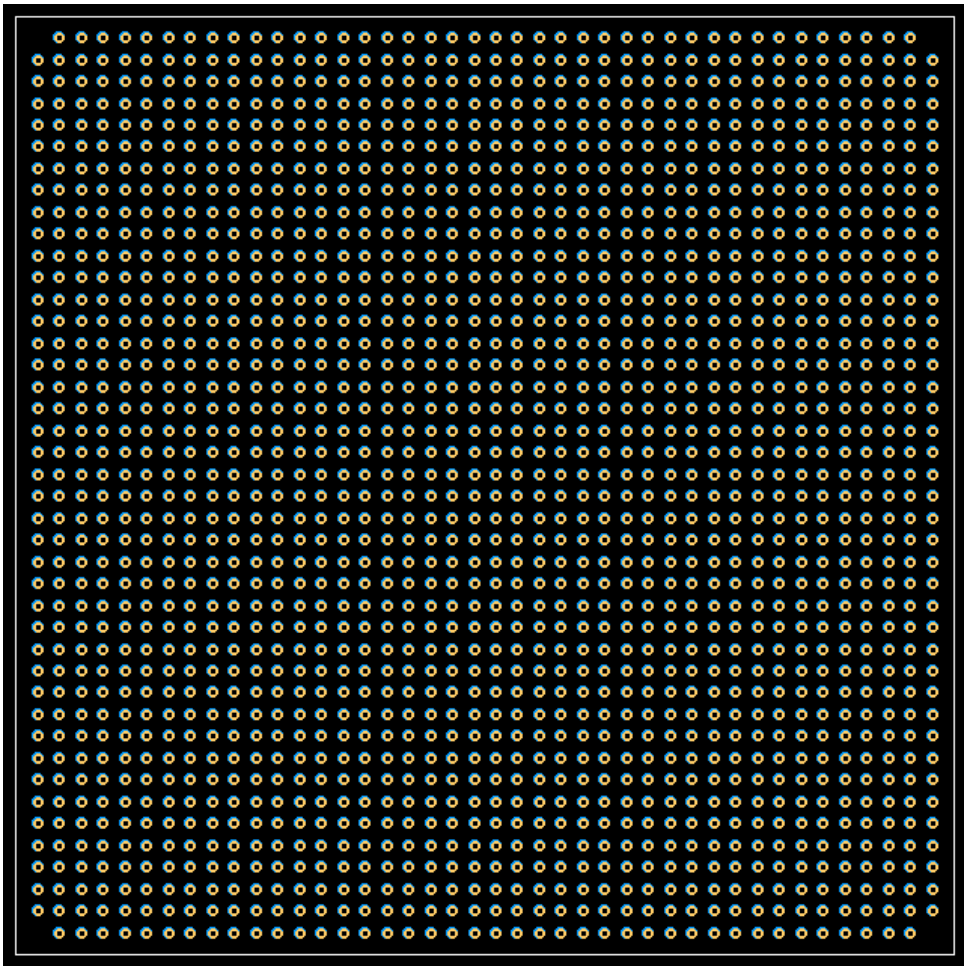


Figure 4-14: Via-in-pad pattern

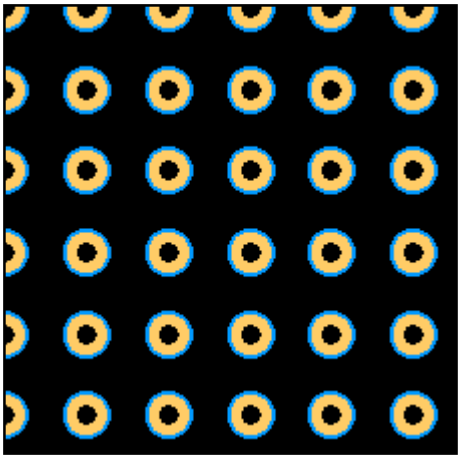


Figure 4-15: Via-in-pad pattern detail

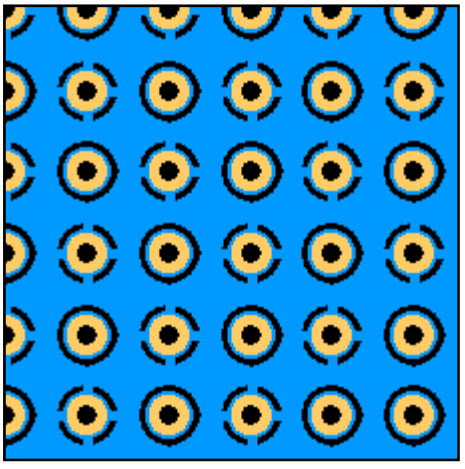


Figure 4-16: Via-in-pad pattern with ground plane on mount layer

Drilled Blind and Buried-vias

Using drilled blind & buried-vias in a sequentially laminated board may be a viable alternative, positioned between through-via laminated boards and micro-via HDI boards. In the context of high pin-count BGAs, layer

reduction and higher density routing can be achieved due to the smaller via sizes compared to through-vias; however, these gains are not as significant as can be achieved with micro-via HDI methods.

The gains are dependent on the size of the blind-via. Since a minimum drilled hole size of 0.2mm (8^{th}) applies to these blind-vias, the pad size should be 0.44mm (17^{th}). These feature sizes will be used in this analysis of fanout patterns.

	mm	mils
Blind-Via Pad	0.44	17
Buried-Via Pad	0.50	20
Through-Via Pad	0.50	20
Ball Pad	0.60	24

Table 4-3: Blind and buried-via pad diameters

This analysis assumes a layer 1:2 blind-via with the intent to route as much as possible on layer 2. The example in Figure 4-17 has the first 5 rows in from the perimeter using the blind vias in a shifted column and row pattern.

If the shifted blind-vias exist on layers 1:3, then it is likely you could breakout an addition 5 or 6 rows inside the perimeter, depending on the number of power, ground and unused pins. This is a substantial notion in the context of layer reduction.

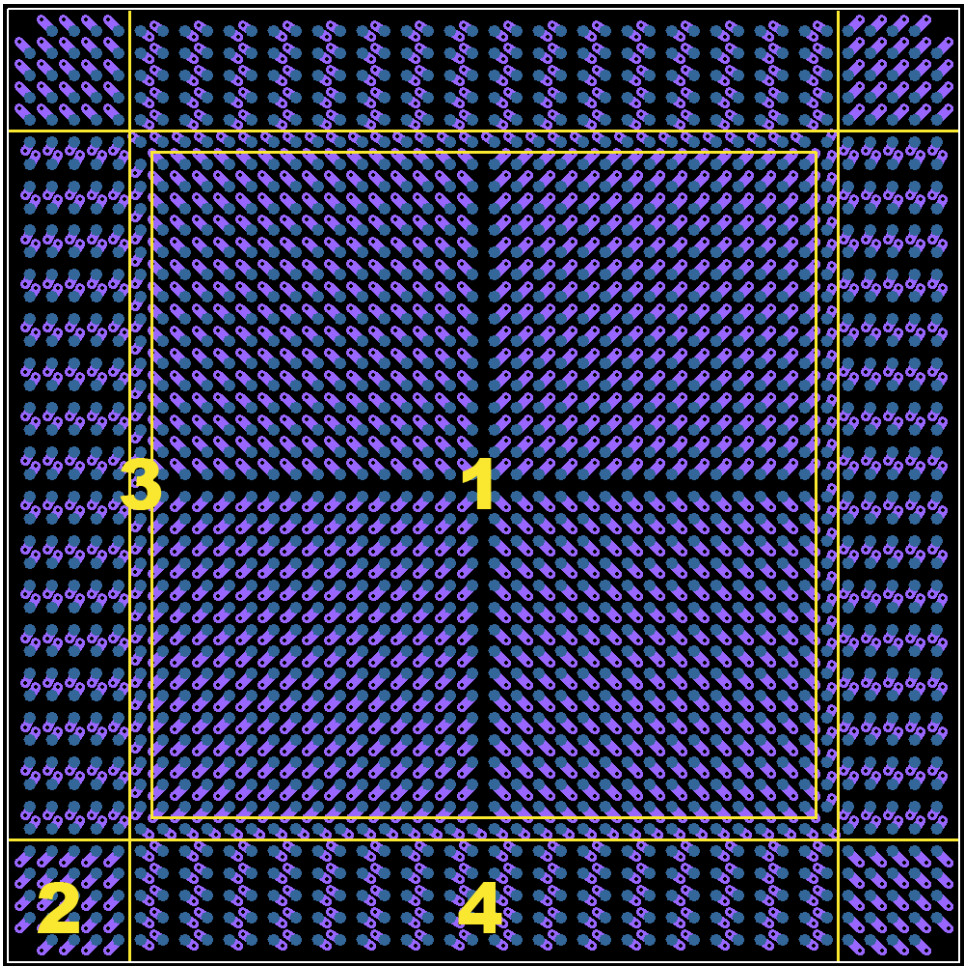


Figure 4-17: Ball pads with blind-vias shifted around perimeter

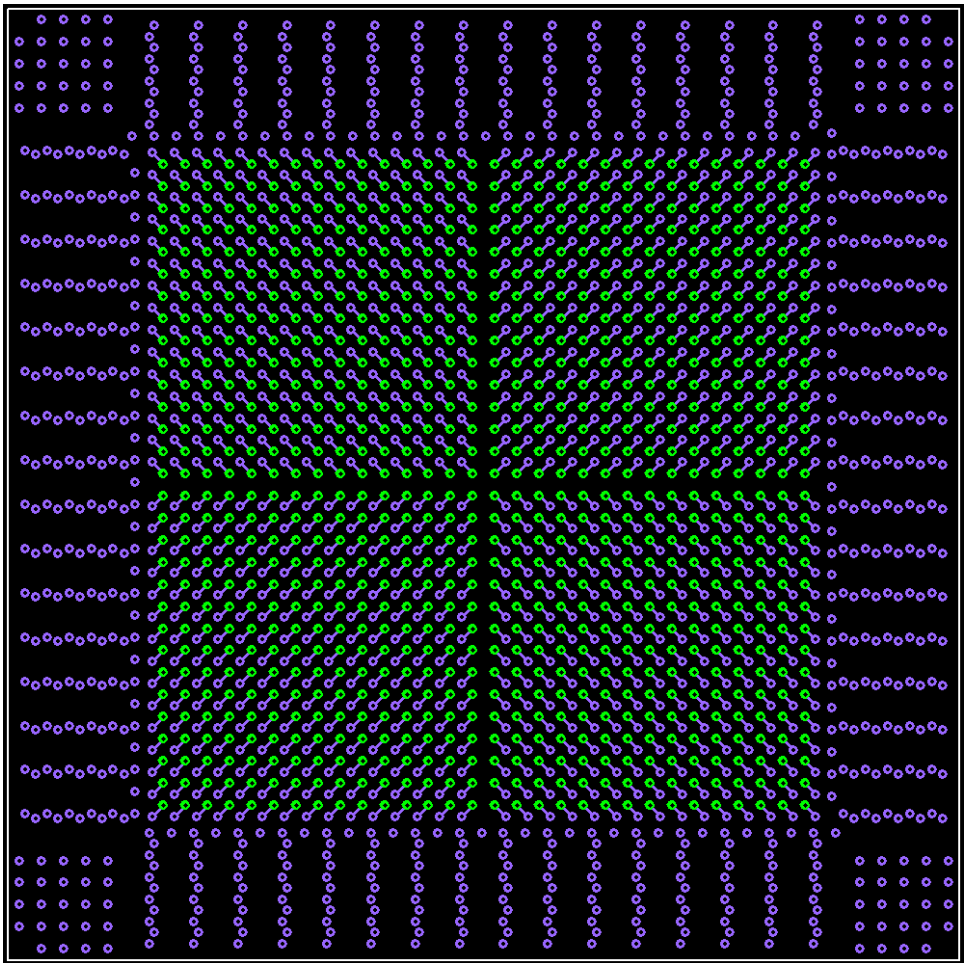


Figure 4-18: Layer 2 blind-vias (purple) with buried-vias (green)

Multiple Fanout Patterns

In Figure 4-17 above, you can see 4 different patterns.

1. **Quadrant dog-bone in the center.**
   The layer 1:2 blind-via uses a quadrant dog-bone pattern and then transitions to a buried-via. The power and ground pins that would need to run to the bottom of the board to connect to bypass

capacitors, or any signals that need pull-up resistors, would have another blind-via between layers n and n-1.

- One alternative to using the blind/buried/blind vias in the center would be to just put in a through-via either in a quadrant dog-bone pattern or via-in-pad configuration. This will simplify the fanout and since most of the pins in the center area are power and ground, it will not impact the route density in a significant manner.

2. **Quadrant dog-bone in the corners**.
   The corners of the BGA are always the easiest to breakout because you have half as many pins to route to the edge, split along the diagonal. Using a simple quadrant dog-bone pattern actually allows for more routing density than if you tried to mix some kind of staggered via pattern along the diagonal of the corner. See Figure 4-19. Most any pattern will result in the same number of escape traces plus or minus a few so you may as well go with a simple pattern.

3. **Short dog-bone in the transition areas**.
   The pins between the pins using the dog-bone via patterns and the shifted vias lack space for the fanouts. I recommend using a row around the perimeter for the transition as shown in Figure 4-19.

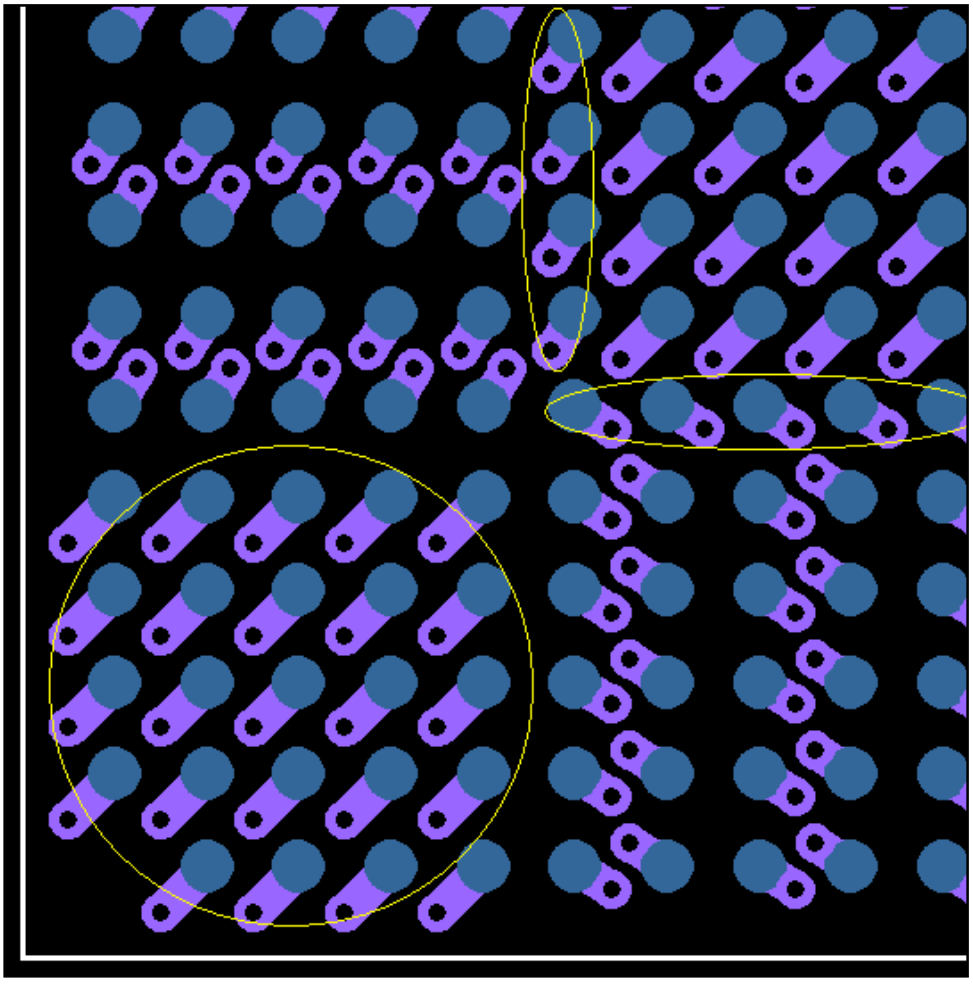


Figure 4-19: Corner via and transition via patterns

4. **Shifted Columns and Rows.**
   Using a blind-via pattern around the perimeter of the BGA, in which the vias are shifted into columns and rows, results in 24% greater route density per layer.

Shifted Columns & Rows

In Figure 4-20, the blind-vias are shifted into columns with the intent of opening up additional routing space. In Figure 4-21, you can see that significant space is created compared to the space in Figure 4-22. When comparing this to an unshifted matrix of vias, you can get 24% more escape traces out to the edge of the BGA when using minimum spacing.

If the ball pads are smaller and 0.6mm as in these examples (as would be the case if lead-free solder is used), you wouldn't be able to shift the vias into a tighter column since the blind-vias are already spaced at a minimum of 0.1mm (4th).

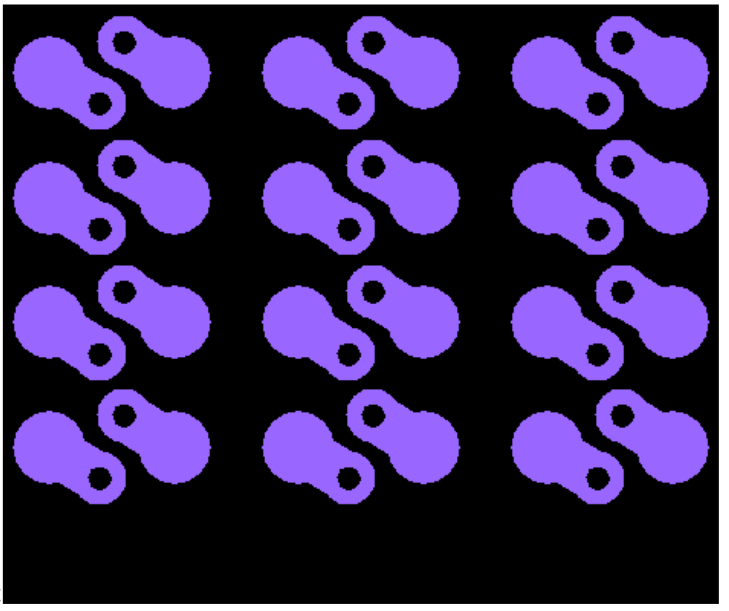
c 

Figure 4-20: Mount layer with frilled blind-vias shifted into columns

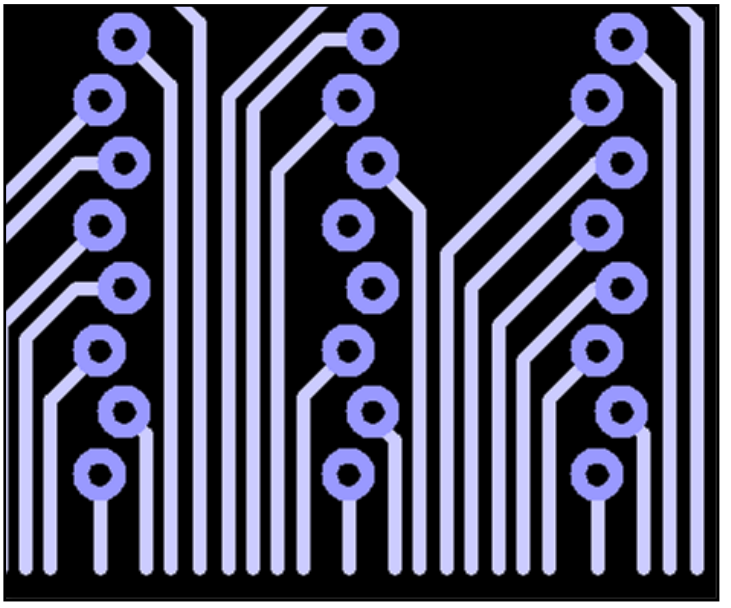


Figure 4-21: Layer 2 with drilled blind-vias shifted into columns

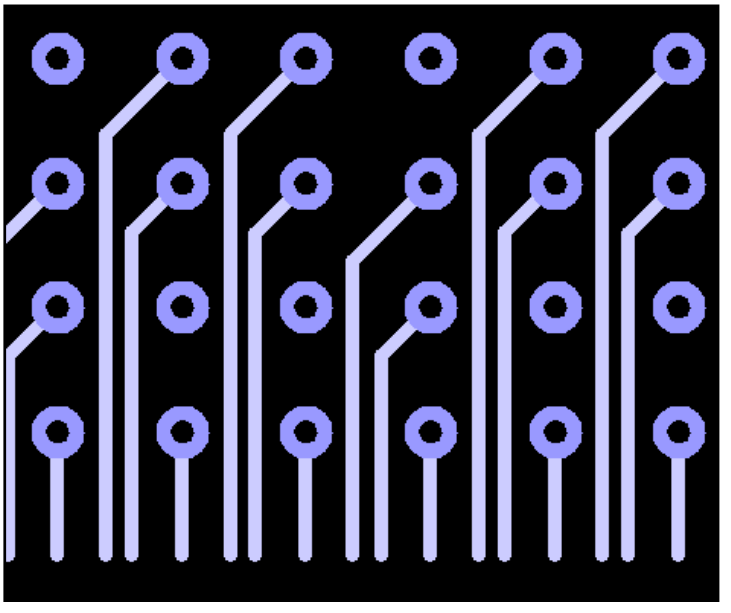


Figure 4-22: Layer 2 with blind-vias using a simple 1mm matrix

Advantages

- 24% increased route density per layer over through-vias and unshifted blind-vias.
- More room for a ground plane on the mount layer. It is not as much as can attained with the vias-in-pad; but certainly more than if the vias are centered in a simple 1mm matrix.
- If you route the high-speed single-ended nets on the layers using blind-vias, via stubs are eliminated and via-via crosstalk is minimized.
- Any signal routed on the blind-via layers, will not need to have a buried via, thus opening up route space on the buried via layers.

Disadvantages

- A blind and buried via stackup is more expensive than a through-via stackup.

Shifting Vias – General Principles

As shown above with blind-vias, it is clear that shifting the vias can increase route density. When using HDI micro-vias, shifting the fanout locations can improve route density even more. Increased route density means potentially fewer layers and lower cost. There are some general principles related to shifting vias that can help make the effort successful.

Differential Pair Coupling and Pin Swapping

When applying a shifted via pattern to increase route density, one of the effects that needs to be managed is the fact that as you transition through the layers with different patterns for via span, the differential-pair compliments may be spread away from each other in the process.

Figures 4-23 and 4-24 illustrate this problem. The ball pads for the differential-pair compliments are close to each other; however, as the fanout vias are added, they compliments get spread apart.

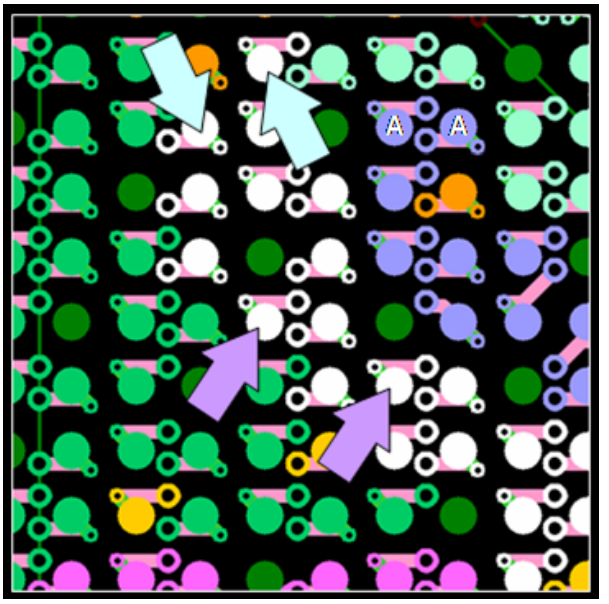


Figure 4-23: Differential pair coupling affected by shifting vias

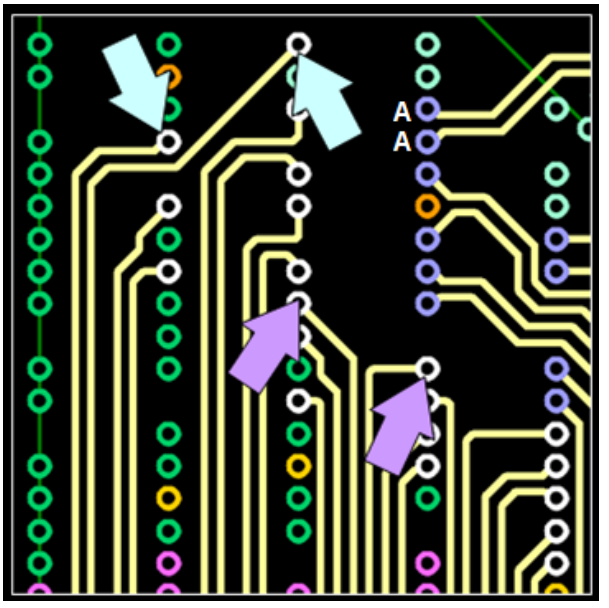


Figure 4-24: Differential pair coupling affected by shifting vias

A good solution, especially for FPGAs is to pin swap so that the ball pads are aligned in a manner that results in the fanout vias remaining close to each other. In the above figures, swapping the differential-pair compliments into the “A” and “A” locations will optimize the coupling.

- The ability to swap pins will be limited by bank locations and power and ground pin distribution.
- Finding the most effective swapping patterns (aligned vertically or horizontally or on a diagonal) will depend on the fanout via pattern used in that area.

Reducing Effective Size of the BGA

In Figure 4-17 the BGA has 1760 pins. If the five columns/rows of ball pads around the perimeter can be routed on the blind-via layer (layer 2), then the effective size of the BGA to be routed on the buried-via layers (Figure 4-25) has become 1024. At that number of pins, breakout and routing of the BGA is no longer the primary contributor to layer count, especially since the innermost pins in most BGAs are dedicated to power and ground.

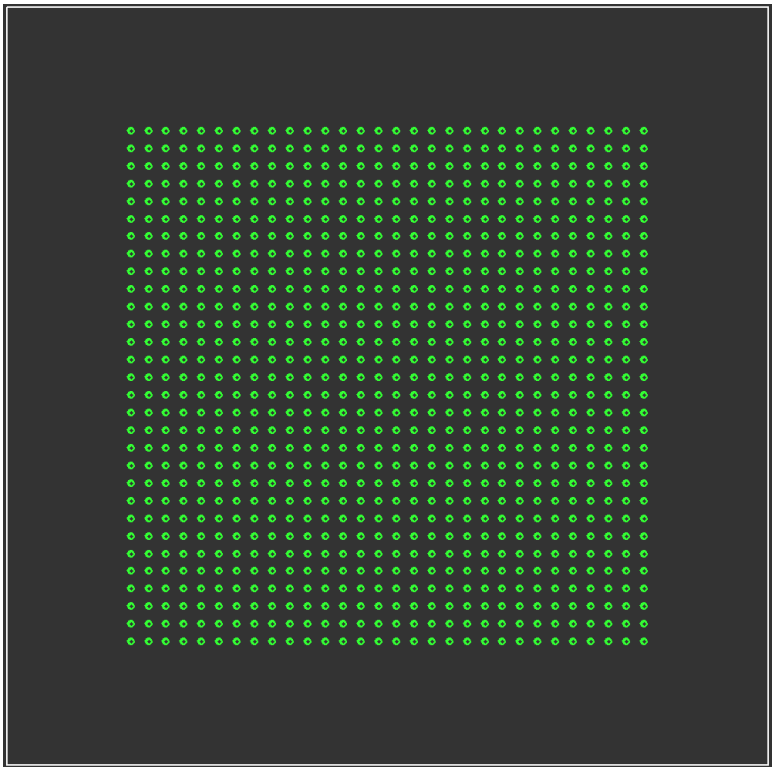


Figure 4-25: Layer 3 buried-vias

HDI Micro-Vias

Fanouts for laser drilled micro-via stackups use the same principles as with mechanically drilled blind & buried vias. The variety of stackups and smaller via sizes provide for tighter shifted column and row patterns, improved route density and greater flexibility in assigning routes to buildup layers as opposed to laminated cores.

When using HDI, the blind micro-vias allow for greater route density and therefore potentially fewer total layers required for routing. Of course the number of layers accessible by the micro-vias will significantly affect the

overall route density. The fanout patterns analyzed in this context will be for the following types of HDI construction:

- 1+N+1 = Type II (layer 1:2 micro-vias with buried vias in laminated core)
- 2+N+2 = Type III (layer 1:2, 2-3 micro-vias with buried vias in laminated core)

Layer 1:2 micro-vias (1+N+1)

If Layer 1 is used for a ground plane and not for routing, then the fanouts need to be patterned to maximize layer 2 route density. The same patterns for the blind-vias can be used for micro-vias; however, since the micro-vias are smaller, you can compact them more and gain additional route space.

In Figure 4-26, the 1:2 micro-vias are aligned in columns (and rows) to maximize route density (12% improvement over shifted blind-vias, 36% improvement over quadrant dog-bone through-vias)

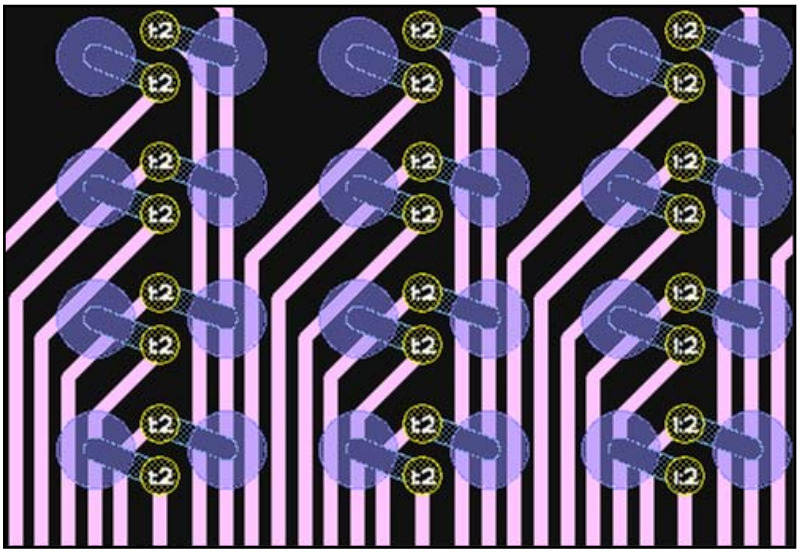


Figure 4-26: Micro-vias aligned

Figure 4-27 shows how route density can be increased when using via-in-pad methods. If the vias are shifted inside the pads, you can open up additional room for the escape traces.

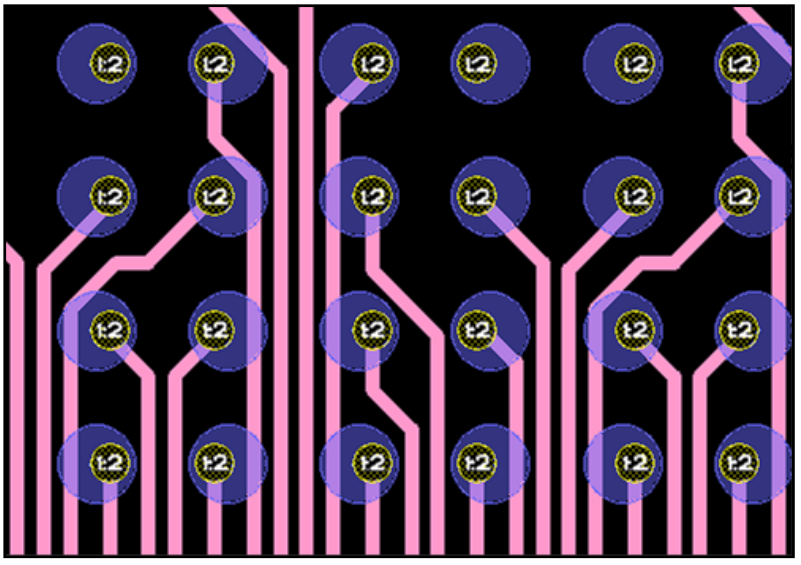


Figure 4-27: Micro-via pattern using via-in-pad method

If only one layer is available for the escape traces as is the case with a 1+N+1 stackup that has a ground plane on the surface layer, then it is important to use a shifted via pattern that is allows for aligned micro-vias around the BGA perimeter and space for the power and ground to extend through the board with additional buried and blind-vias.

Layer 1:2, 2-3 micro-vias (2+N+2)

Again assuming the layer 1 will not generally be used for routing, then the fanouts need to be patterned to maximize layer 2 and layer 3 route density. With layers 2 and 3 available for routing with micro-vias, you can use either a quadrant style breakout or layer biased. This shows how effective the general principle of aligning the vias works to open additional route space on the inner layers.

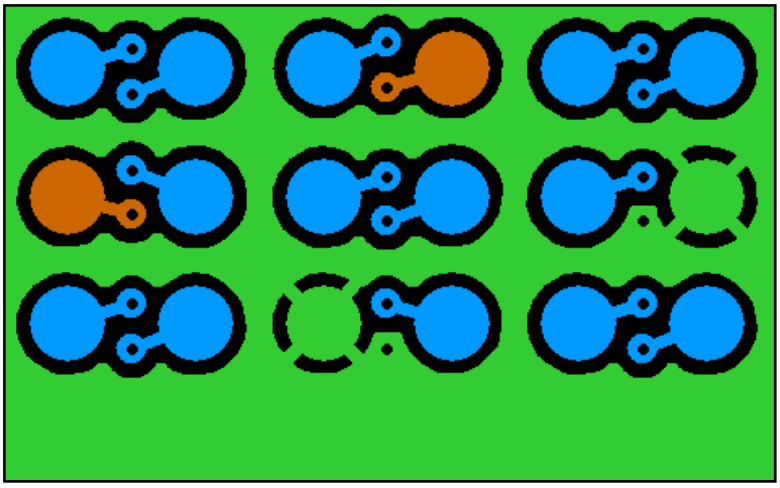


Figure 4-28: Layer 1 with 1:2 micro-vias for all ball pads

The above figure shows plenty of room on the mount layer for the ground plane to fill with little interruption. The shifting of vias not only provides additional route density, it also opens space for ground fill. Also note how nicely in Mentor Graphics Expedition PCB the ground via fits and the copper fill and clearance around it provides for good manufacturing.

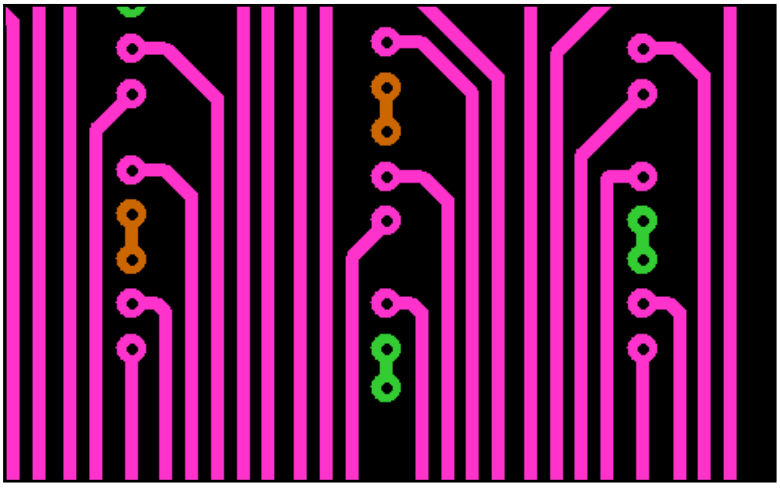


Figure 4-29: Layer 2 escape traces and micro-vias

In Figure 4-29 note the significant space for routes after shifting the vias. In this case, the traces are routed as single-ended nets; however, if the nets were differential pairs, there would be plenty of room to route three sets of differential pairs between the aligned vias. Of course actual amounts may vary depending on design rules.

The power (orange) and ground (green) vias are paired because you are seeing not only the 1:2 vias, but also the 2:3 vias.

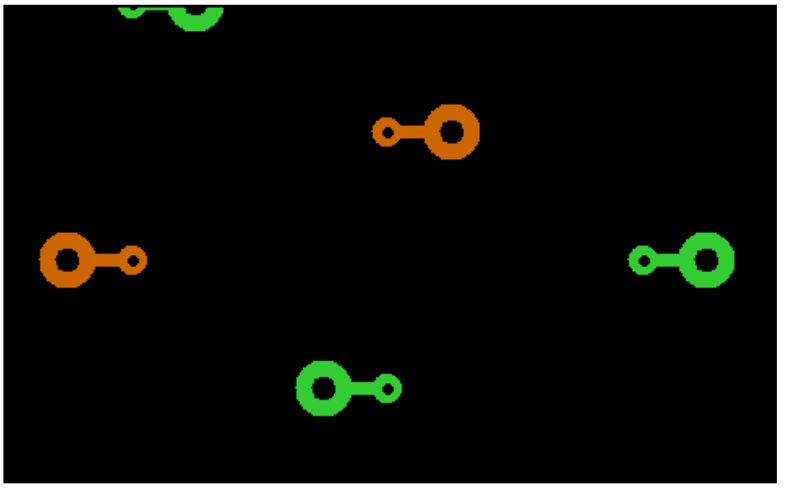


Figure 4-30: Layer 3 with 2-3 micro-vias and buried-vias

The large via is the buried-via that extends through the laminated core.

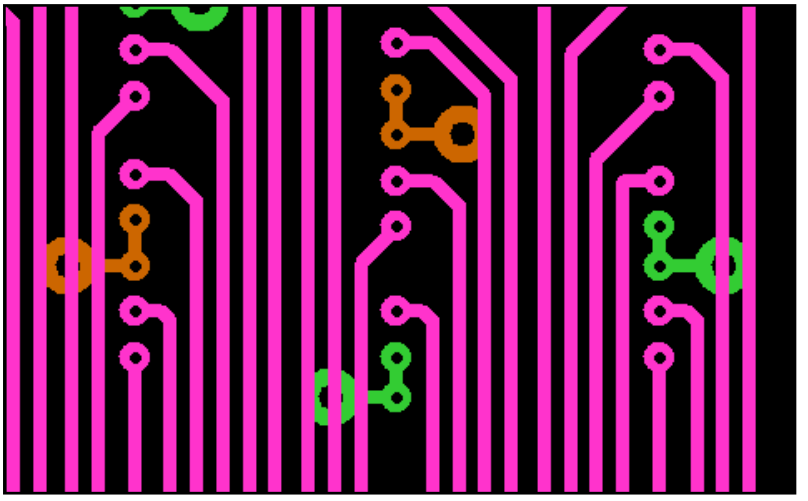
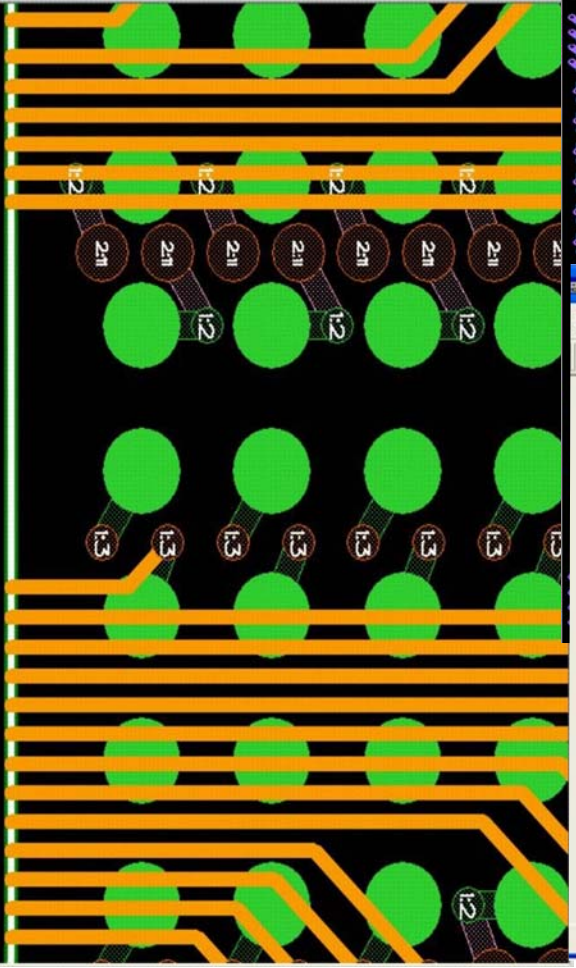


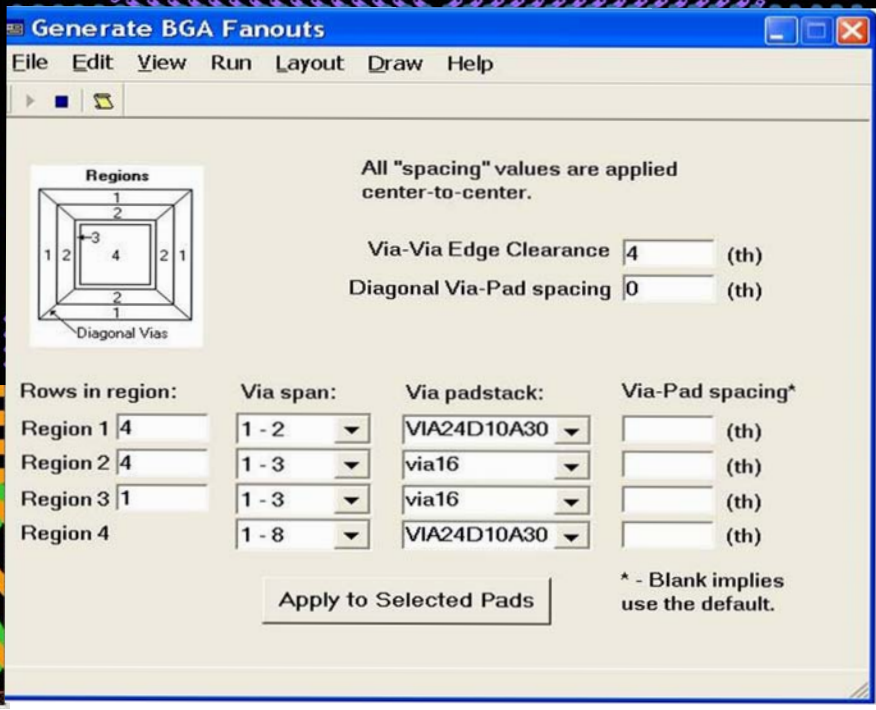
Figure 4-31: Layers 2 and 3 shown together

In Figure 4-31 you can see the combination of layers 2 and 3 with the escape traces on layer 2 and the wide open space for traces on layer 3.

Summary

Effective fanout patterns can increase the route density significantly. Designs with through-vias have limited options under BGAs. When using laminated blind-vias, route density can be increased 24%. HDI micro-vias enables the possibility of increasing route density by 36%. My discussion in this chapter clearly shows that using blind-vias or micro-vias and aligning them is a very effective method for potential layer reduction through increased route density.





PRINTED CIRCUIT BOARD DESIGN

Designing with HDI / Microvia Technology

Driven by the need for denser, higher performing, and lower cost products, the use of High Density Interconnects (HDI) and Microvias is rapidly emerging in many industries. By using this technology a designer can effectively break out from dense, fine pitch BGAs, reduce PCB layer counts and size, and improve performance.

But designers need the tools that fully understand the complex via stacking rules as well as automate the routing process. Mentor's Expedition Enterprise and Board Station XE flows enable highly efficient automatic and interactive routing of HDI/Microvia layers to provide the productivity you need to get the job done quickly and develop the most competitive products for your company.

To connect with other innovators and visionaries
of future HDI and microvia technology
join Mentor's PCB community at
http:// communities.mentor.com, call us at 800.547.3000
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Chapter Five - Layer Biased Breakouts

This chapter communicates my findings during this study of a real design with 19 large BGAs. The primary goal was to reduce the layer count, maintain signal integrity and obtain a high percentage of automatic routing completion.

Board Description

- 18”x14”
- 34 layers, 22 signal layers
- HDI with 2 buildup layers on top and bottom, 30 layer laminated core inside.
- 52,513 pins
- 11,529 nets
- 7,729 parts
- 18 BGAs each with 1513 pins/1mm pitch (Xilinx Virtex-4 XC4VLX100 FPGA)
- 1 BGA with 1520 pins/1mm pitch (Xilinx Virtex-4 XC4VLX200 FPGA)

General Assessment of Original Board

It should be possible to design this board in 16-18 layers, 10 of which are signal layers. What are the significant difficulties to attaining this goal?

- Crosstalk is an overriding concern and therefore the desire to spread traces apart as much as possible to fulfill accumulative parallelism rules.
- The sheer volume of nets to be routed eliminates the feasibility of interactively routing the board.
- A significant number of tuned differential pairs.
- An average of 240 bypass capacitors per FPGA, located on the opposite side of the FPGA. This large number of capacitors requires all the power and ground pins to have fanouts that go all-the-way

through the board. This requires considerable space and prevents use of some breakout methods that could help in routing the signals.

Recommendations and Solutions

Stackup

Reduce the layer count to 16 or 18 layers with 10 signal layers.

Fanout Patterns

The need is to develop fanout patterns that facilitates routing and supports the requirement for so many bypass capacitors. Also consider a stackup that provides excellent direct coupling between power and ground by using buildup layers and a very thin dielectric, thus reducing the need for such a large number of bypass capacitors.

Rule Areas

Use Rule Areas around the BGAs to enable spacing that provides dense routing in the area under the device and wide spacing between traces outside the BGA areas.

Stackup

The stackup used for this study is 16 layers using micro-vias and buried vias in a common HDI structure. See Figure 5-1.

- Red = laser drilled micro-vias, 10th pad, 4th hole
- range = mechanically drilled buried-vias, 18th pad, 8th hole

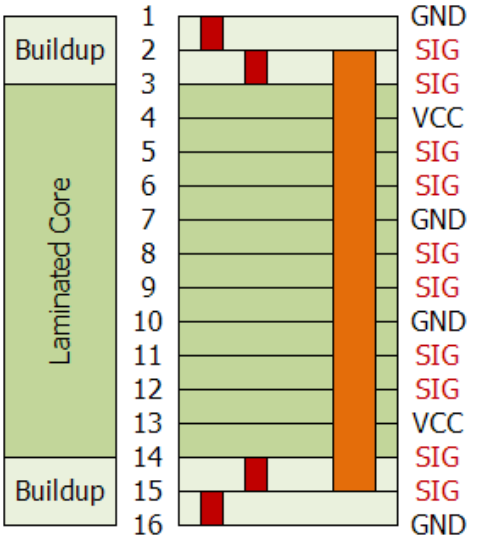


Figure 5-1: 2+N+2 HDI stackup

Using Layer Biased Breakouts

What are “layer biased breakouts”? The traditional breakout trace pattern has traces running North, South, East and West (NSEW) on the same layer. This is quite good for density purposes, especially on a design that has 4 or less signal layers. When a design has over 8 or more signal layers, it is better to have the breakout traces match the layer bias. The layer biased breakouts allow much higher auto route completion rates because the auto router is inherently biased.

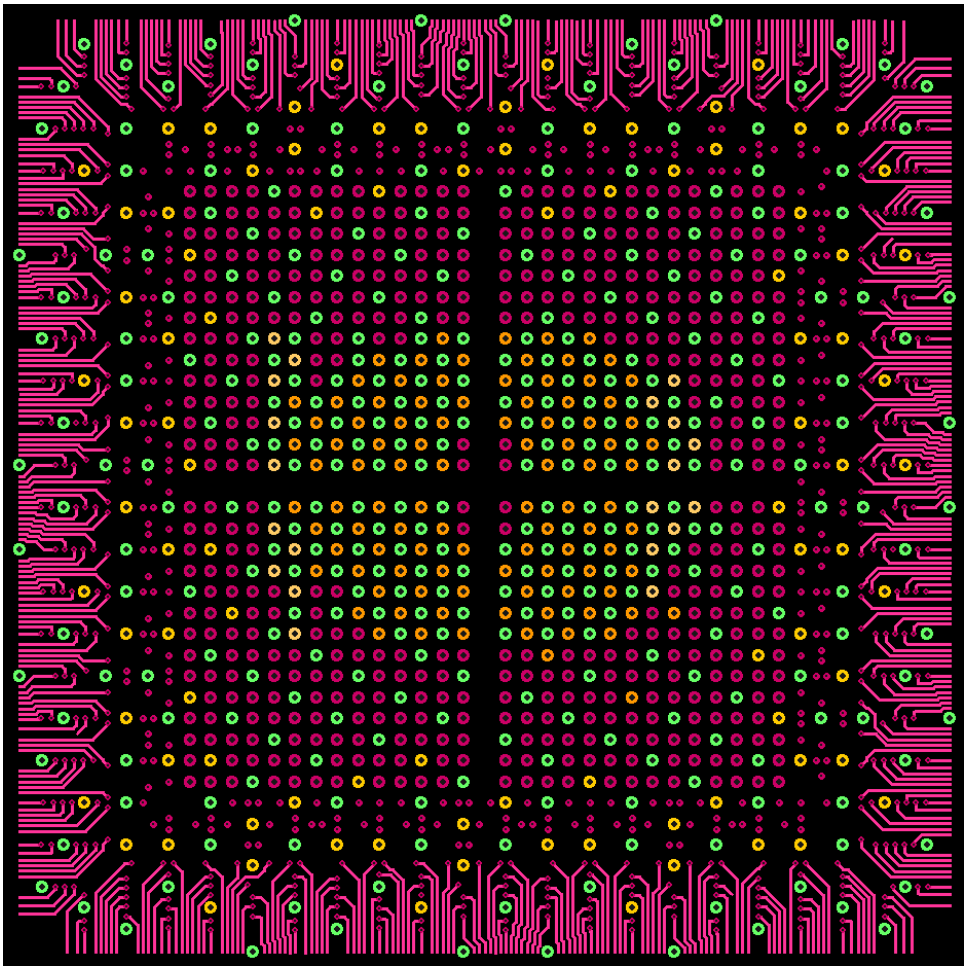


Figure 5-2: NSEW breakouts

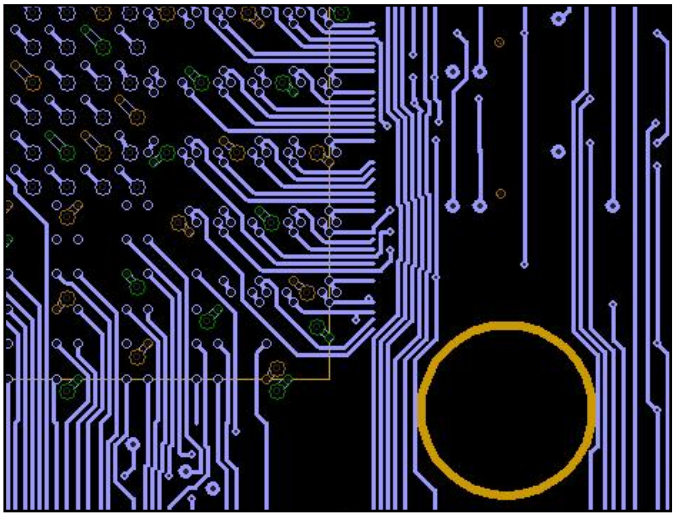


Figure 5-3: Routing with NESW escape traces

In Figure 5-3 that the NESW escape traces are blocked by a normally biased autorouter. This shows a problem with NSEW breakouts when trying to auto route with a layer biased router. The breakouts that are perpendicular to the layer bias are not going to be routed.

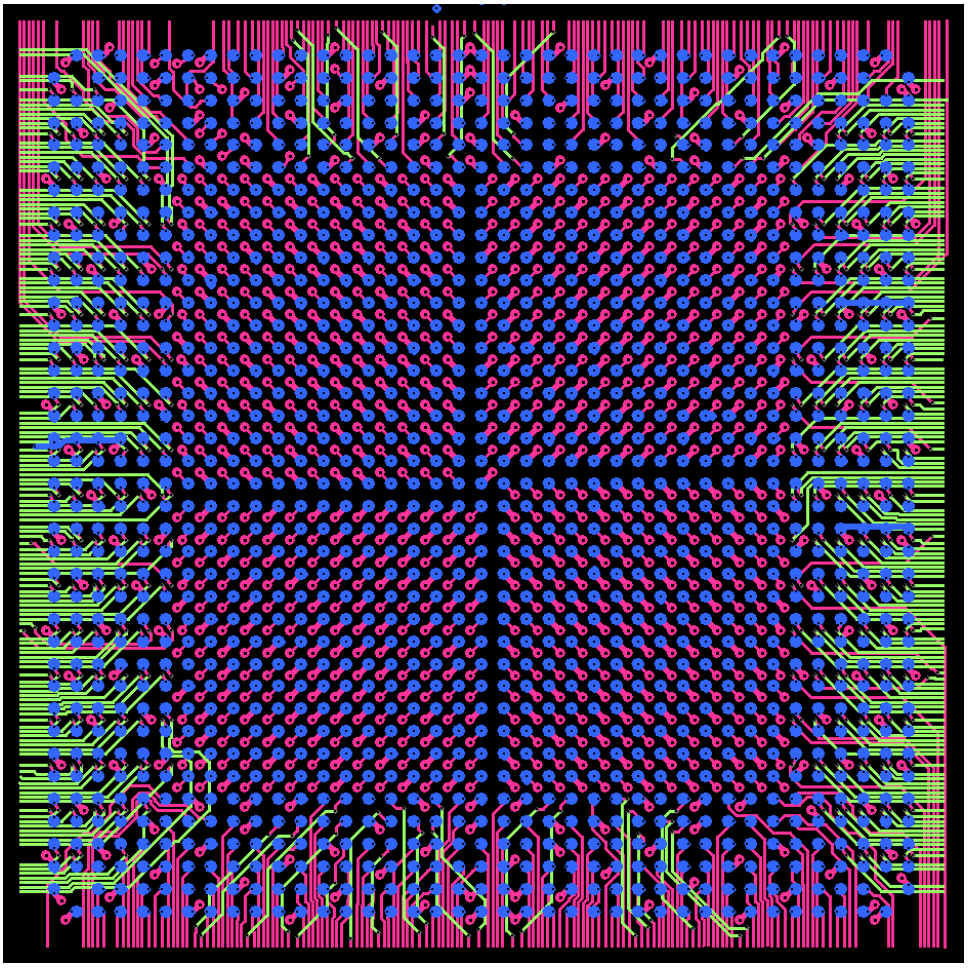


Figure 5-4: Layer biased breakouts

In the above image, the green traces are on the horizontally biased routing layer and the red on the vertical. This kind of bias is more natural for an autorouter and if the escape traces are generated in the direction of the target pin, the routing effectiveness is even higher.

Notes

- Multiple fanout patterns will be needed to support the bias and to most effectively use the buildup layer micro-vias.

- Use Rule Areas around the BGAs to enable spacing that provides dense routing in the area under the device and wide spacing between traces outside the BGA areas.

Fanouts for Micro-Via Layers

Vertical Biased Layer 15: Via-In-Pad

The layer 16-15 micro-vias were placed in the pad on the edge. This is a rule that can be specified for individual pads. The intent was to enable five route paths where the via space was maximized and one route path where the via space was minimized.

- I also changed the Ball Pad size to ROUND_0.25 (from ROUND_0.1811) so that the vias could be spread sufficiently and still stay inside the pad.
- If a smaller solder area is desired, you can either make the ball pad smaller and have a “near via-in-pad” or use a smaller opening in the soldermask to control the effective soldering area for the BGA ball.

If the via is simply placed in the center of the pad, the number of total routes between four ball pads would have been six compared to sevenwith the vias spread in the manner shown in the figure below.

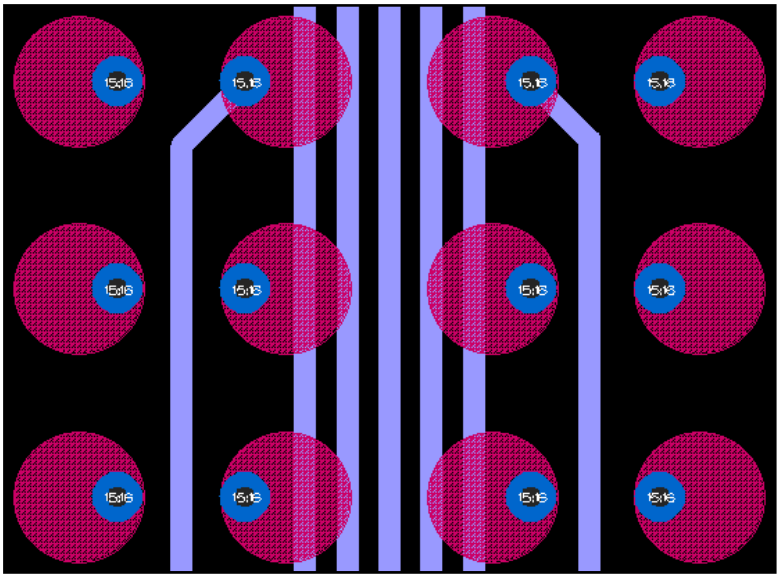


Figure 5-5: Layer 16-15 fanouts

You might be thinking, “One trace? What’s the big deal?” Figure 5-6 shows the fanouts and escape traces when the buried-vias are added for power and ground. There is less room for the traces. However, compared to if the micro-vias vias were just placed in the center of the pad and the buried vias staggered from that location, there is more total room for traces. This method makes it so that the buried-via eliminates one trace at most.

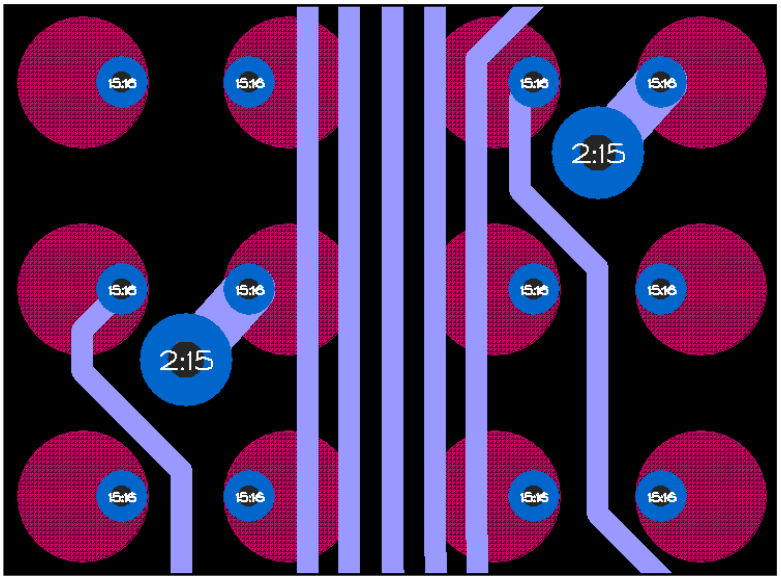


Figure 5-6: Layer 16-15 fanouts with buried vias for power and ground

Horizontal Biased Layer 14

The micro-vias are staggered in a different manner because to get to layer 14, a 16-15 micro-via and a 15-14 micro-via are required. I have considered using a 16-14 via, and indeed, that may be a better method but I haven't tried it yet on this board.

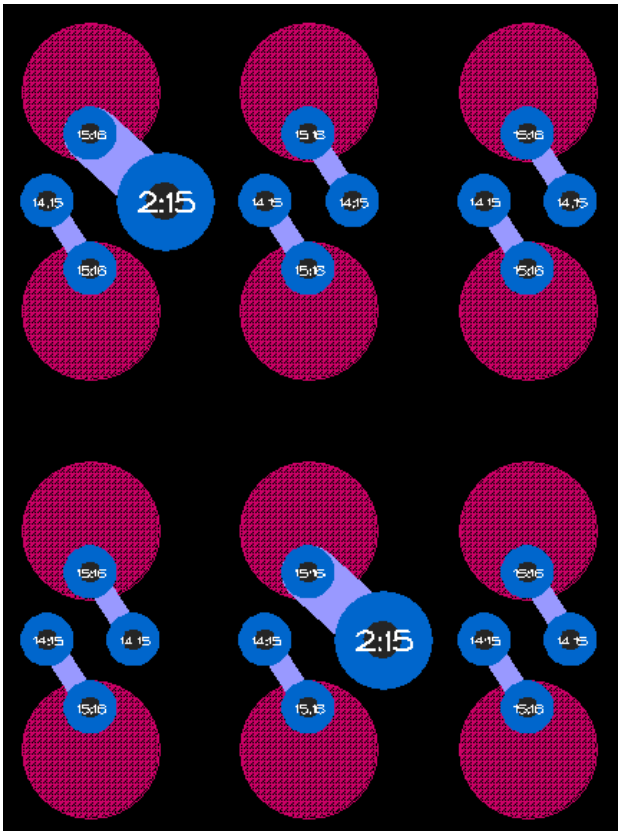


Figure 5-7: Layers 16, 15, 14 fanouts without escape traces

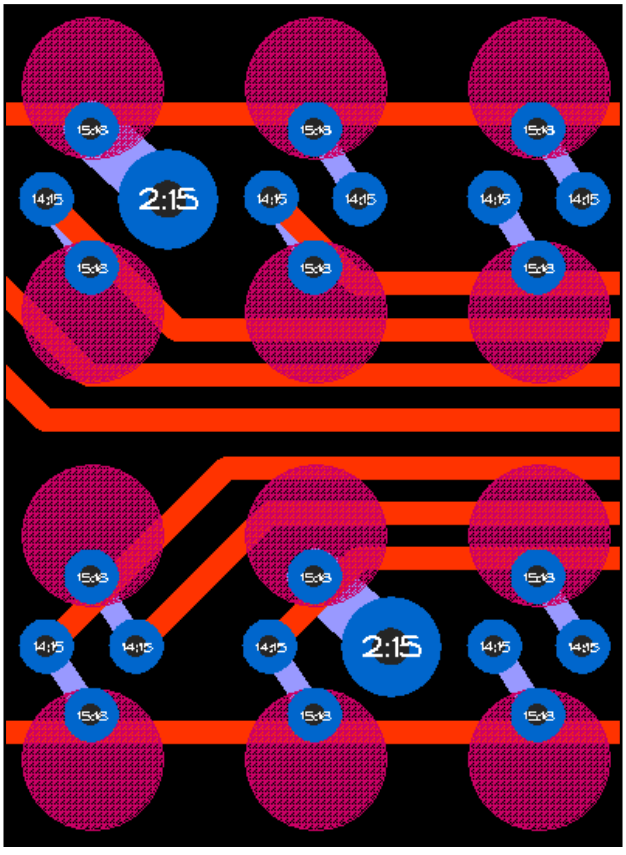


Figure 5-8: All layers shown with fanouts with escape traces

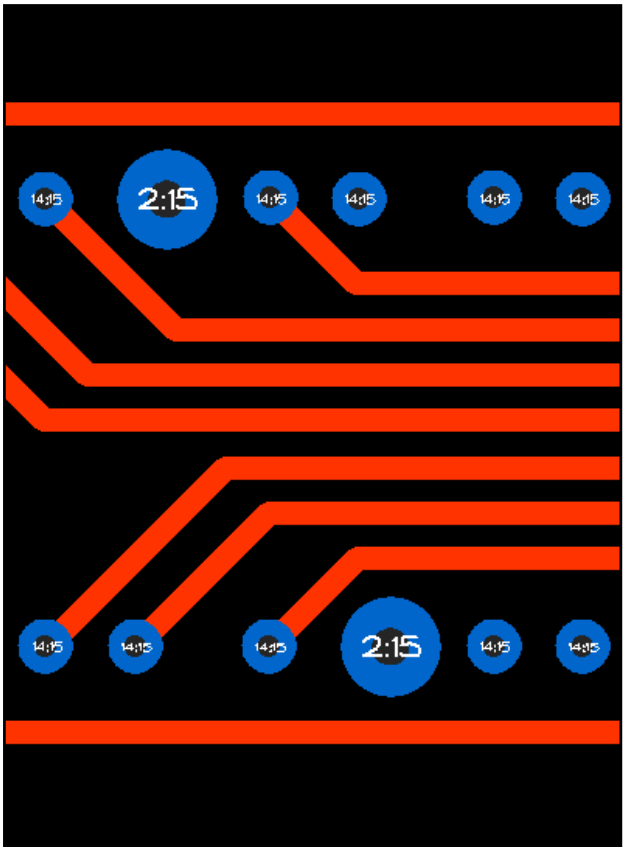


Figure 5-9: Layer 14 fanouts with escape traces

Micro-Vias, Row Depth

One question that had to be resolved before completing the fanouts was how many rows will use the fanout patterns with micro-vias? This question needs to be asked each time the breakout task is done because the answer will affect the route-ability.

- Initially four rows were attempted, which left a total of 961 pins in the center to be routed using the buried-vias. The breakout task was fairly simple and straightforward.
- Then six rows were tried, (729 remaining pins in the center) which made it more difficult to do the breakouts because there were more pins that had to fit breakouts on layers 14 and 15.

- In the end, the auto routing showed higher total completion rates with six rows of pins. A high “total” completion rate for auto-routing is the goal of effective breakouts, especially on very large designs with upwards of 10,000 nets.

Once the fanout patterns were established, different escape routing patterns can be explored. As mentioned previously, the first attempts with NSEW breakouts resulted with ineffective auto-routing due to the fact that the bias of the escape traces was in conflict with the layer bias. Indeed, the auto-router performed so much better with layer biased breakouts.

Does this mean that NSEW breakouts are useless? No, in fact, on boards with four or less signal layers, NSEW breakouts are much more effective because with so few routing layers, the routes usually end up unbiased and often the routing is done manually.

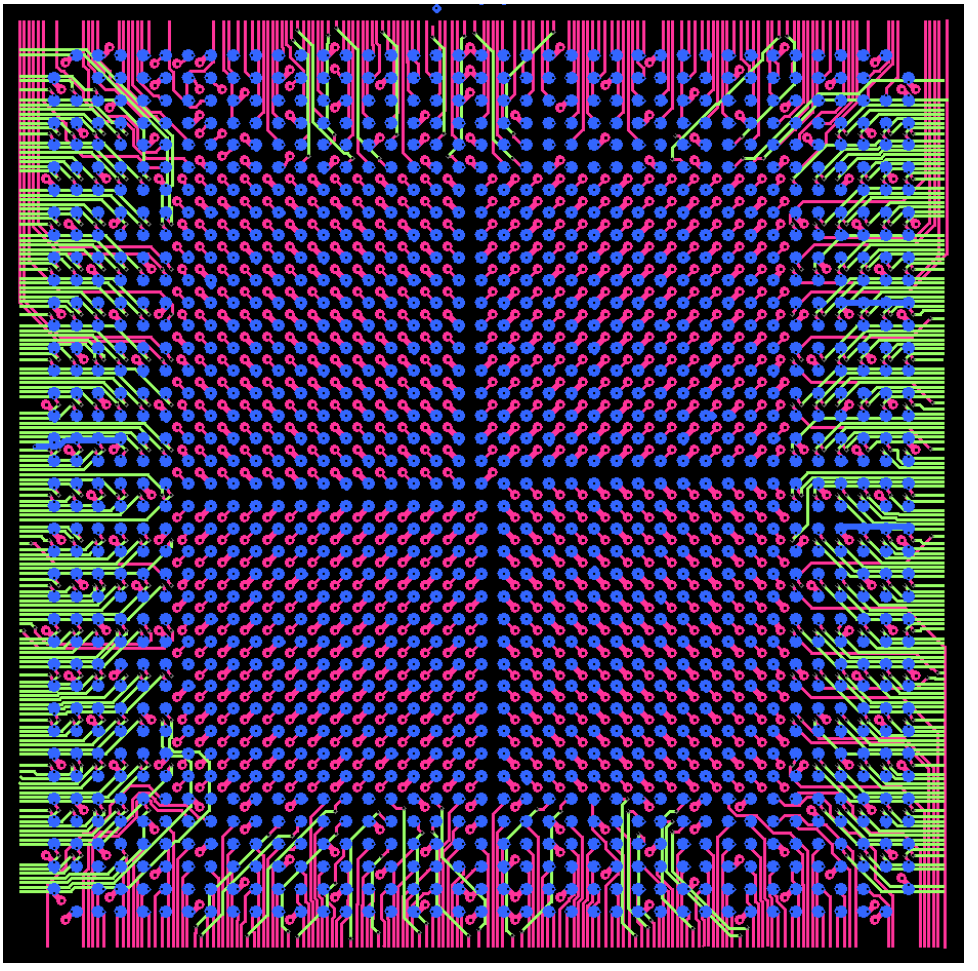


Figure 5-10: Layers 15 and 14 layer biased breakouts

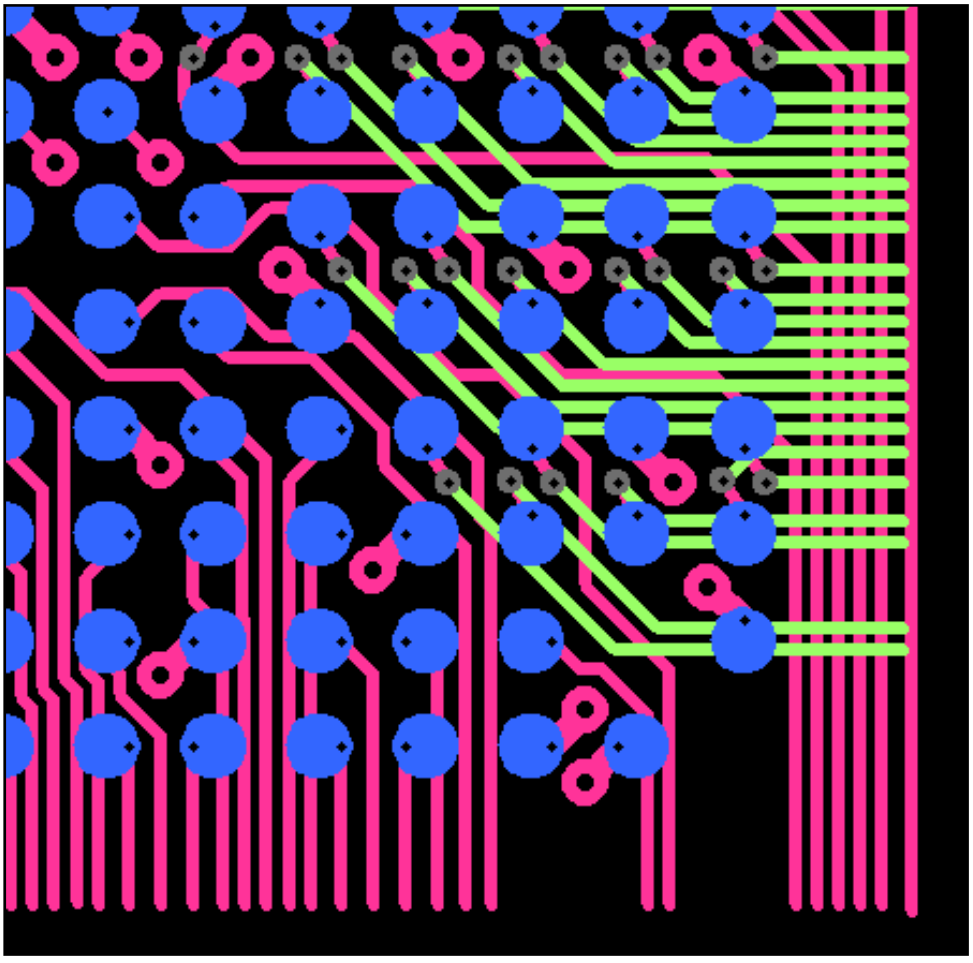


Figure 5-11: Layers 15 & 14 lower right detail

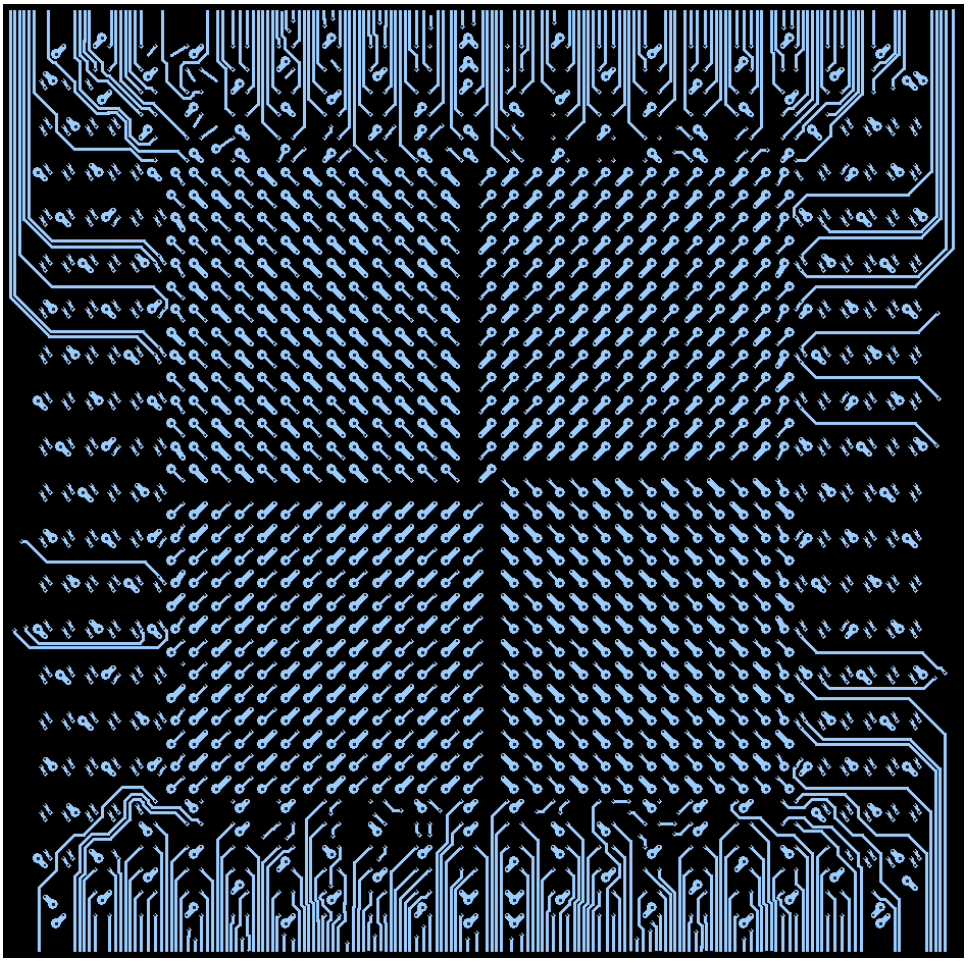


Figure 5-12: First signal layer

This layer has a vertical bias and the netlines that are generally in the vertical direction are routed on this layer using the micro-vias. There are some horizontal routes, but notice they have an additional via to bring it to the nearest horizontal layer. Of course if you don't want additional vias, try to find a horizontal layer that has room to route to the original fanout via.

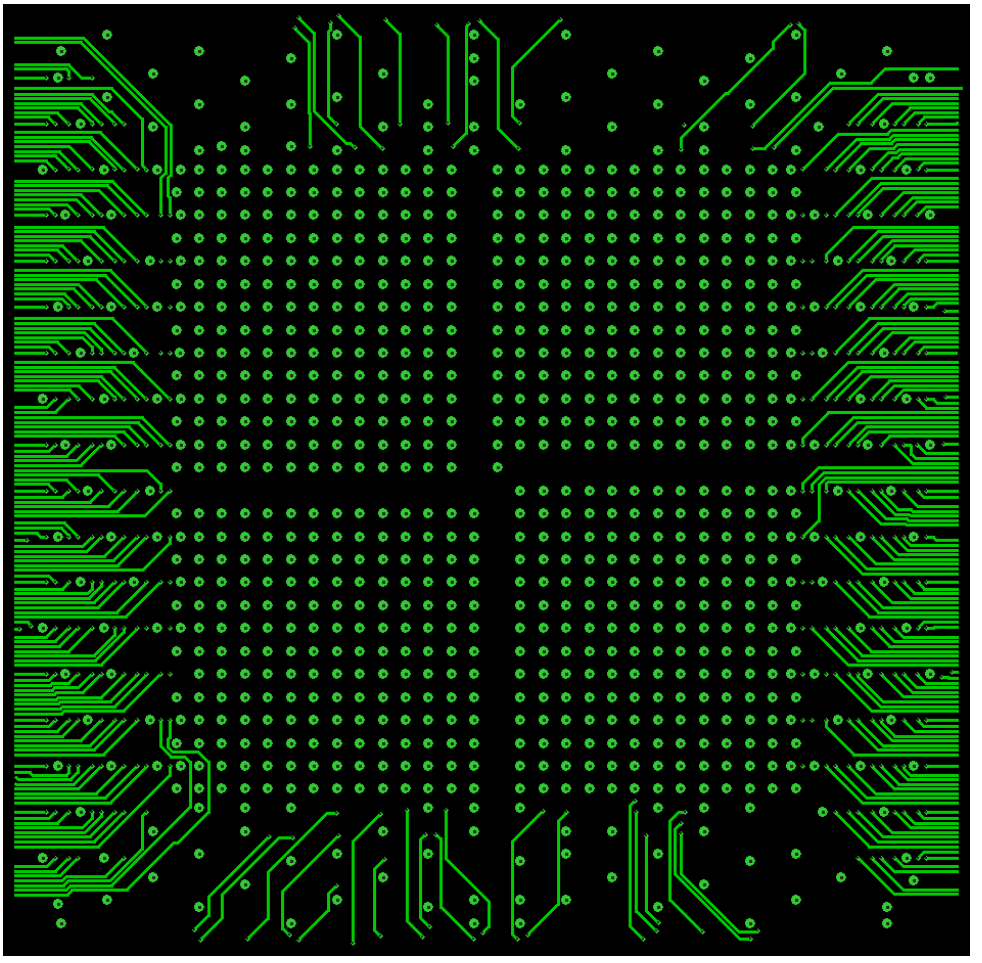


Figure 5-13: Second signal layer

Similar to the first layer using the micro-vias, except this layer has a horizontal bias.

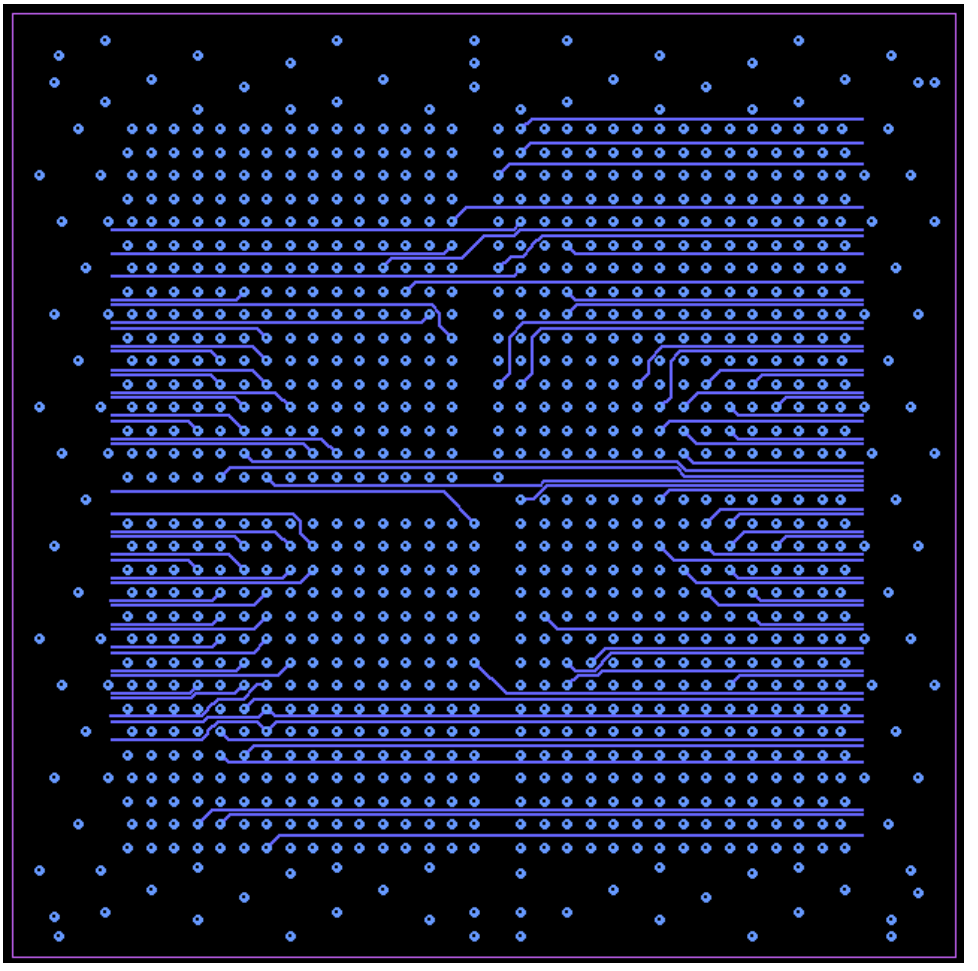


Figure 5-14: Buried via layer biased breakouts

These escape traces are for the netlines that run in a horizontal direction. You can see this clearly in Figure 5-15. Not all the netlines are strictly horizontal, rather generally horizontal and at least valid for a horizontally biased routing layer.

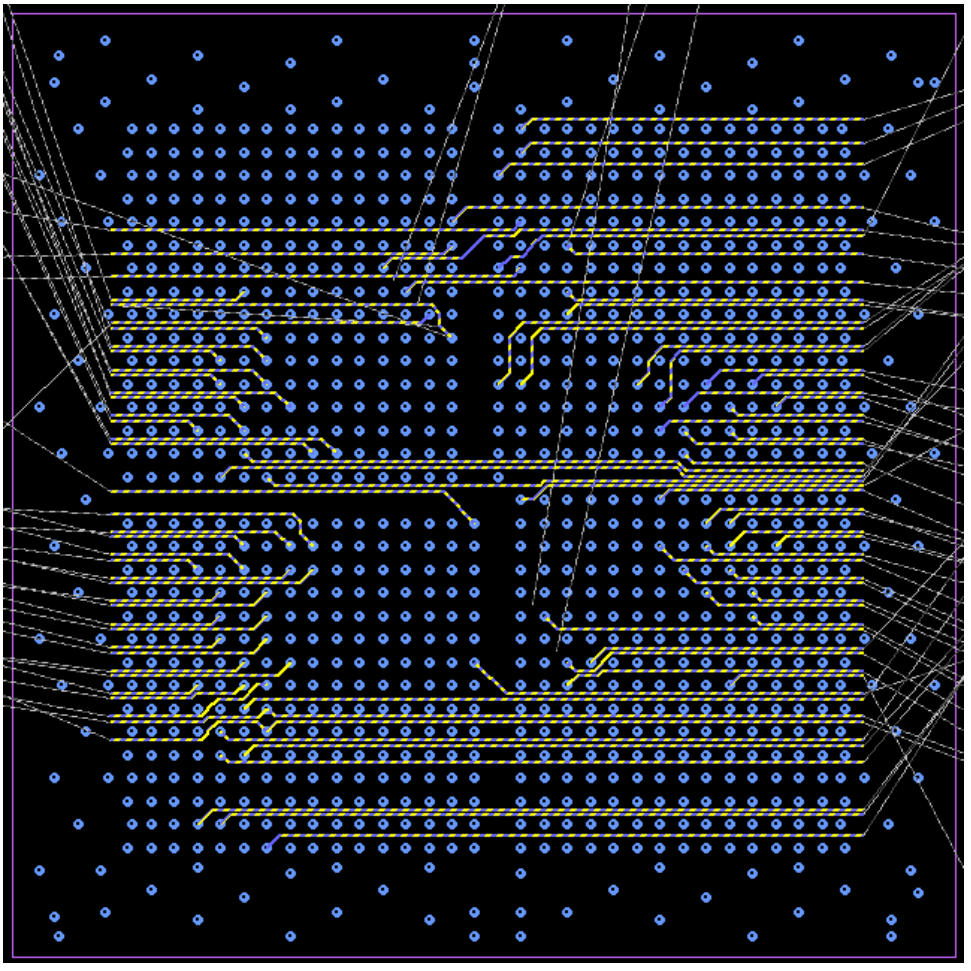


Figure 5-15: Nets selected to show direction of netlines

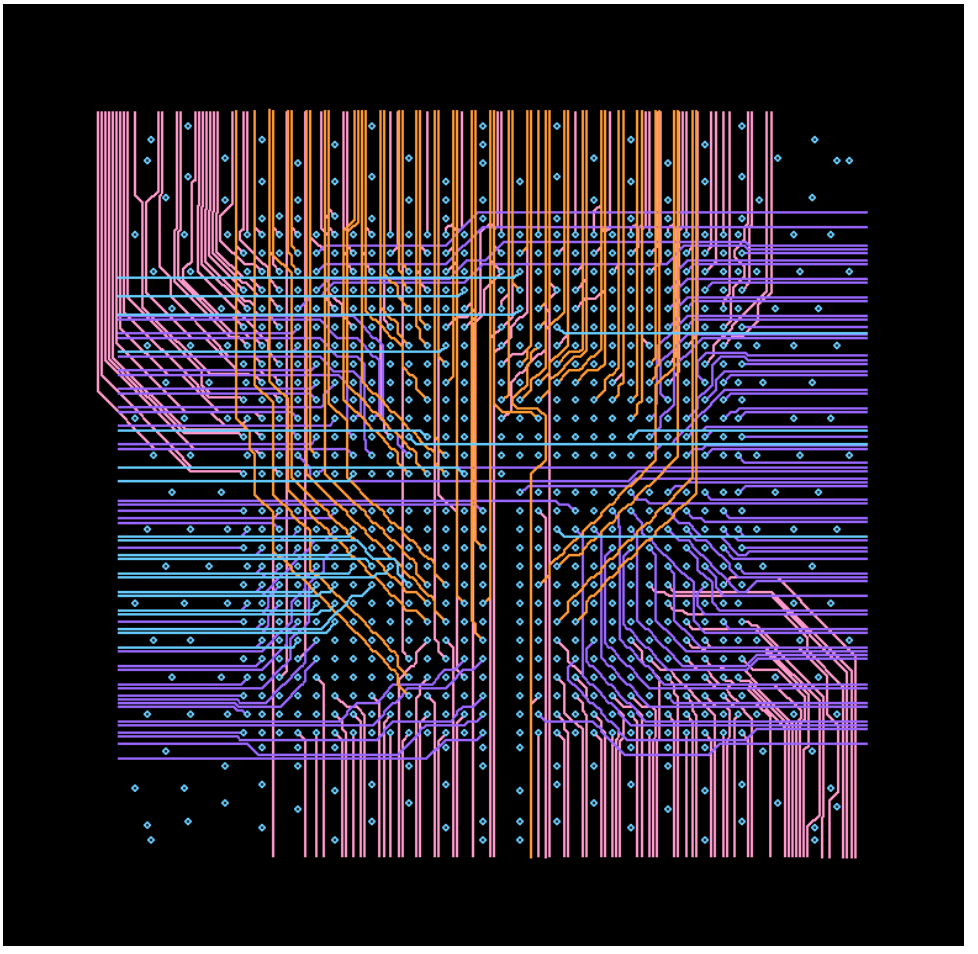


Figure 5-16: Escapes on all layers using buried-vias

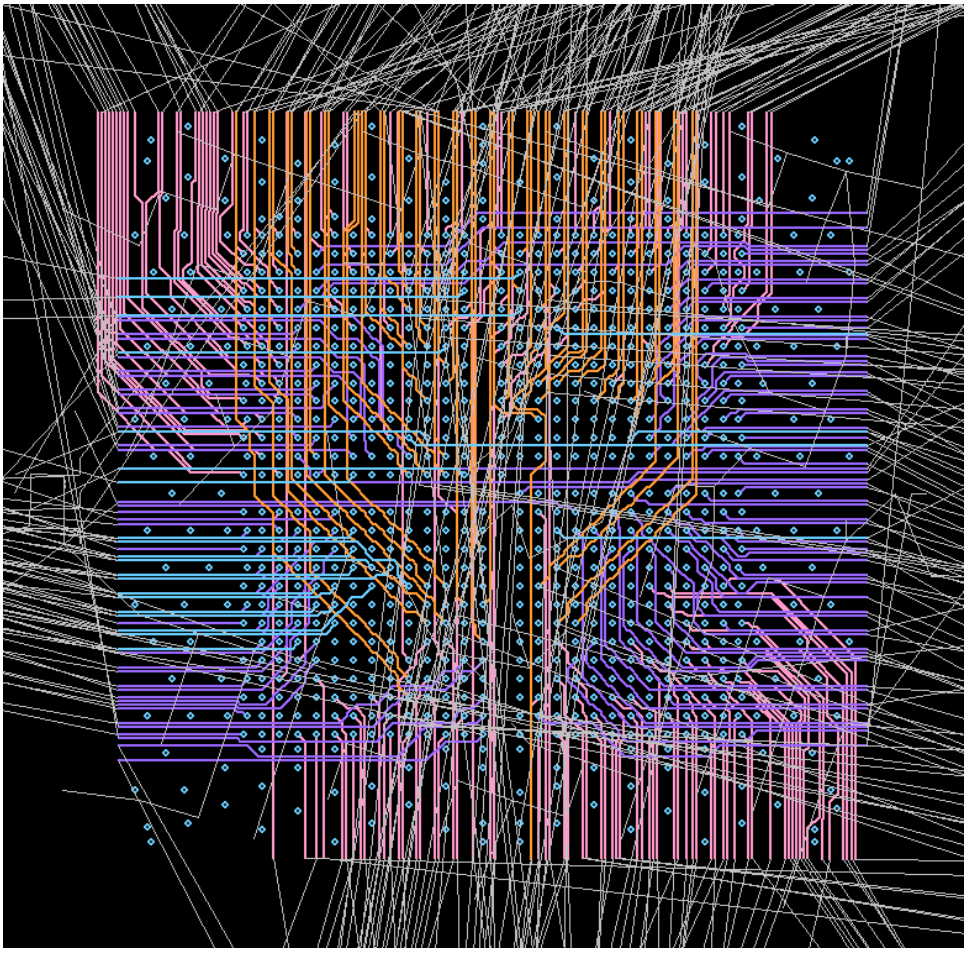


Figure 5-17: Netlines for escapes on buried-via layers

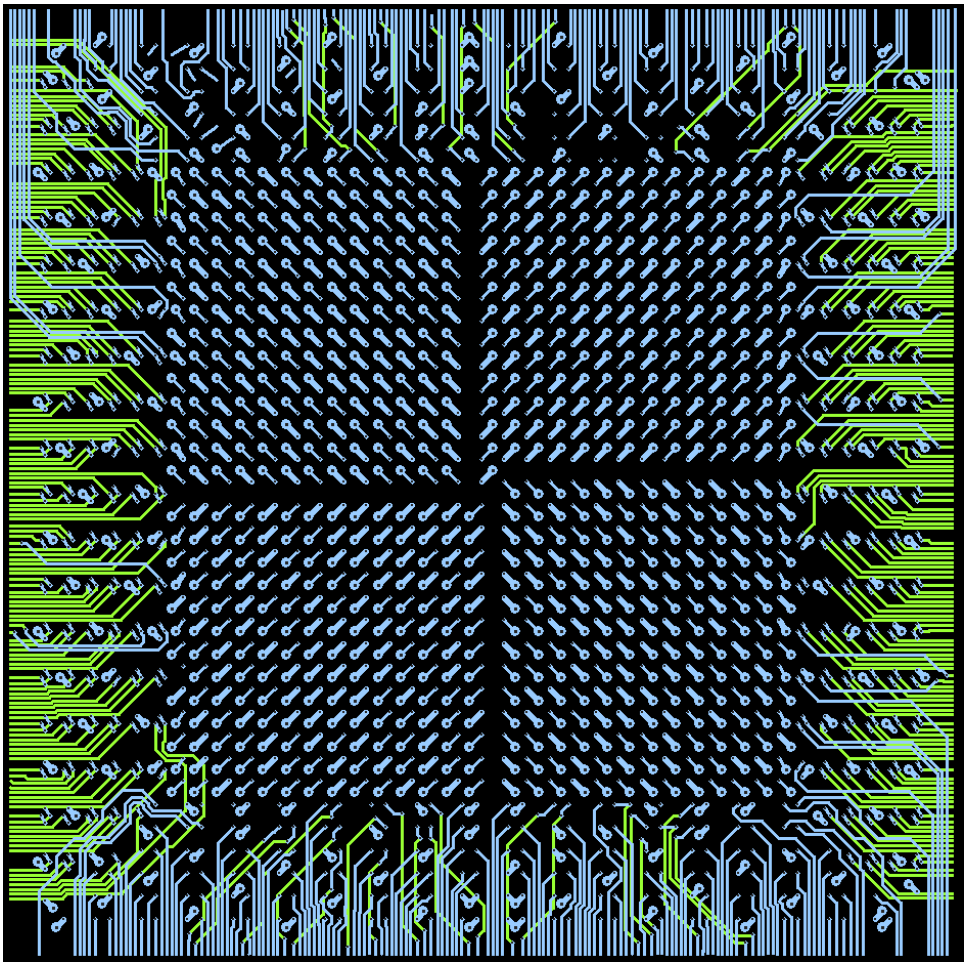


Figure 5-18: Signal layers 1 and 2

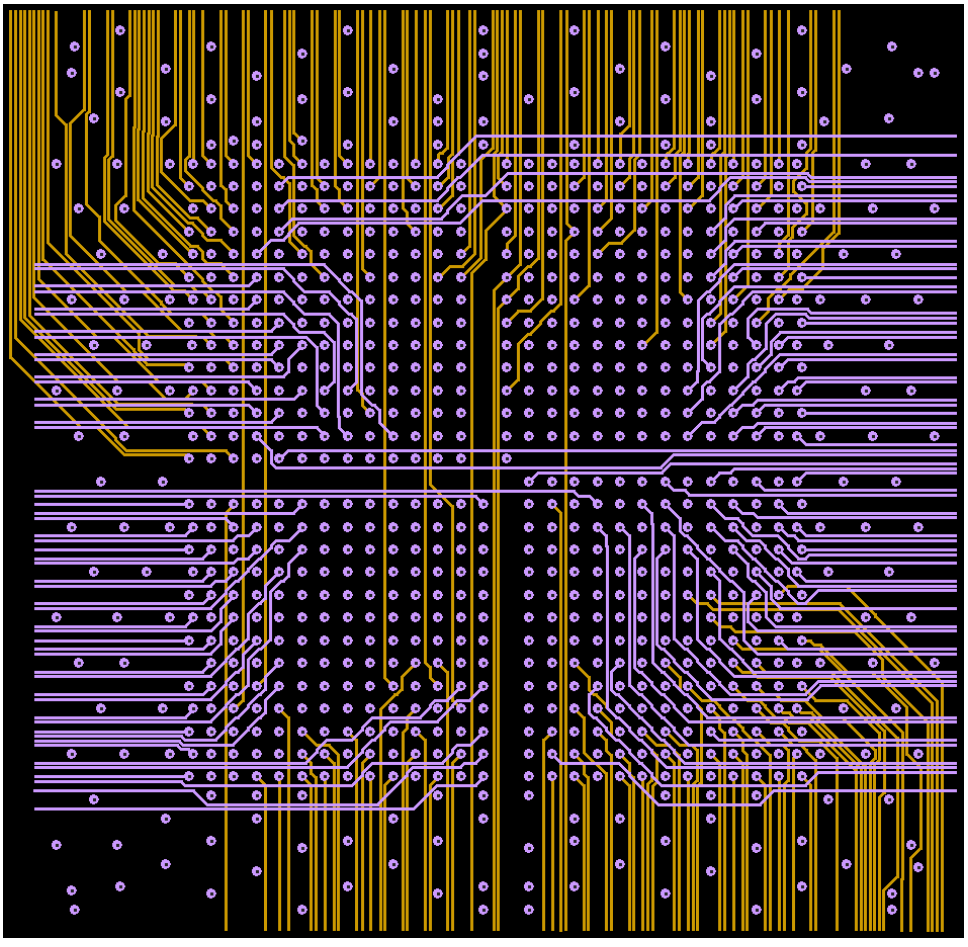


Figure 5-19: Signal layers 3 and 4

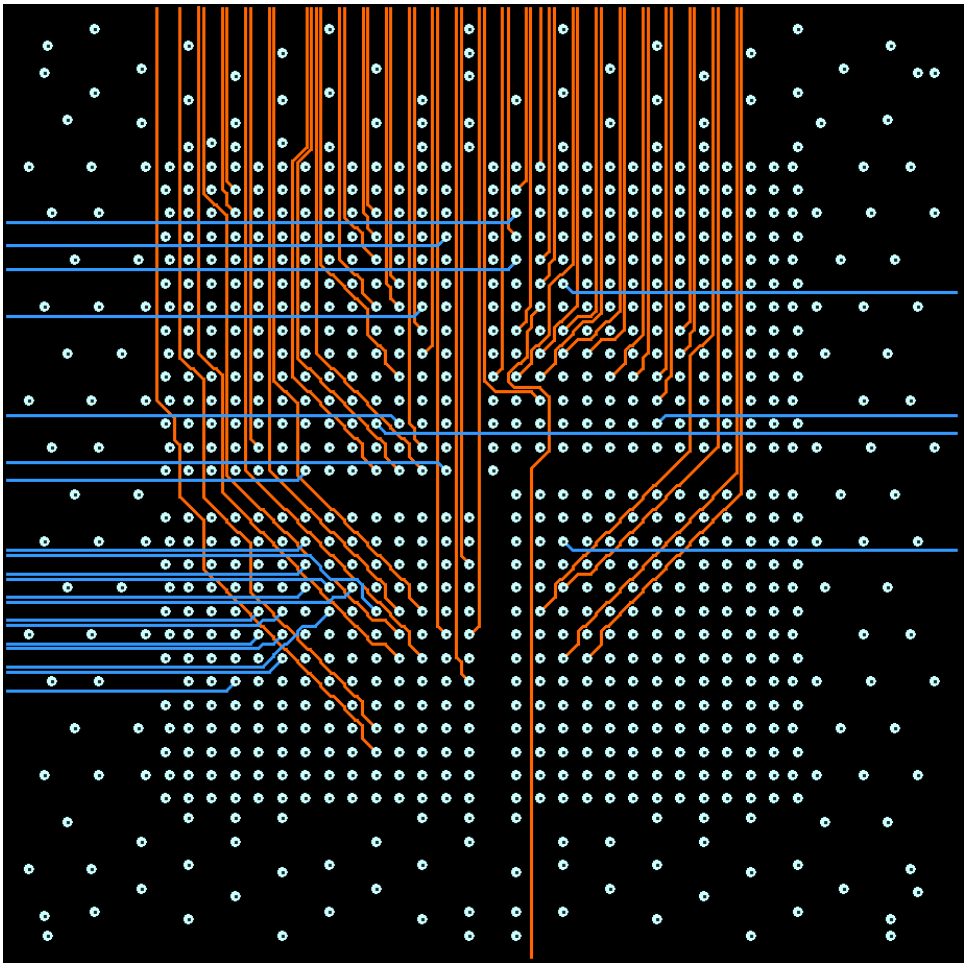


Figure 5-20: Signal layers 5 and 6

Route Results

Attempt #	Layers	Breakouts	*Rule Areas	**Via Obstructs	Tried	Opens	% Routed	Time Min.
1	14-15	None	None	None	678	145	79%	12
2	14-15	Layer Biased, fixed	None	None	678	209	69%	4
3	14-15	Layer Biased, unfixed	None	None	678	91	87%	15
4	2-15	None	None	Yes	1140	277	76%	48
5	2-15	NSEW, unfixed	None	Yes	1140	170	85%	44
6	2-15	NSEW, unfixed	None	No	1140	125	89%	24
7	2-15	Layer Biased, unfixed	None	Yes	1140	74	94%	27
8	2-15	Layer Biased, unfixed	None	Yes	1140	55	95%	28
9	2-15	Layer Biased, unfixed	None	No	1140	39	97%	16
10	2-15	Layer Biased, unfixed	Yes	No	1140	36	97%	24

Table 5-1: Layer biased route results

* Rule Areas: In the final test, a rule area was added around the outside of all the BGAs so the width/spacing inside was 4th/4th and outside 4th/7th for single ended nets.

** Via Obstructs: Originally a via obstruct around the BGA was added to prevent additional vias from being added inside, potentially modifying the alignment of the existing via fanout pattern. However, the route results were better when the via obstruct was removed and the fanouts didn't really get "messed up".

Analysis of Layer Biased Route Results

Attempts 1-3

The first three attempts only addressed routing of the fanouts using with the micro-vias. They compare routing of the nets connected to this BGA when there are no breakouts and when there are layer biased breakouts, either fixed or unfixed.

- The highest completion is provided by "Layer Biased, unfixed".

- With the escape traces unfixed, the router was free to push and shove them to make room for routing.
- With the layer biased breakouts, the router was able to complete 8% or 54 more connections. This is significant, especially if similar results would be obtained for all 19 of the large BGAs on this board.

Attempts 4-10
These attempts compare the results of routing layers 2-15 using micro-vias and buried-vias. In these cases, a total of 1140 connections were tried by the autorouter. The key attempts are:

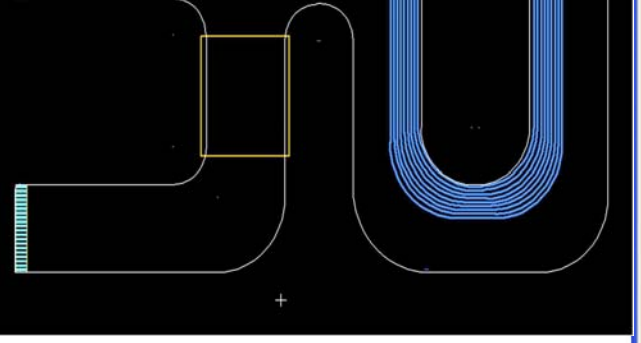
- 4 (no breakouts) 76% completion
- 6 (NSEW breakouts) 89% completion
- 10 (Layer Biased breakouts) 97%.

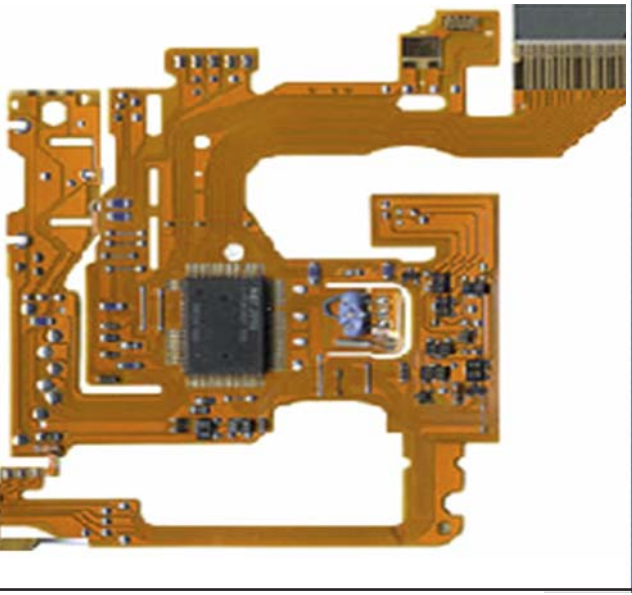
Using the layer biased breakouts improved the routing 21% over not using breakouts and 8% over NSEW breakouts.

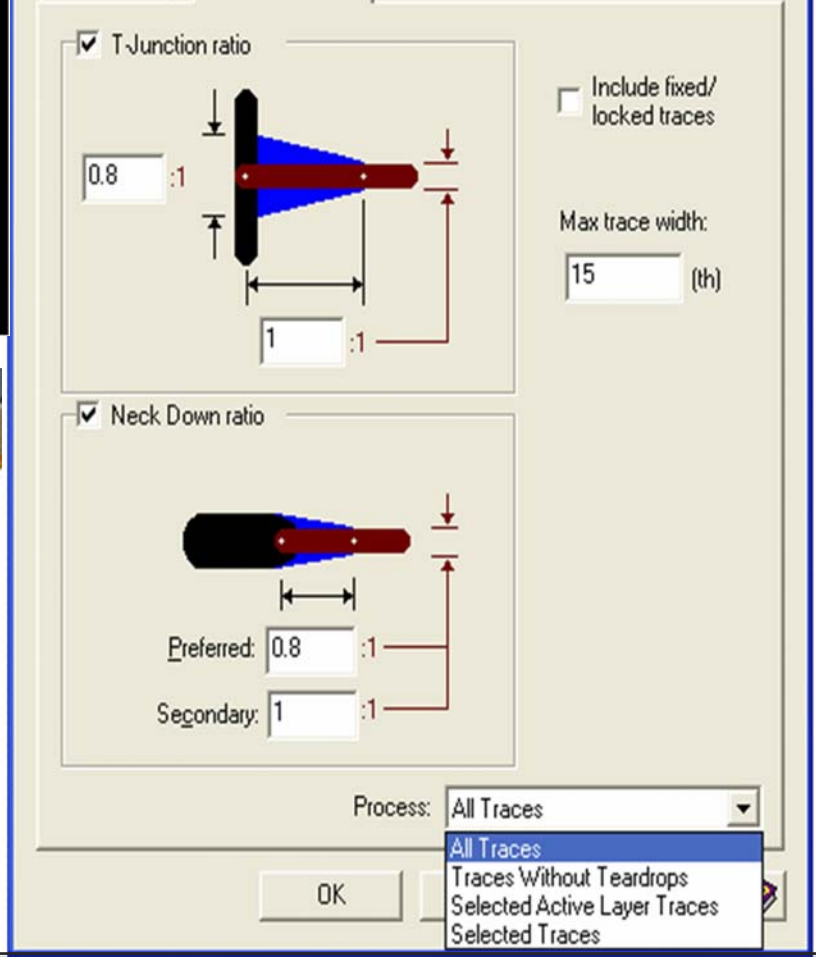
- Using a Rule Area to increase the spacing between traces outside the BGA actually helped to increase the routing completion by three connections. This is not a significant number, but it is interesting.
- With the increased spacing, the router took some different paths for the routing and as chance would have it, the overall routing was better.
- With spacing increased, there is more room for vias in critical areas.
- It is also interesting that using layer biased breakouts took half the time (24 minutes compared to 48) of not using breakouts at all.
- This is an indication that without the breakouts, the router struggled and spent more time doing rip-up and retry – which inherently takes more time than if it can find a path just using push and shove.

Summary

It is clear that on large board with multiple large BGAs, layer biased breakouts can make a significant difference in auto route completion percentage and time to route.







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Chapter Six - 0.8mm Pin-Pitch BGA Tests

Although I am unaware of any BGA with a pin-pitch of 0.8mm and over 1500 pins, the day will come when it will be the norm as opposed to the large 1mm devices. The FPGA companies who are approaching 2000 pins with 1mm pin-pitch are correctly concerned about the transition to 0.8mm. Exceeding 2000 pins with 1mm pin-pitch results in a very large BGA which is not only more expensive to manufacture, it is also more difficult to attach to the board due to potential warping of either the device or the board. The FPGA customers want increased functionality (resulting in more pins), yet they have no experience routing such a device.

Using the principles described previously for 1mm BGAs, this section will explore fanout and breakout solutions for routing the large 0.8mm devices. The solutions include use of multiple via-fanout patterns and even the application of Any-Layer Via technology.

I encourage you to look at all the test results. Numerous different via patterns were applied along with some interesting techniques for increasing route density.

Test Scenario

I took a footprint for a Virtex-5 with 1760 pins at 1mm pitch and converted it to 0.8mm pitch. In the next two figures, observe that reducing the pin pitch only 20% requires a significantly smaller set of features and a first impression that screams, “How am I going to route that?”

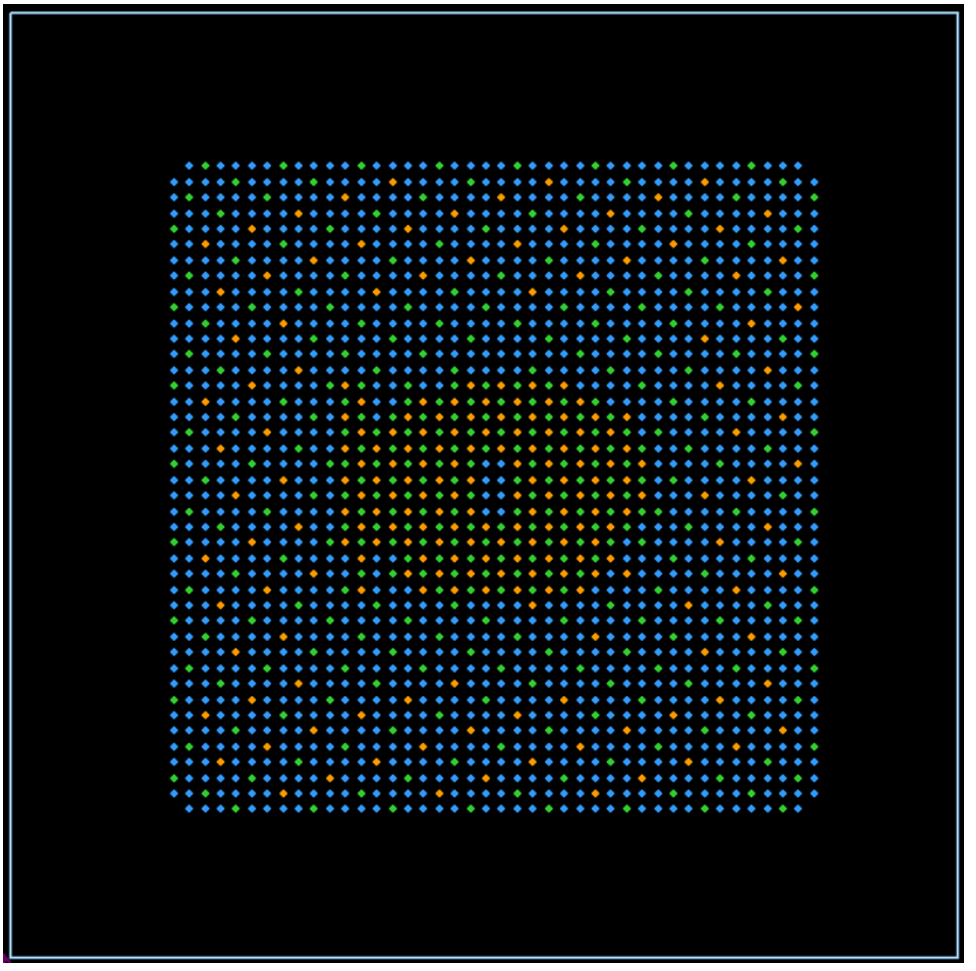


Figure 6-1: 1760 pins with 0.08mm pitch

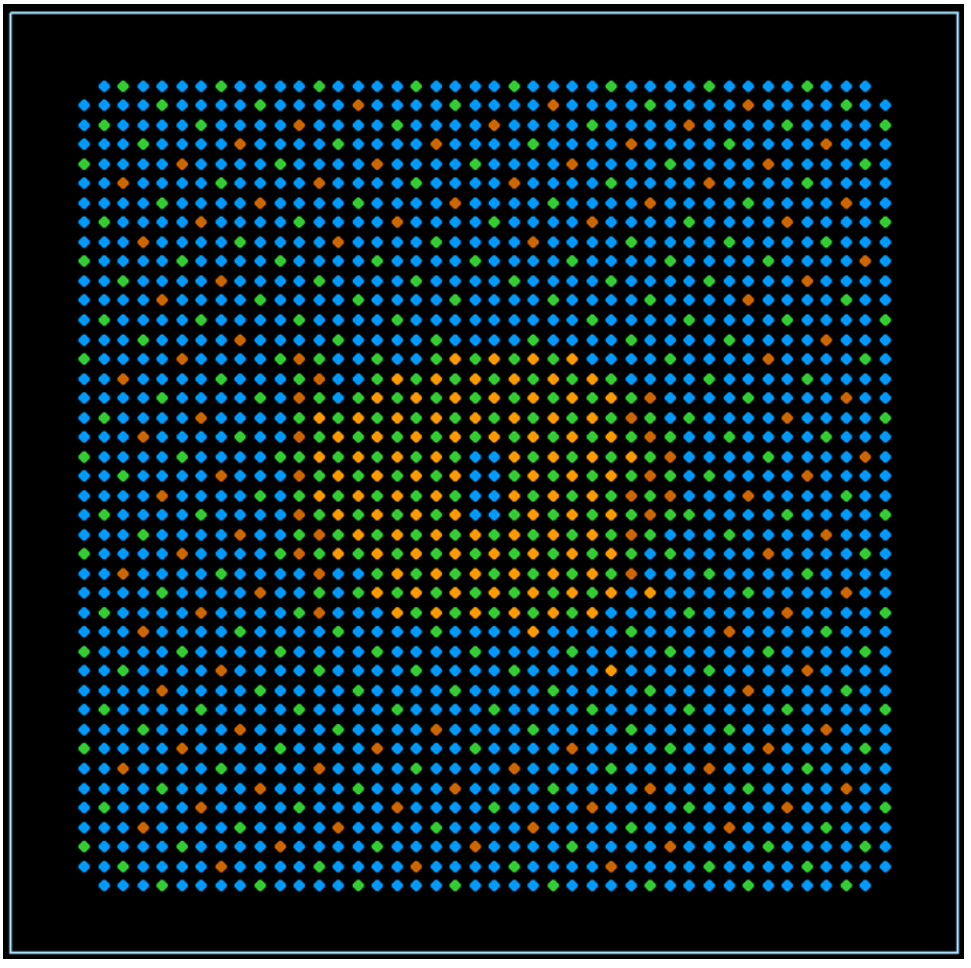


Figure 6-2: Virtex-5, 1760 pins with 1mm pitch

I performed fanout patterns and NSEW breakout patterns for three different via configurations:

- Test 1: Through-vias
  Total Signal Layers for Breakout: 7
- Test 2: Through-vias, 1:2 micro-vias, 1:3 micro-vias
  Total Signal Layers for Breakout: 5
- Test 3: Any-layer-vias
  Total Signal Layers for Breakout: 3

Test 1: Through-Vias

The first test used only through-vias to demonstrate the number of layers required for such a method so it could be compared to the other more efficient solutions.

Design Rules

The design rules for the first test are the same as used in the 1mm pitch tests from the previous chapters, except the ball pads are a little smaller due to the smaller pin-pitch.

		mm	mils
0.8 mm Pitch	Through-Via Pad	0.50	20
	Ball Pad	0.40	16
	Trace Width	0.10	4
	Diff Pair Clearance	0.10	4
	Trace-Trace Space	0.10	4
	Via-Trace Space	0.10	4
	Via-Pad Space	0.10	4

Table 6-1: Design rules (Test 1)

Fanout Patterns

Except for the outer row of ball pads, this test used a standard Quad Dog-Bone Matrix for the fanout vias.

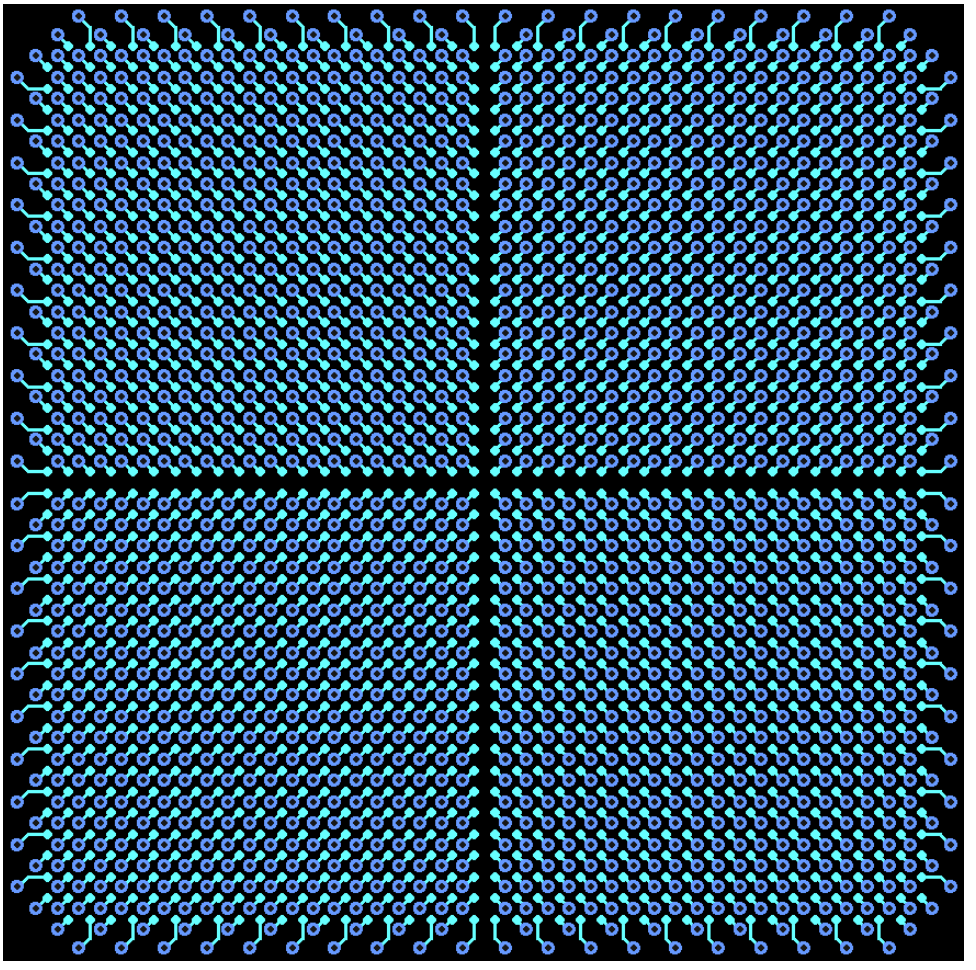


Figure 6-3: Fanout pattern (Test 1)

In Figure 6-4, you can see why the vias are staggered on the outer row. The pink traces are on the second layer and by staggering the outer row vias, you can get two traces between the vias as opposed only one. This makes a big difference for routing the escape traces belonging to the outer rows of ball pads.

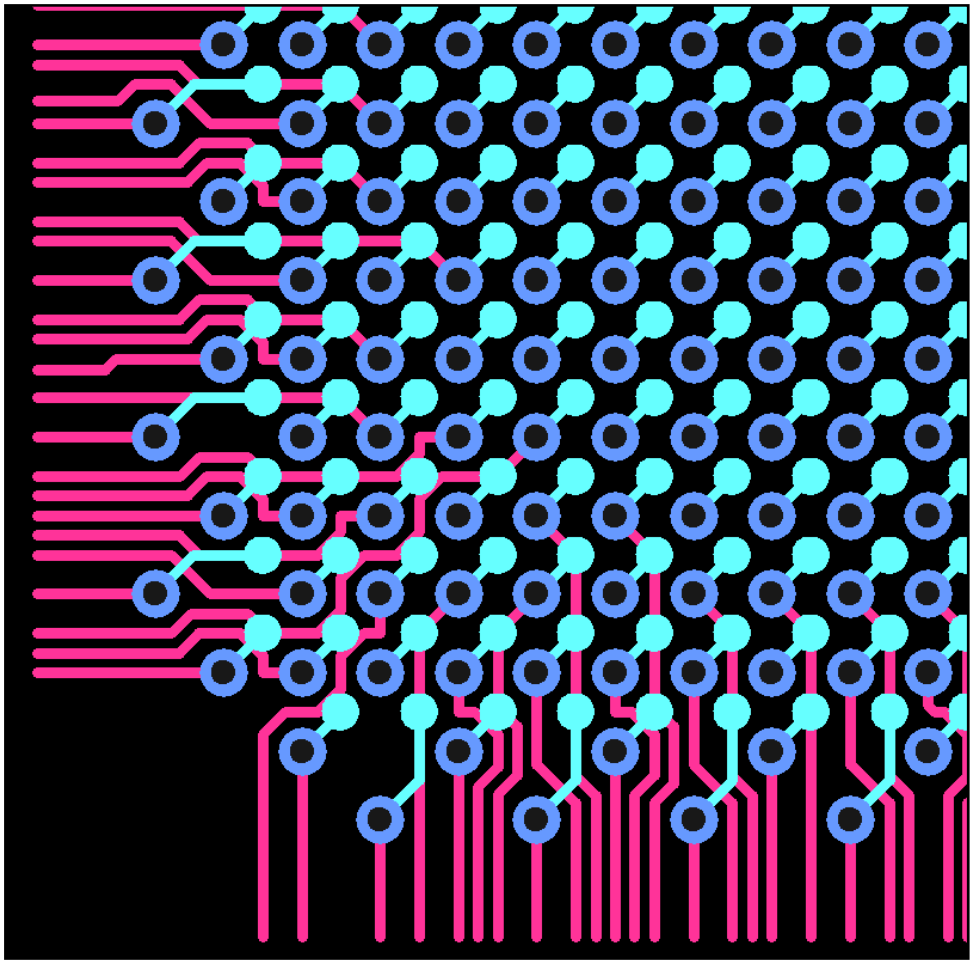


Figure 6-4: Fanout pattern detail (Test 1)

Test 1 Breakout Results

When using the through-via only, it took seven routing layers to accomplish the NSEW breakout. In the context of a board, layer biased breakouts will most likely produce better routing, however, NSEW is used here to demonstrate comparisons between the different via configurations.

Test 1 Breakout Images

Figures 6-5 through 6-11 show the escape traces for each of the signal layers. GND vias are colored green and VCC (all voltages) vias are colored orange.

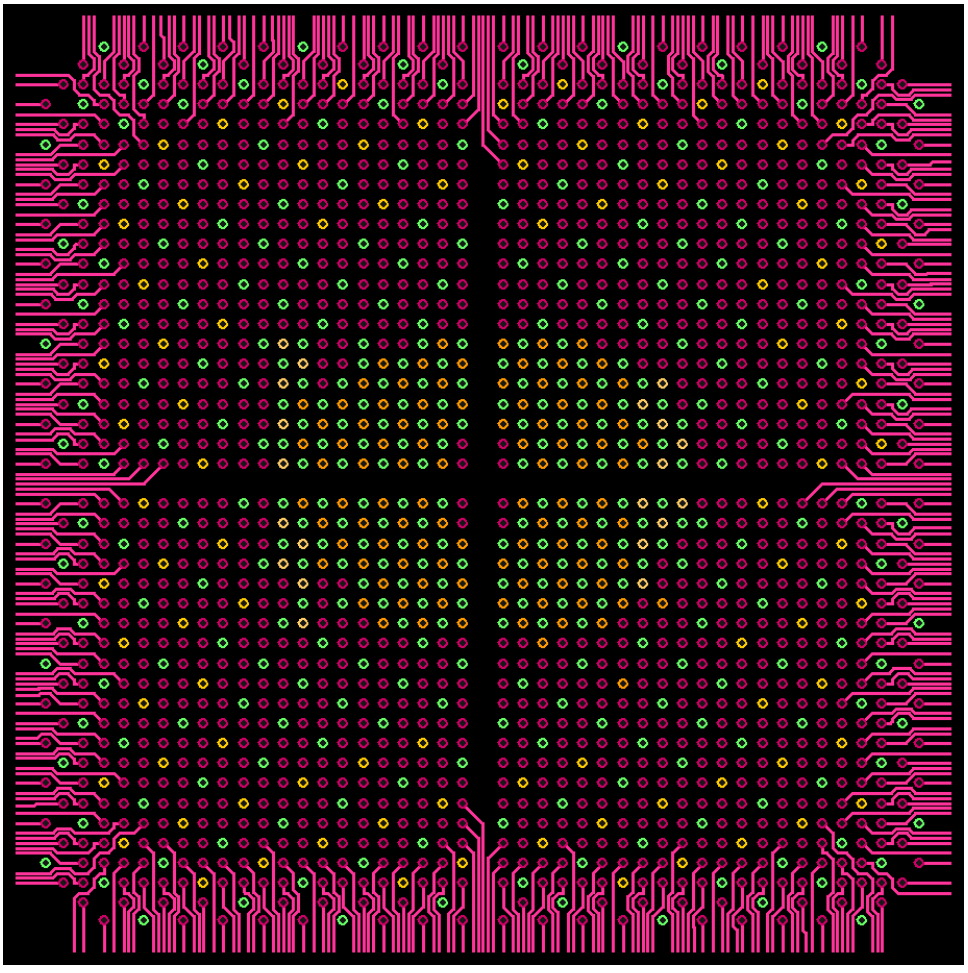


Figure 6-5: First signal layer (Test 1)

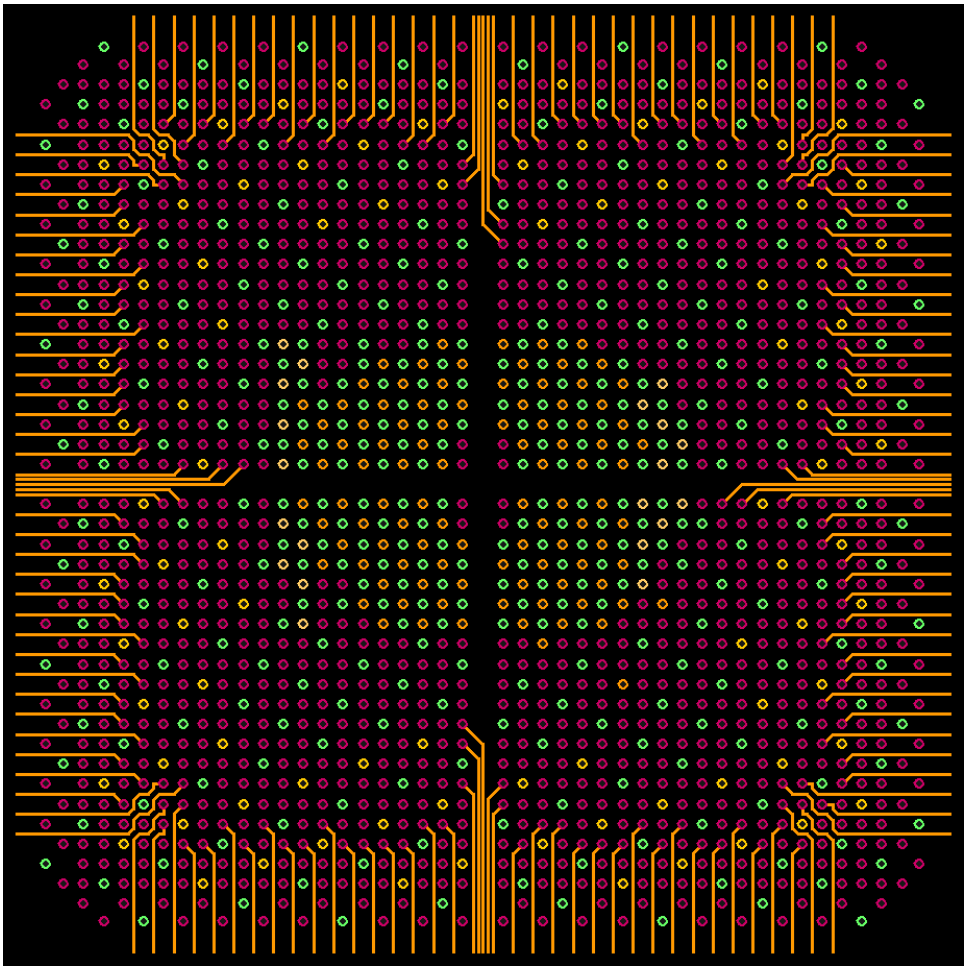


Figure 6-6: Second signal layer (Test 1)

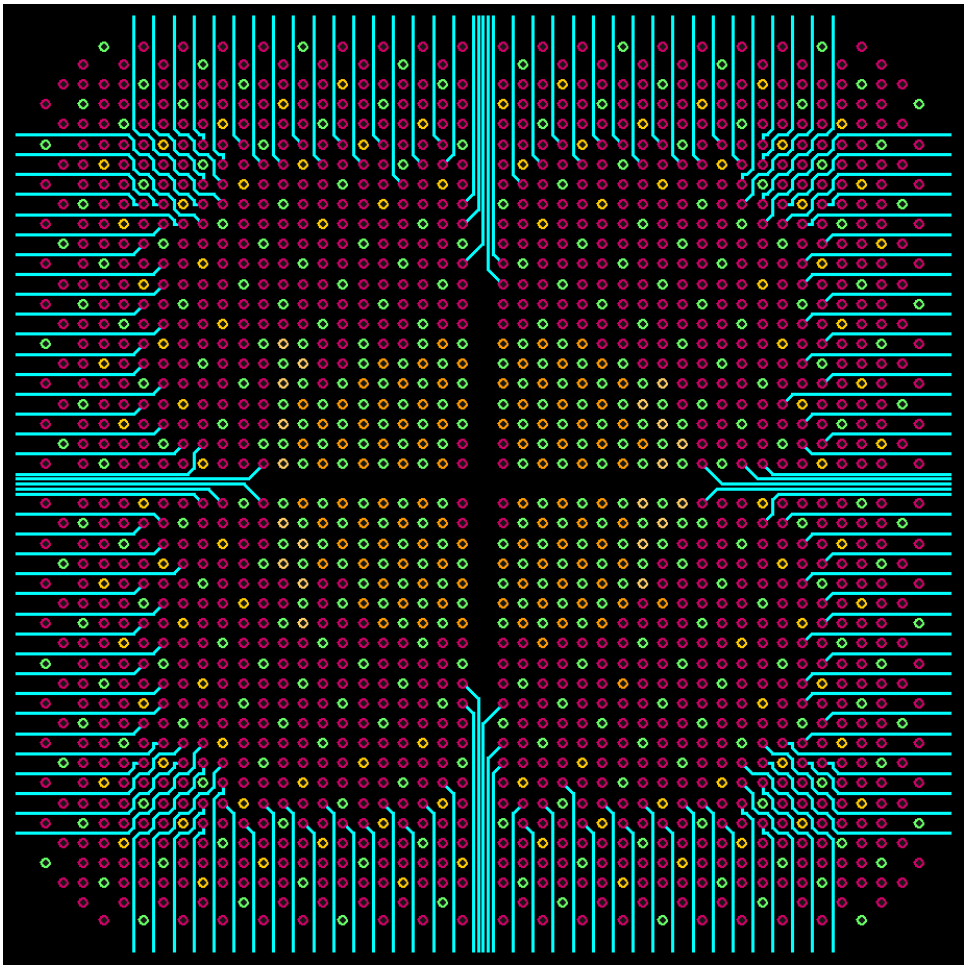


Figure 6-7: Third signal layer (Test 1)

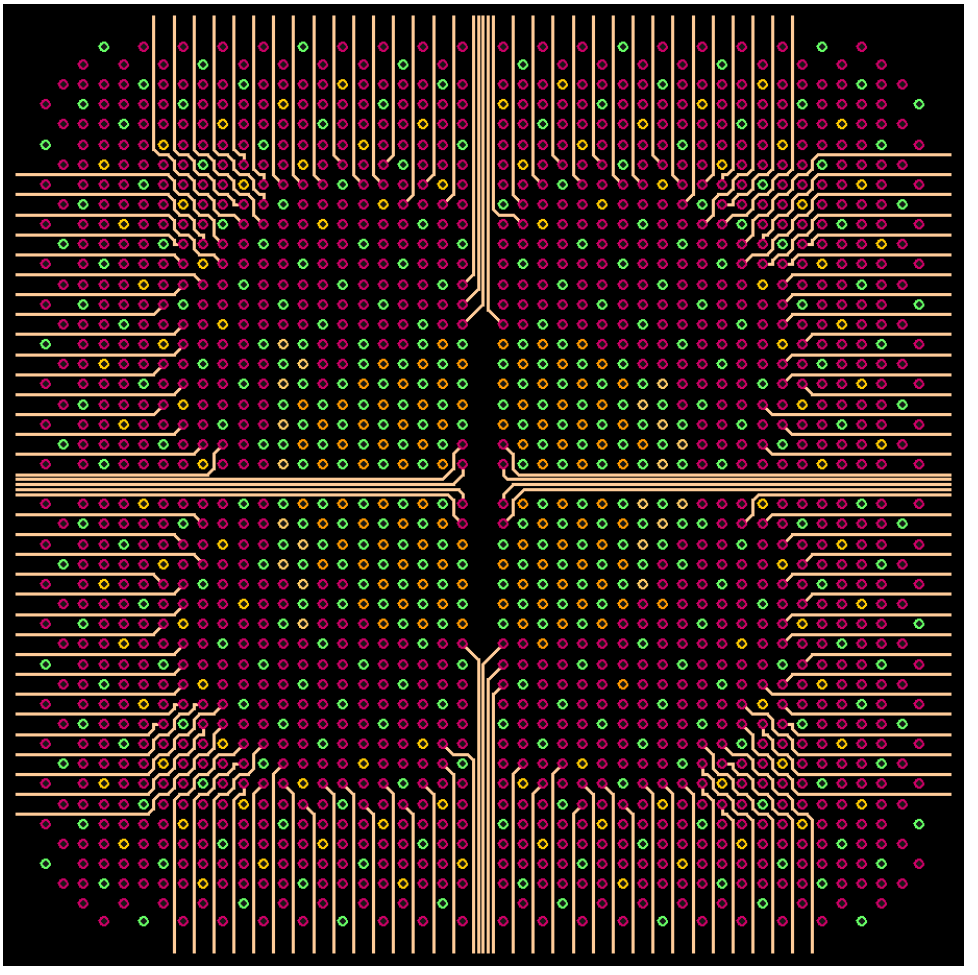


Figure 6-8: Fourth signal layer (Test 1)

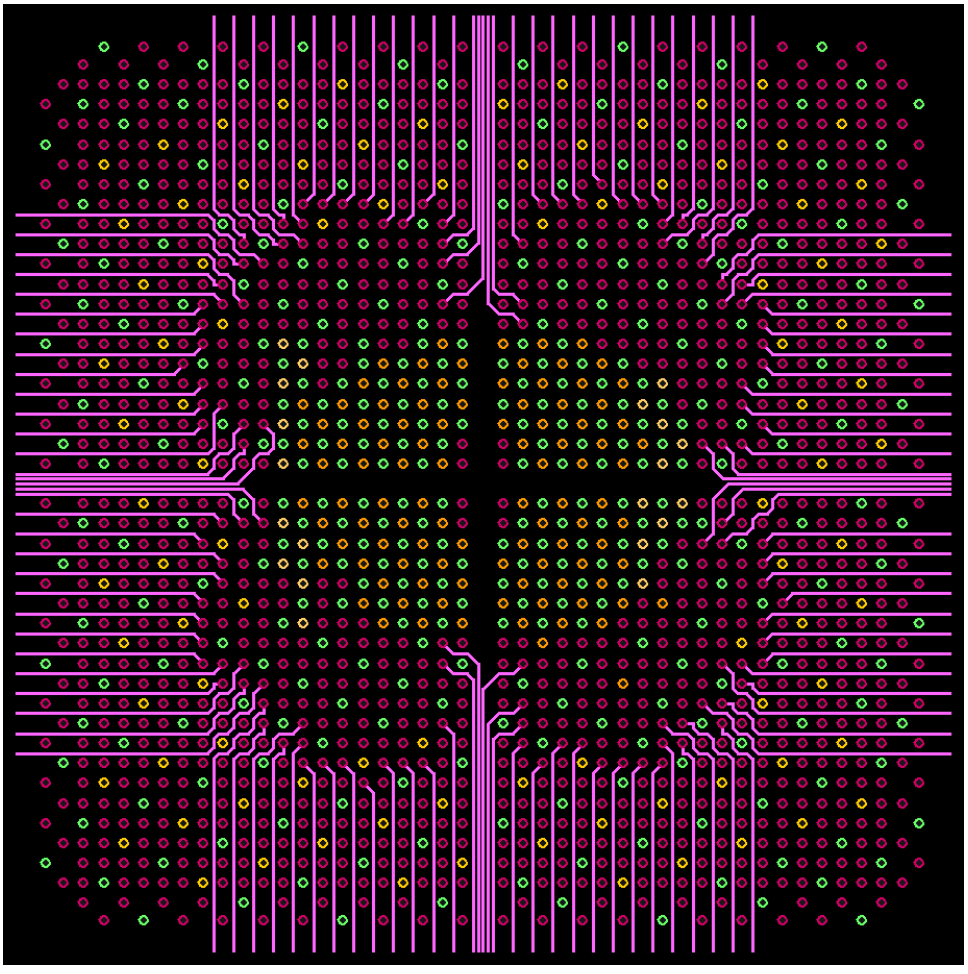


Figure 6-9: Fifth signal layer (Test 1)

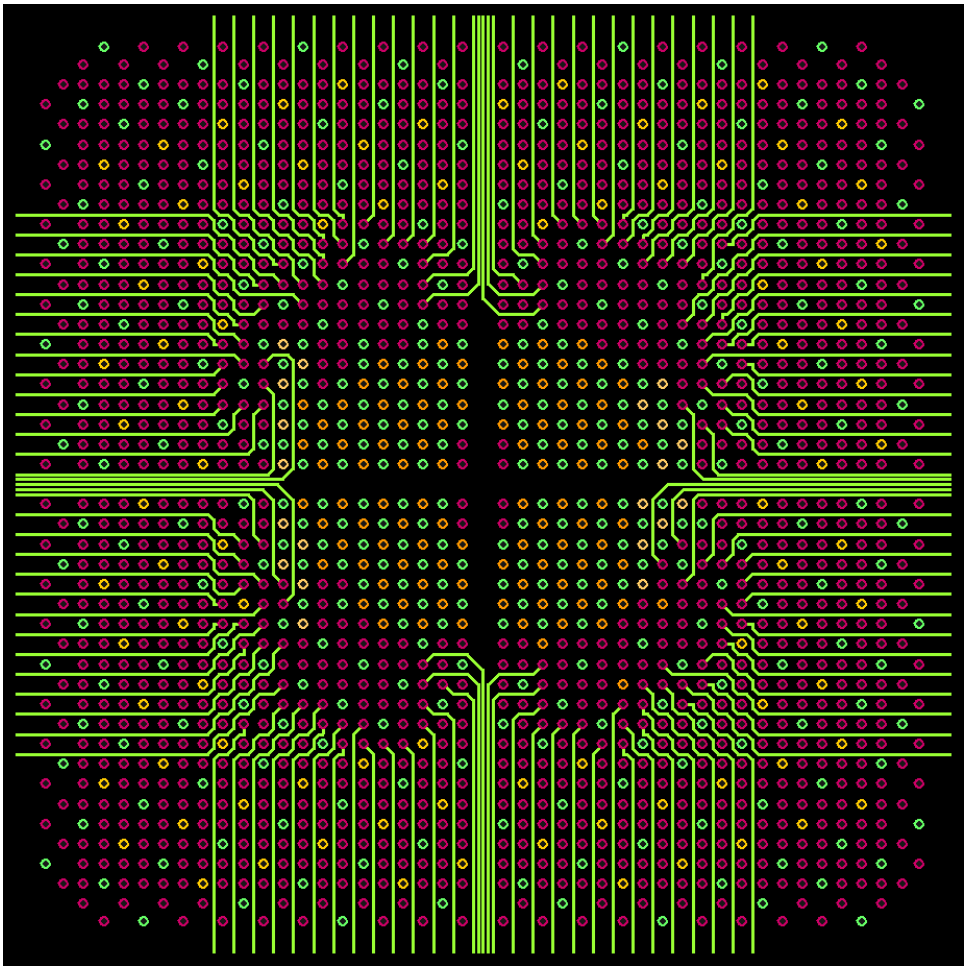


Figure 6-10: Sixth signal layer (Test 1)

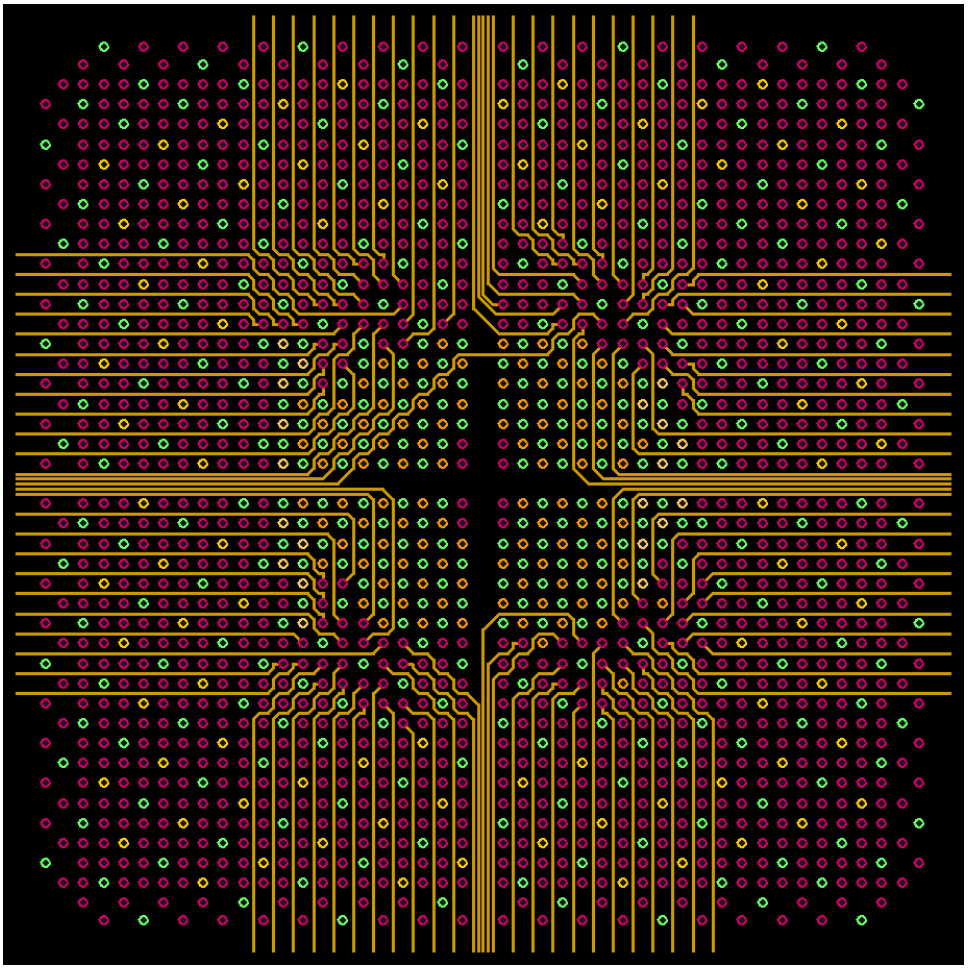


Figure 6-11: Seventh signal layer (Test 1)

Test 1 Summary

- When using through-vias on 0.8mm pitch devices, the layer count goes up very quickly because the maximum number of traces between the vias is just one.
- For this 1760 pin device, it took a minimum of 7 signal layers and there is the potential of signal degradation since the differential pairs need to be split.

Test 2: Micro-Vias and Through-Vias

The second test used a combination of micro-vias and through-vias.

Design Rules

With the finer pin-pitch smaller ball pads are required. However the rest of the design rules were the same as those applied to the 1mm pitch parts. The second test used smaller rules.

		mm	mils
0.8 mm Pitch	1-2 Micro-Via Pad	0.25	10
	1-3 Skip-Via Pad	0.30	12
	Through-Via Pad	0.50	20
	Ball Pad	0.40	16
	Trace Width	0.10	4
	Diff Pair Clearance	0.10	4
	Trace-Trace Space	0.10	4
	Via-Trace Space	0.10	4
	Via-Pad Space	0.10	4

Table 6-2: Design rules (Test 2)

Test 2 Stackup

An HDI stackup was used with 1:2 micro-vias, 1:3 skip-vias and a through-via. The through-via was used for fanout of the power and ground pins so they could attach to all the planes and the discrete components on the opposite side of the board. I chose the through-via over a buried-via because it turns out that the through-via is the same size as the buried-via would have to be and the through-via is more direct and simple. The through-via in this case did not affect the route density significantly so from a cost and simplicity point of view, it was more appropriate.

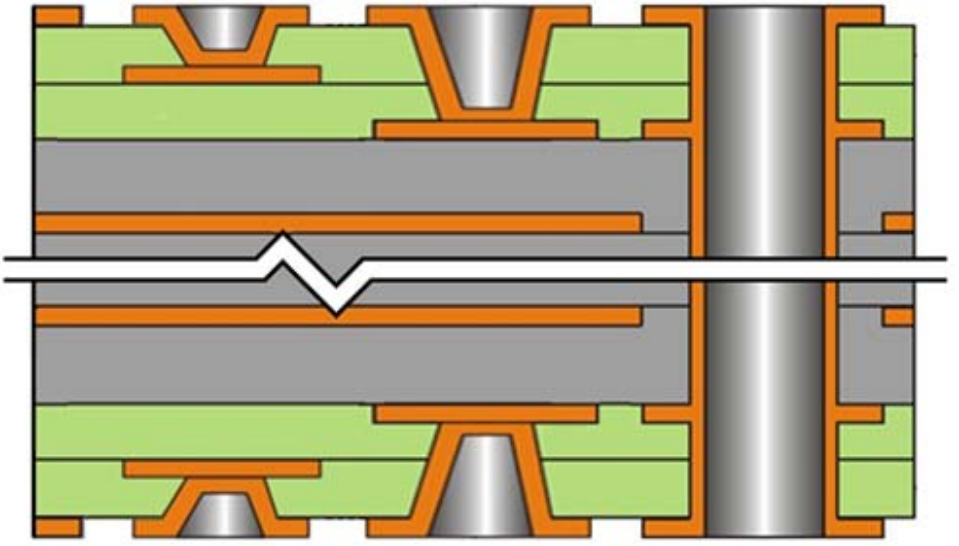


Figure 6-12: Stackup (Test 2)

Fanout Patterns

Figure 6-13 initially appears to present a very different set of fanout patterns. However, a closer look shows that the principles of aligning vias and combining different patterns to maximize the route density are applied.

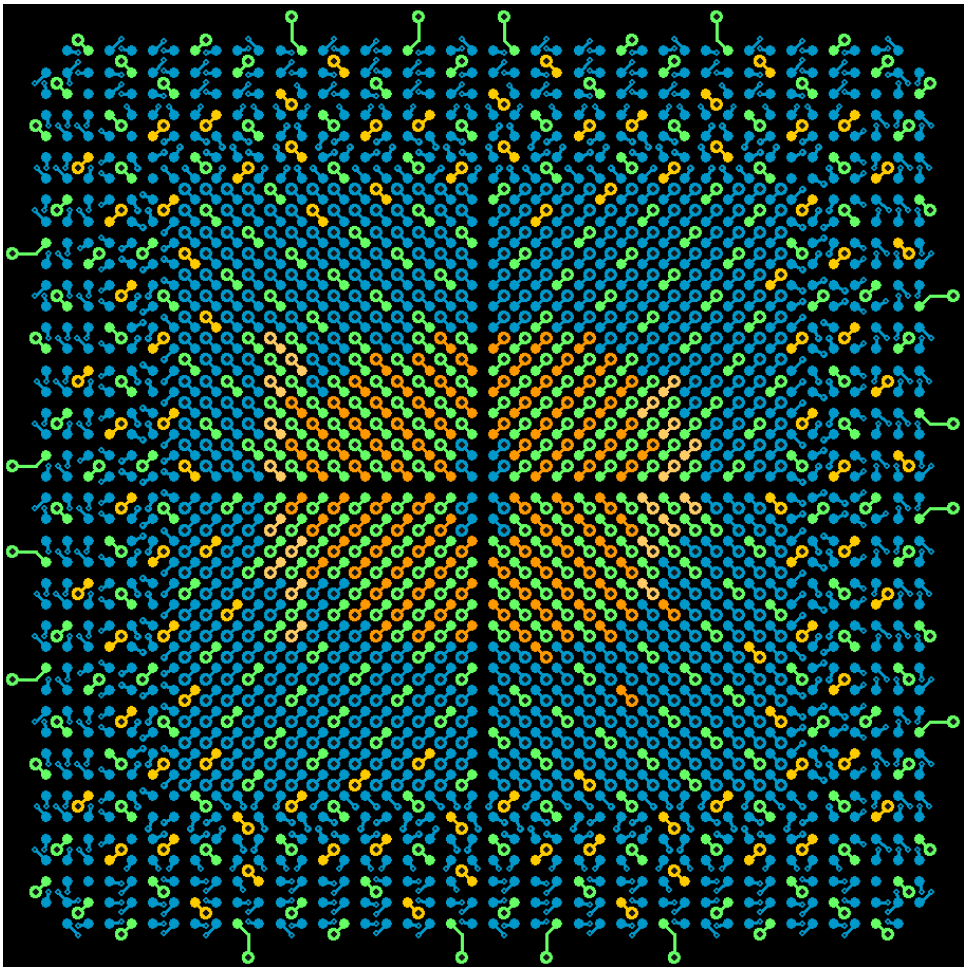


Figure 6-13: Fanout patterns (Test 2)

Power and Ground

The power (orange) and ground (green) vias are all through-vias, large enough to not be of concern for current-carrying capacity. In the center of the device, the standard Quadrant Matrix pattern is used, then for the outer seven rows and columns of ball pads, the via is placed aligned with the shifted micro-vias for the I/Os which are colored blue.

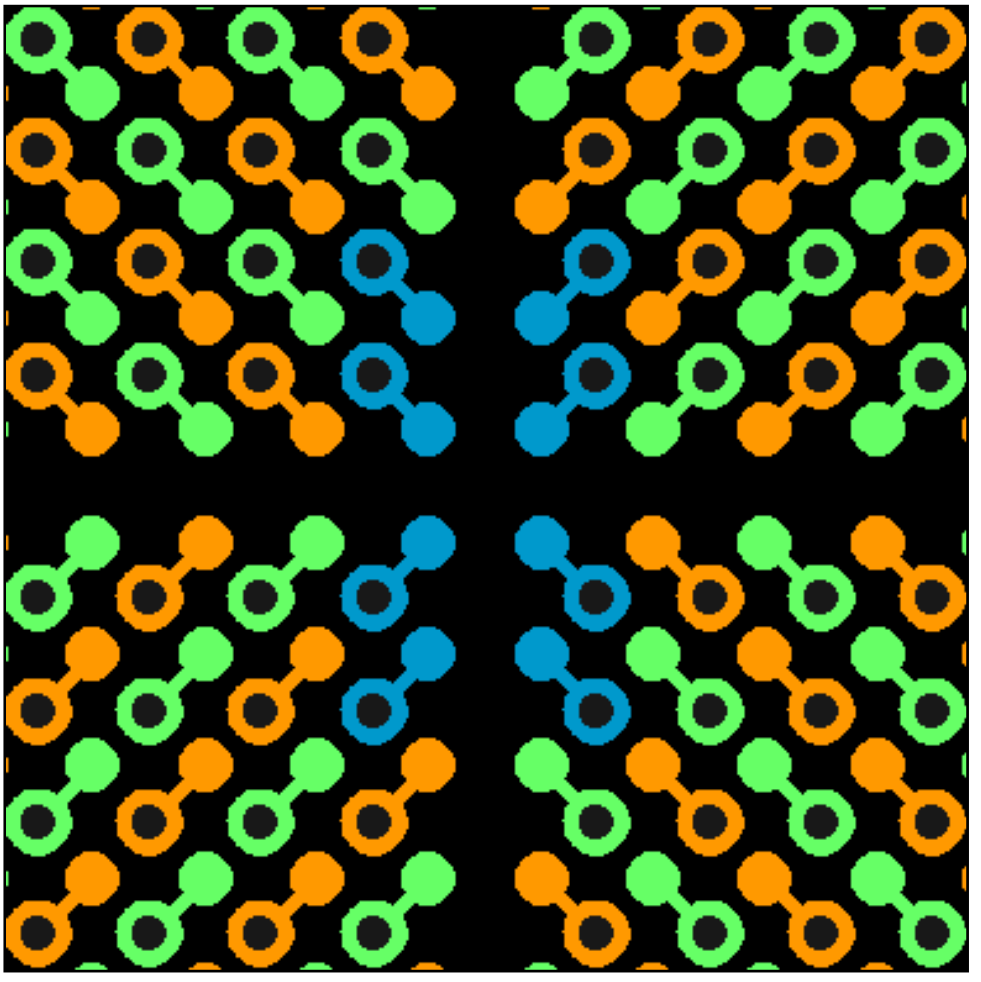


Figure 6-14: Power and ground quadrant matrix fanouts in center (Test 2)

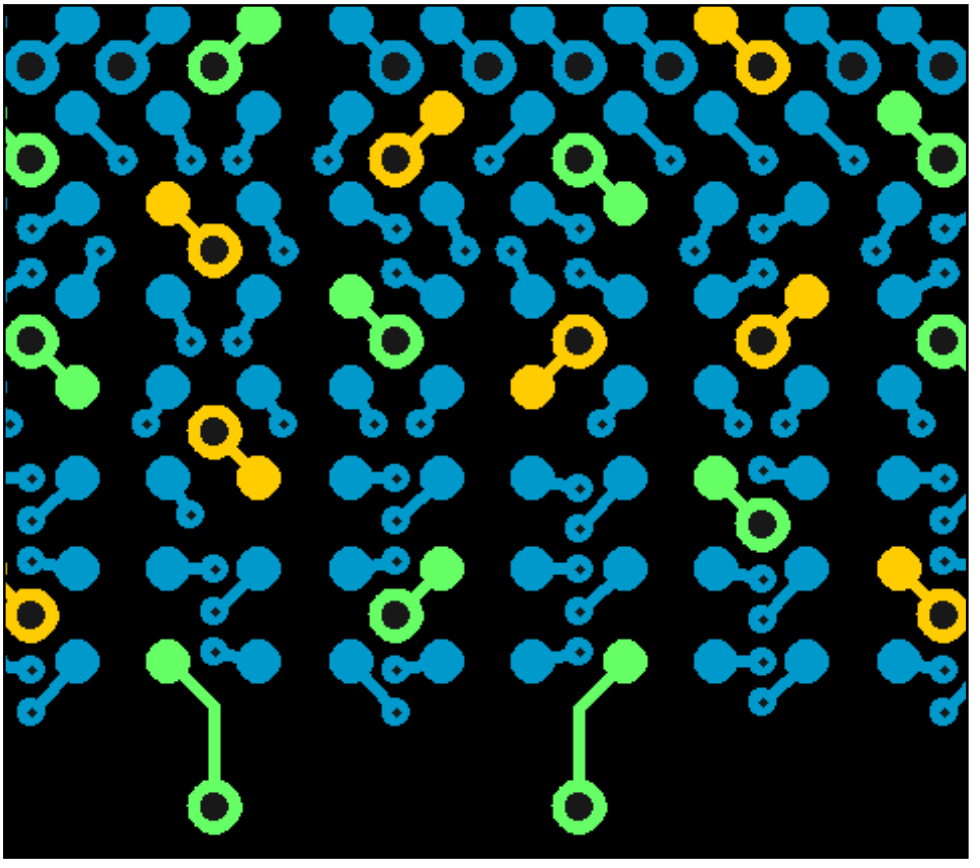


Figure 6-15: Power and ground fanouts around perimeter layer 1 (Test 2)

Notice in the above figure, power and ground through-vias are aligned vertically in every-other channel of ball pads. This section of the BGA is in the lower center of the device as shown in Figure 6-13. As you will note in figures later in this chapter, the power and ground vias generally do not block routing channels, except with the outer row around the perimeter. The ground fanouts have been added some distance away from the ball pads so that an extra trace could be added as you can see in Figure 6-16.

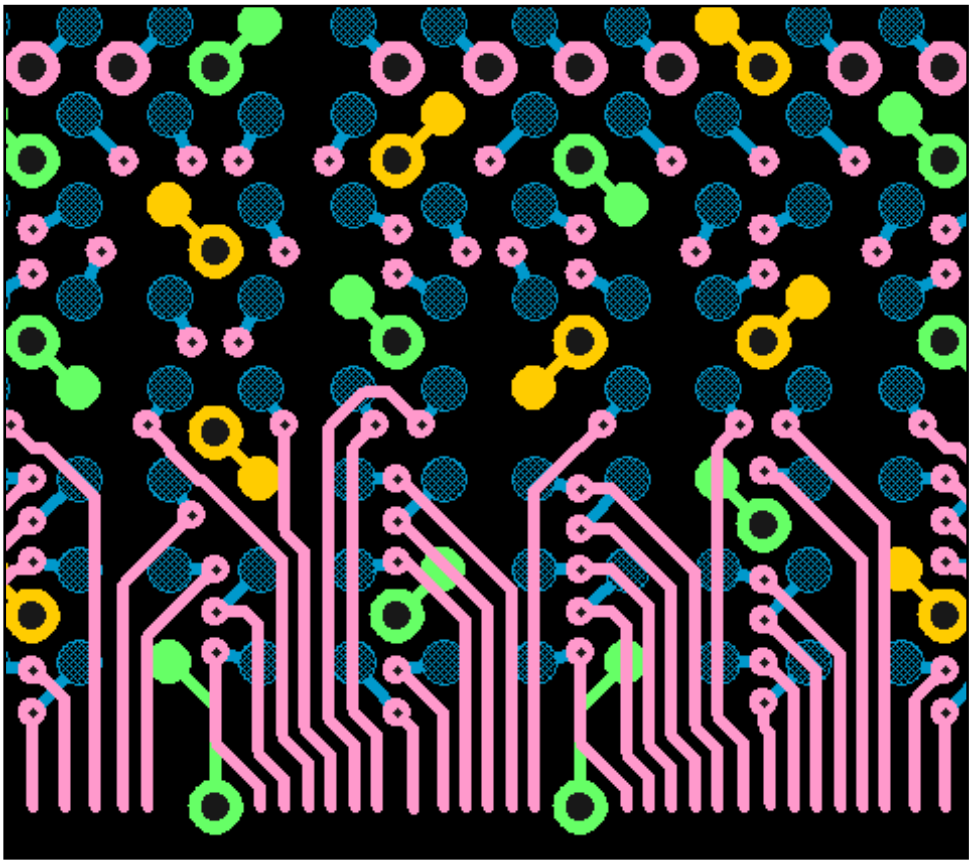


Figure 6-16: Power and ground fanouts around perimeter layer 2 (Test 2)

By moving the ground via down and away from the ball pads, an extra route channel is opened between the through-vias and the micro-vias on layer 2.

I/O Pins

As you can see in Figure 6-13, the center of the BGA has I/O pins with through-vias in a Quadrant Matrix. You might ask, "If through vias can be used in the center, why not for the whole BGA?"

- By using micro-vias on the perimeter, the effective size of the BGA (to be routed using through-vias) has been reduced from 1760 pins to 784.

- Since the center of the BGA is primarily power and ground pins, the actual number of I/Os that need to be routed (after the micro-vias are used around the perimeter) with through-vias is reduced to 544. This is a reasonable number of pins to be routed out of the through-via array without forcing the addition of layers that would otherwise not be needed for general routing of the board.
- When through-vias are used, there is room for only one trace between the through-via array and as such, the number of layers would be significantly increased if through-vias were used for all pins.
- Also, differential pairs will need to be split since only one trace can fit through the through-via array. This requirement can be effectively minimized by using micro-vias around the perimeter.

Layer 1:2 Micro-Vias

The 1:2 micro-vias are aligned in nice columns and rows between pairs of ball pads. Because of the 0.8mm spacing between the ball pads and because of the rather large space that the through-via takes, the micro-vias are not evenly spaced as they would be if the pin-pitch was 1mm.

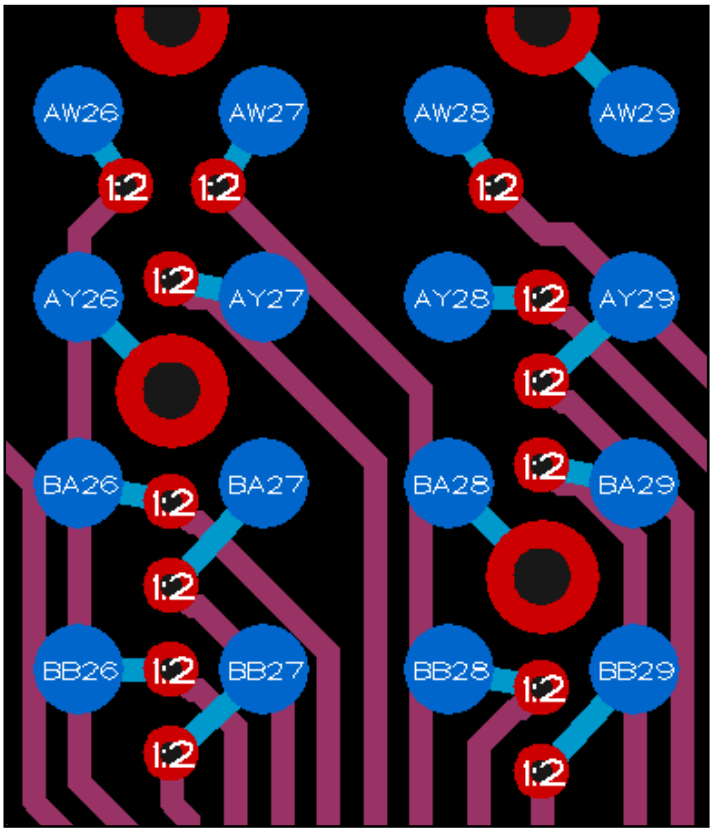


Figure 6-17: Layer 1:2 micro-vias (Test 2)

In the above figure, the colors have been changed to emphasize the 1:2 micro-vias.

At the top, you can see the micro-vias connected to pins AW26 through AW28 are not aligned in a column. This is because the through-vias for the power and ground take up enough space that there isn't room for the micro-vias to be aligned. It turns out that it really doesn't affect the route density. Since there are no additional traces on layer 2 (purple traces) that have to come through that area, placing the vias horizontally doesn't block any other traces.

This is a general principle when placing the fanout vias. In this case we are using 1:2 micro-vias for the four rows of ball pads around the perimeter. The innermost row of ball pads can have their vias placed in almost any manner because they will not block routing on any other layer. These vias don't exist after layer 2, so obviously they won't block routing on layer 3.

If you are routing differential pairs through the columns of vias, you could spread them out a little when feasible.

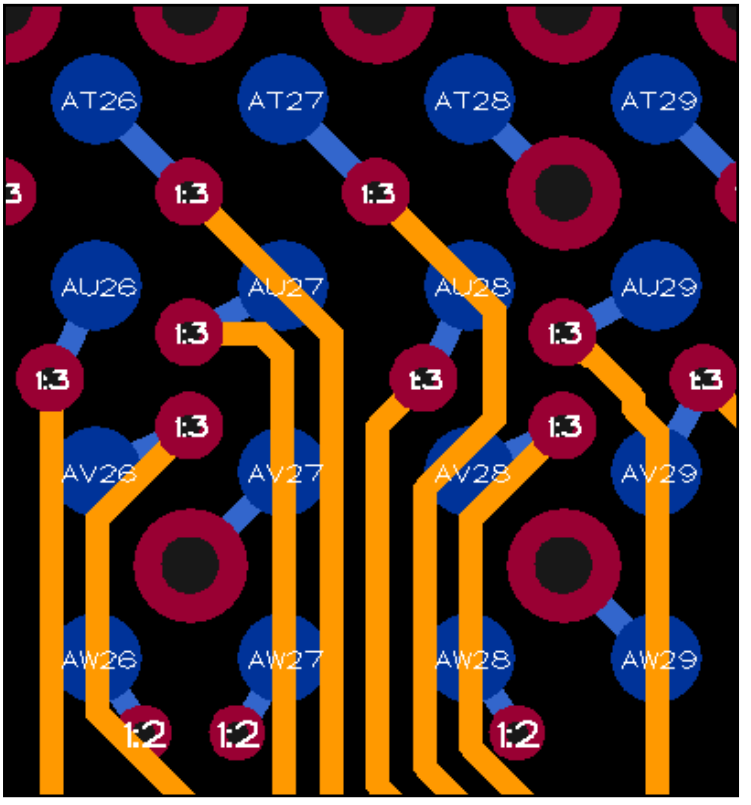


Figure 6-18: Layer 1:3 micro-vias (Test 2)

The layer 1:2 micro-vias are used for the first four rows of pins and the layer 1:3 micro-vias are used for the next three rows of pins. Due to the

through-vias used for the eighth row of pins, the 1:3 micro-vias had to be packed into a smaller area. This means the 1:3 micro-vias are not aligned in columns, however, there is a pattern to the madness. You can see the pattern in Figure 6-16.

- On layer 3, there is considerable room for the routing. In fact, I suspect that if I had spent more time packing in the traces, there might even be room for one more row of pins to be routed on layer 3 using the 1:3 micro-vias.

Test 2 Breakout Images

Figures 6-19 through 6-23 show the breakouts on all layers using the NSEW method. The total number of signal layers required to breakout this device was five.

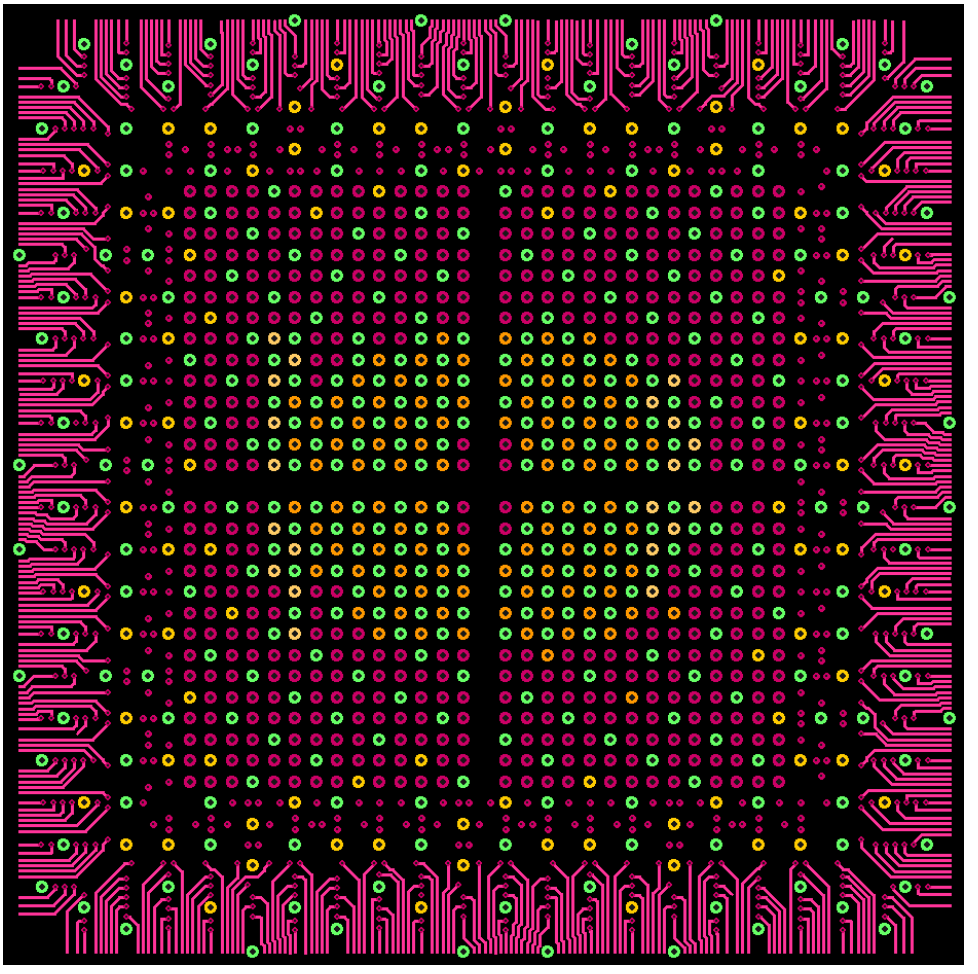


Figure 6-19: First signal layer (Test 2)

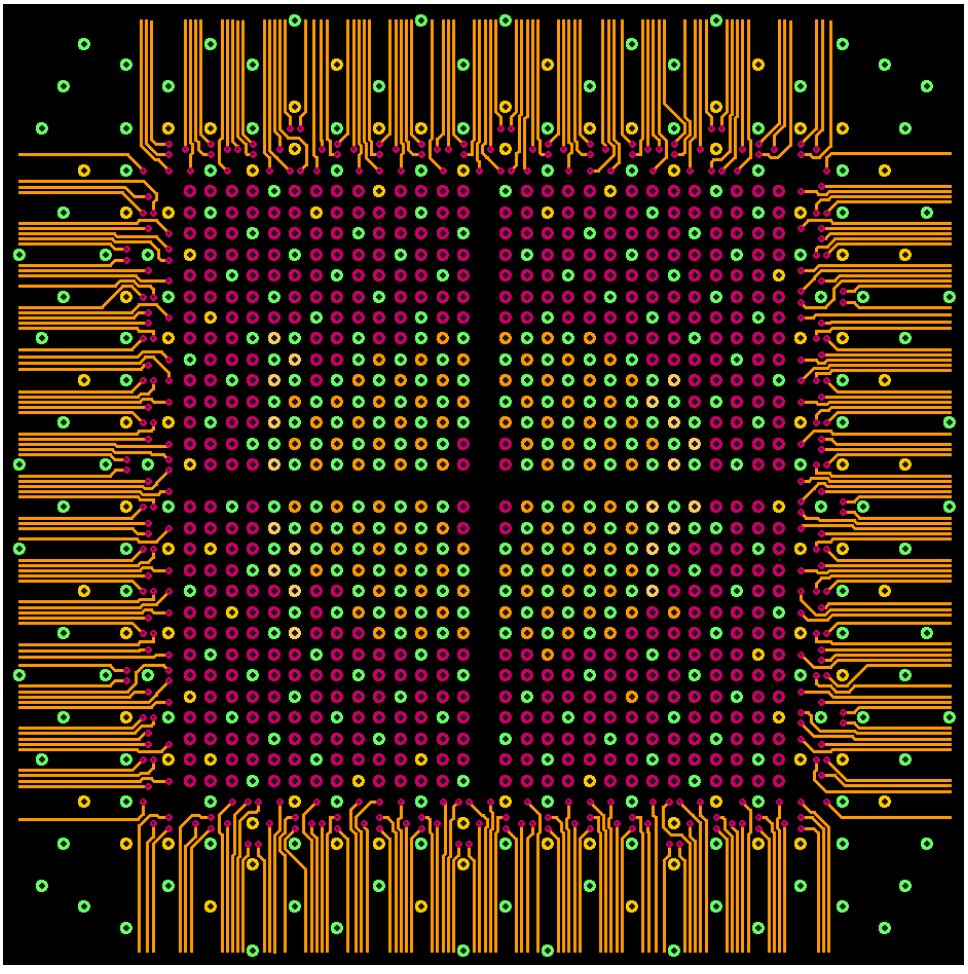


Figure 6-20: Second signal layer (Test 2)

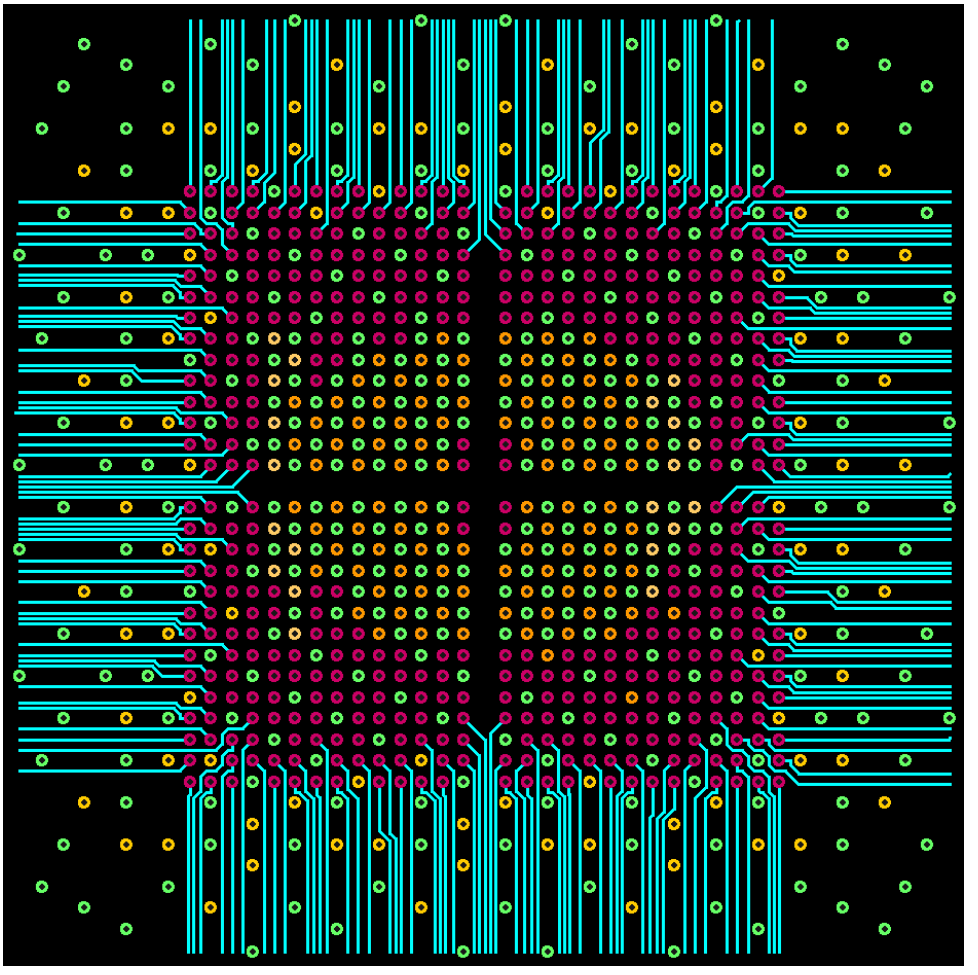


Figure 6-21: Third signal layer (Test 2)

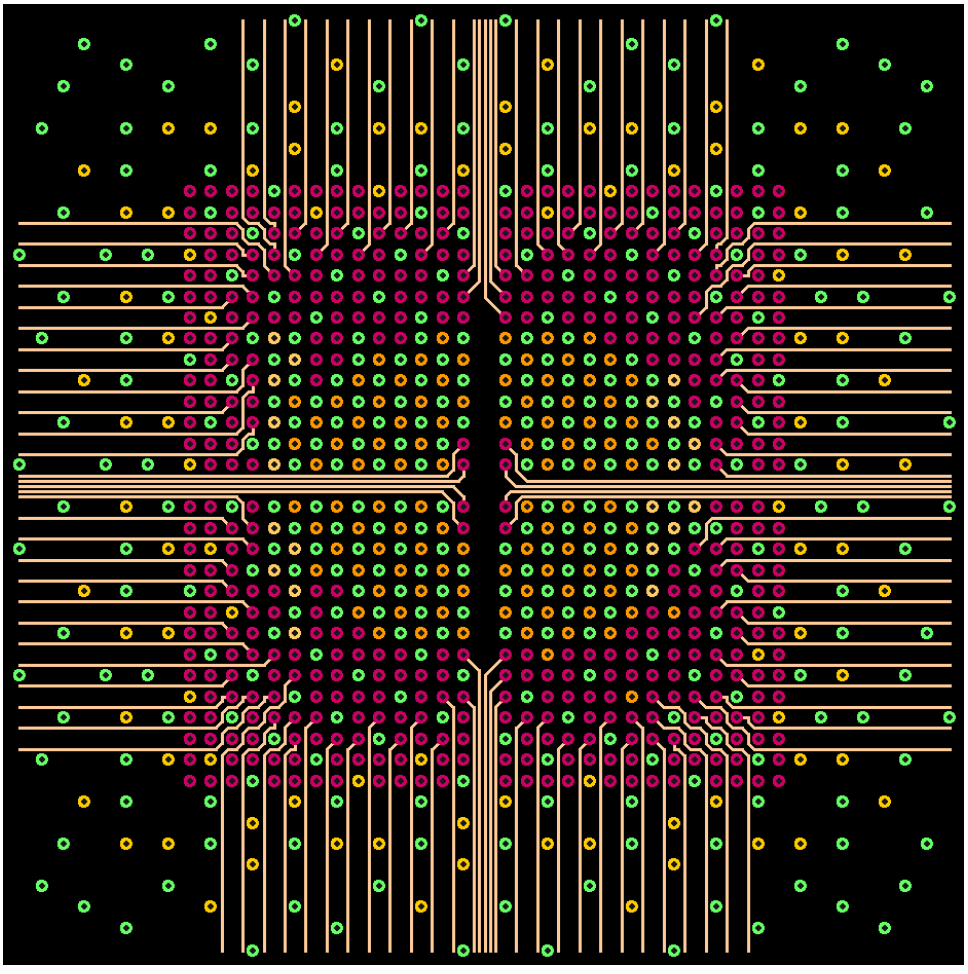


Figure 6-22: Fourth signal layer (Test 2)

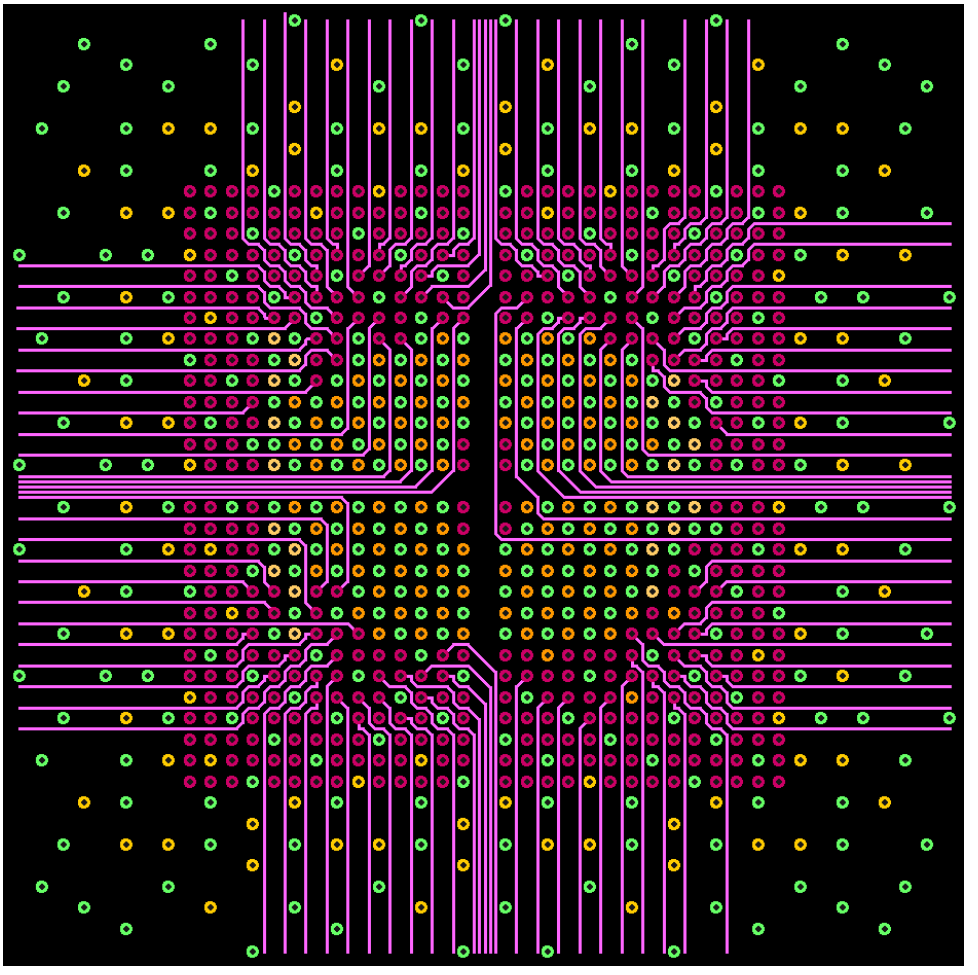


Figure 6-23: Fifth signal layer (Test 2)

Test 2 Summary

- Applying NSEW breakouts with good fanout patterns enables breakouts on large BGAs in five-to-six signal layers.
- With increased spacing for differential pairs, it probably could be done with eight-to-ten signal layers.
- This method can maintain normal trace widths and clearances
- If the BGA has over 2000 pins, may have to compromise trace widths and clearances.

Test 3: Any-Layer-Vias

The third test uses an any-layer-via stackup in which each layer is buildup and has a via-hole in it. Via spans are created by continuous coincident locations up and down the stackup.

Design Rules

Smaller design rules are used in this test because it is expected that when any-layer-vias are widely adopted, the fabrication process will have gone through another miniaturization cycle.

		mm	mils
0.8 mm Pitch	ALIVH-Via Pad	0.20	8
	Ball Pad	0.40	16
	Trace Width	0.08	3
	Diff Pair Clearance	0.08	3
	Trace-Trace Space	0.08	3
	Via-Trace Space	0.08	3
	Via-Pad Space	0.08	3

Table 6-3: Design rules (Test 3)

Stackup

This stackup allows vias to span any set of consecutive layers. Chapter 3 has a description of the any-layer-via stackup.

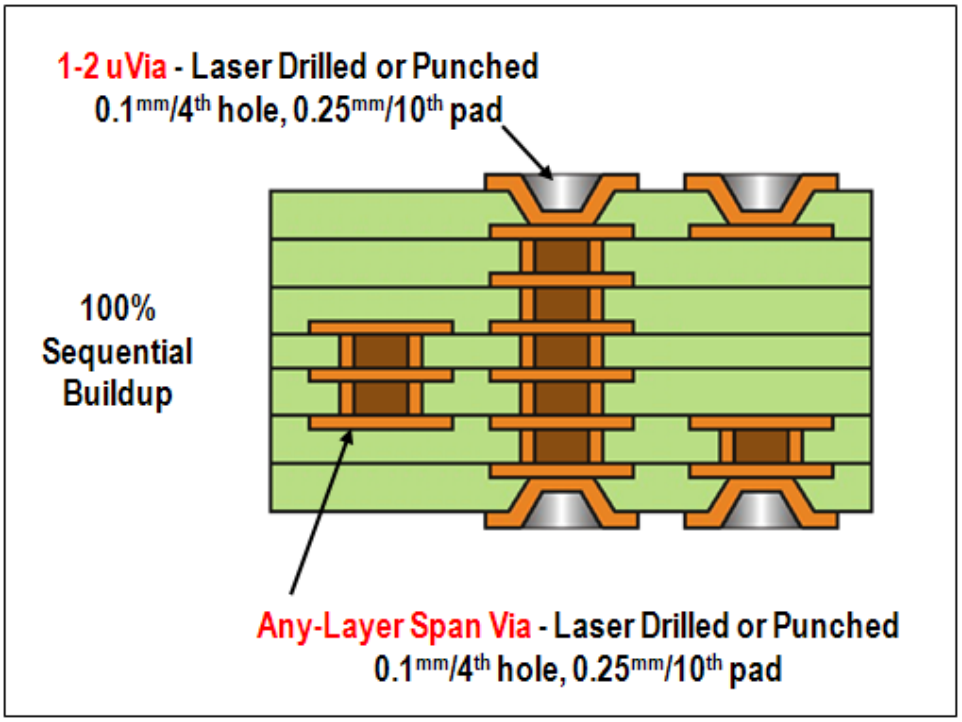


Figure 6-24: Any-layer-via stackup (Test 3)

Via Patterns

The any-layer-via provides a unique opportunity to try different patterns. The pad is small and only exists on the layer-pairs that are needed.

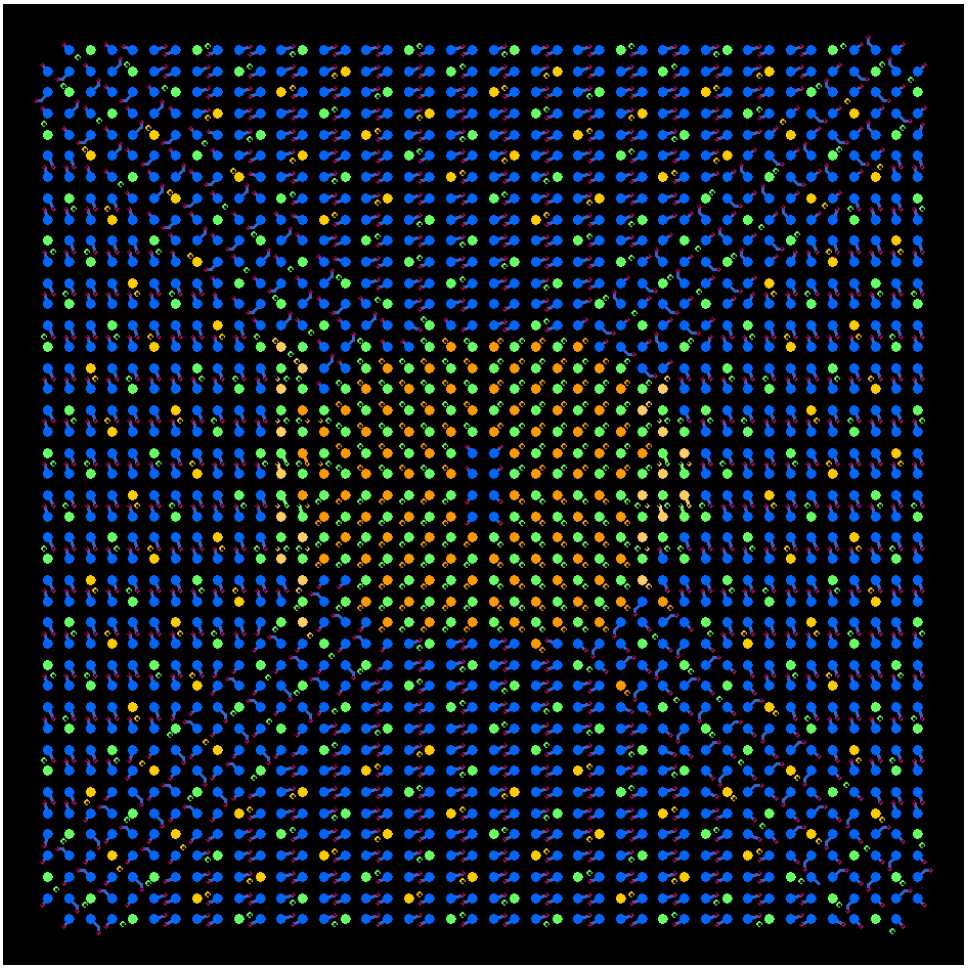


Figure 6-25: Top layer (Test 3)

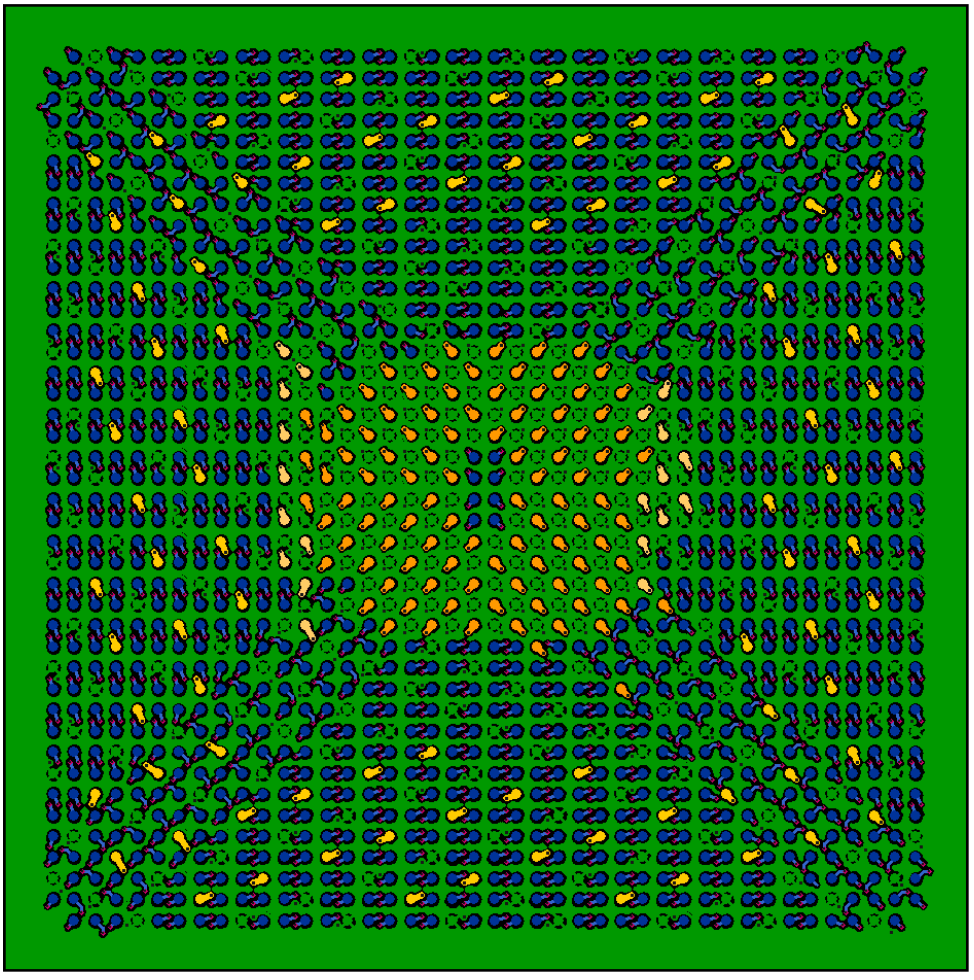


Figure 6-26: Top layer with ground plane (Test 3)

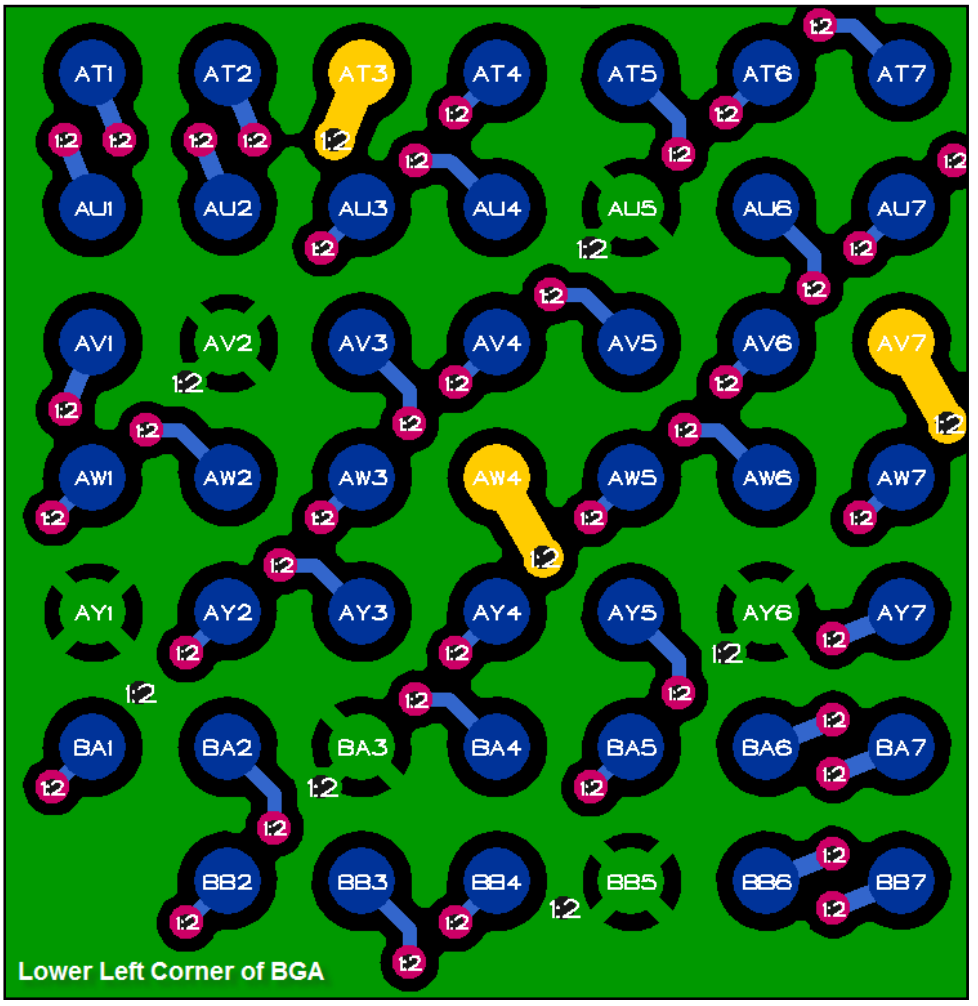


Figure 6-27: Top layer ground plane detail (Test 3)

Notes

- Each ball pad connected to ground uses a thermal relief and a via that goes to the bottom side of the board. These vias are embedded in the plane and are located nearby each ground ball pad.
- The hole for the ground and power vias are larger than the vias for the signals to ensure adequate current carrying capacity.

- The vias are aligned in a diagonal at the corners. This provides additional routing space as you can see in Figure 6-29.

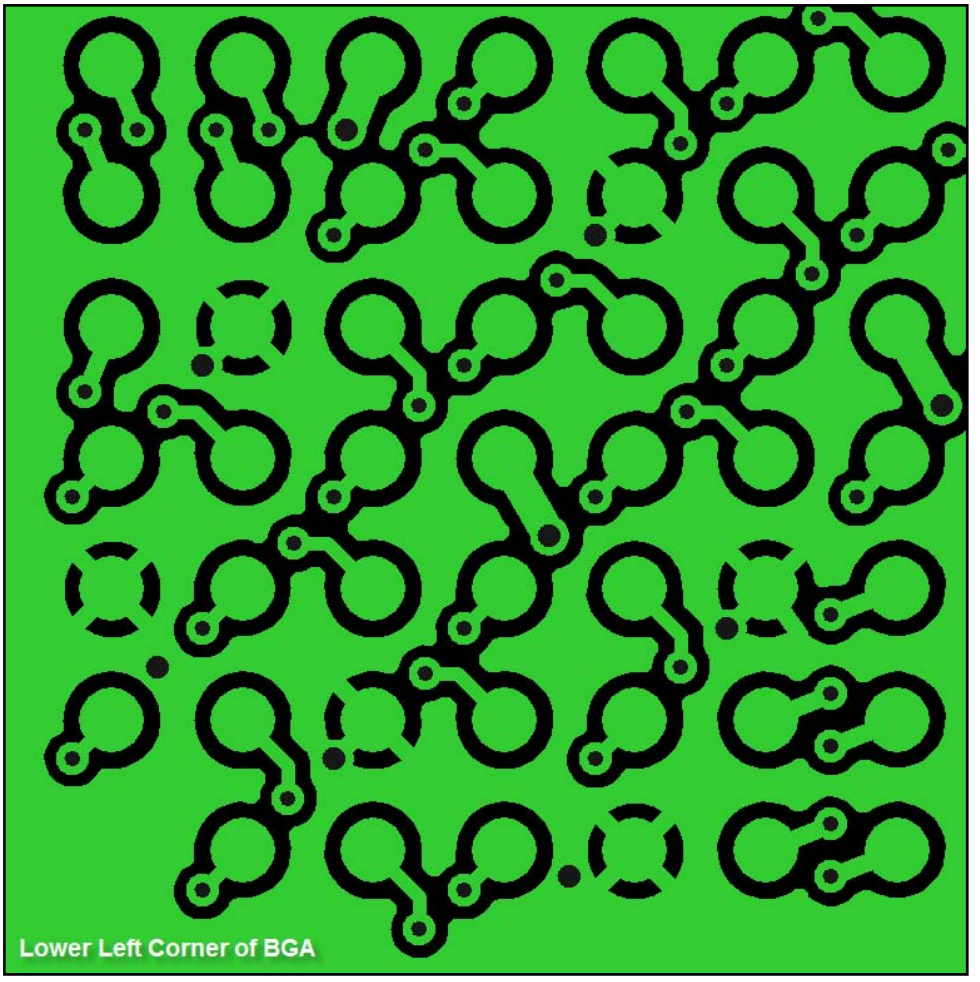


Figure 6-28: Top layer ground plane detail without net class colors (Test 3)

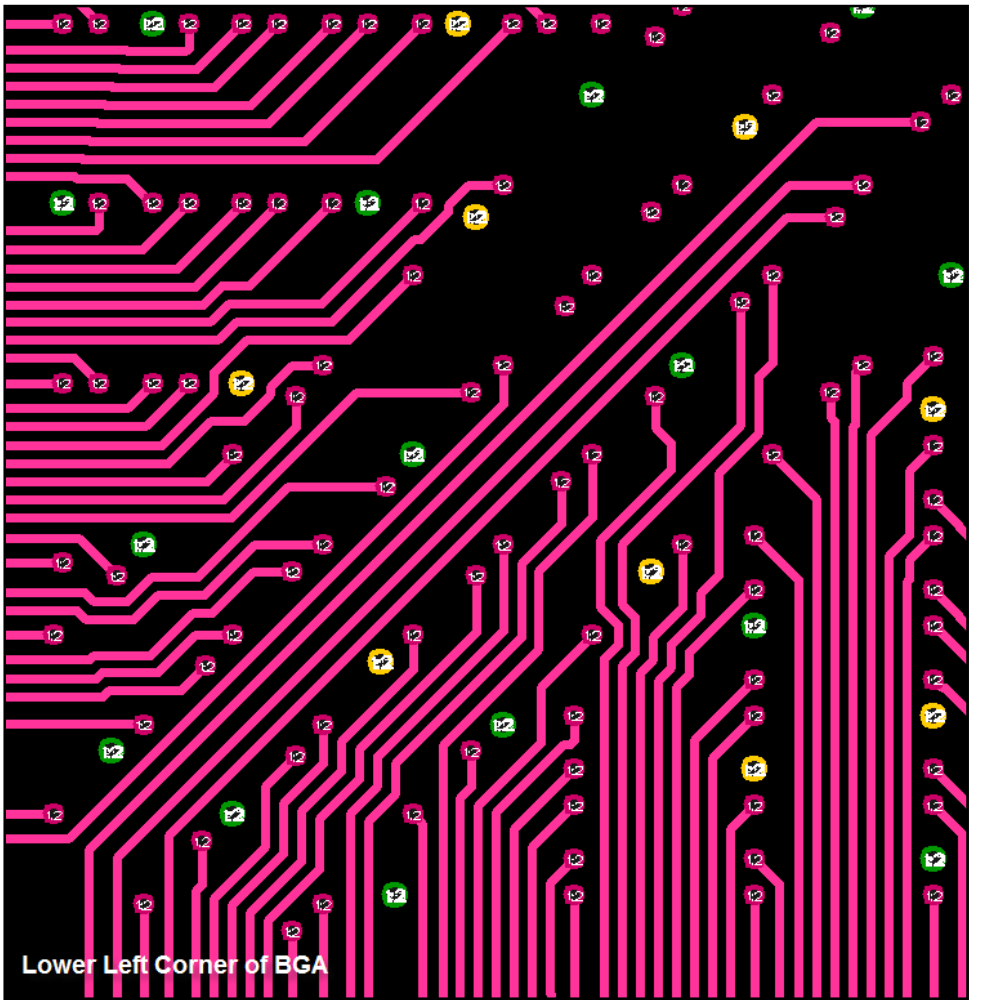


Figure 6-29: Test 3 layer 2 corner via patterns and breakouts (Test 3)

Notes

- All the 1:2 fanout vias that are connected on this layer do not need to extend to layer 3. The ground and power vias extend layer-by-layer all the way through the board.
- The route density has been maximized by shifting the vias into a diagonal, horizontal or vertical alignment.

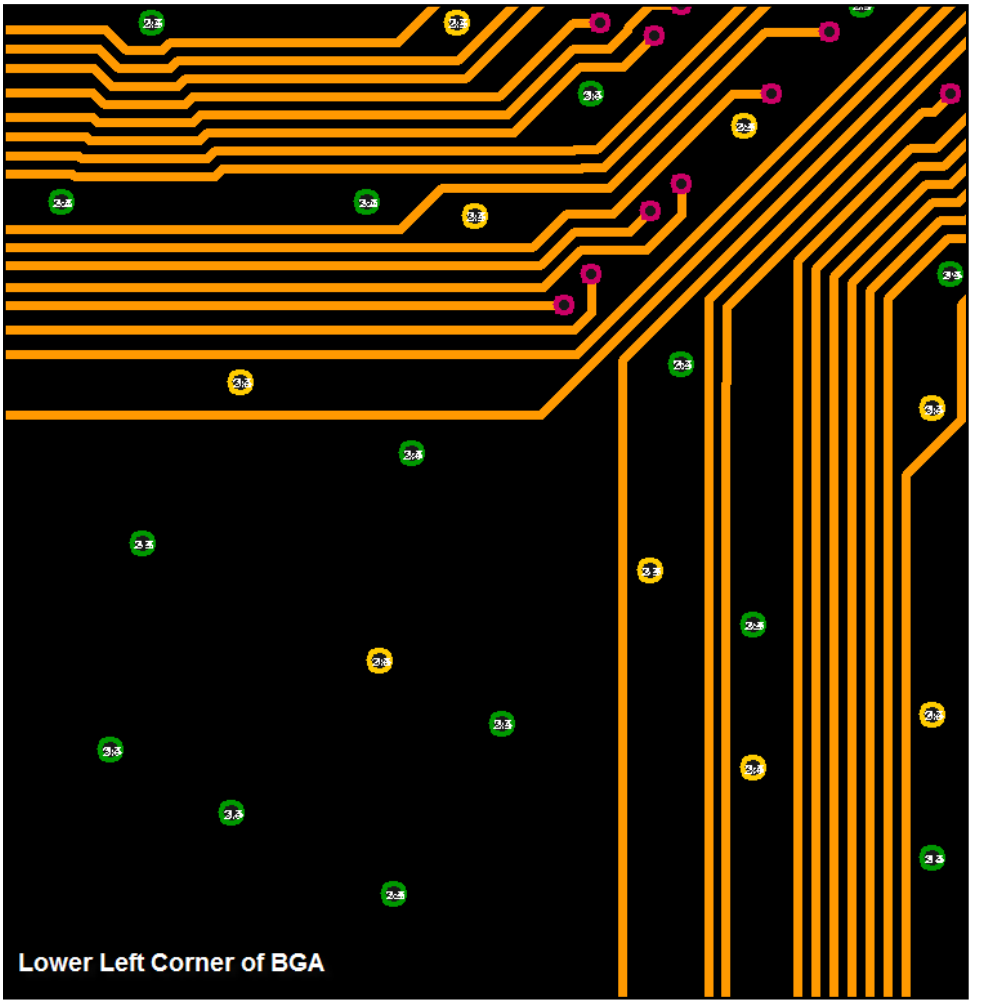


Figure 6-30: Layer 3 corner via patterns and breakouts (Test 3)

Notes

- You can see that all the 1:2 vias do not exist on this layer. There is a tremendous amount of room for routing.

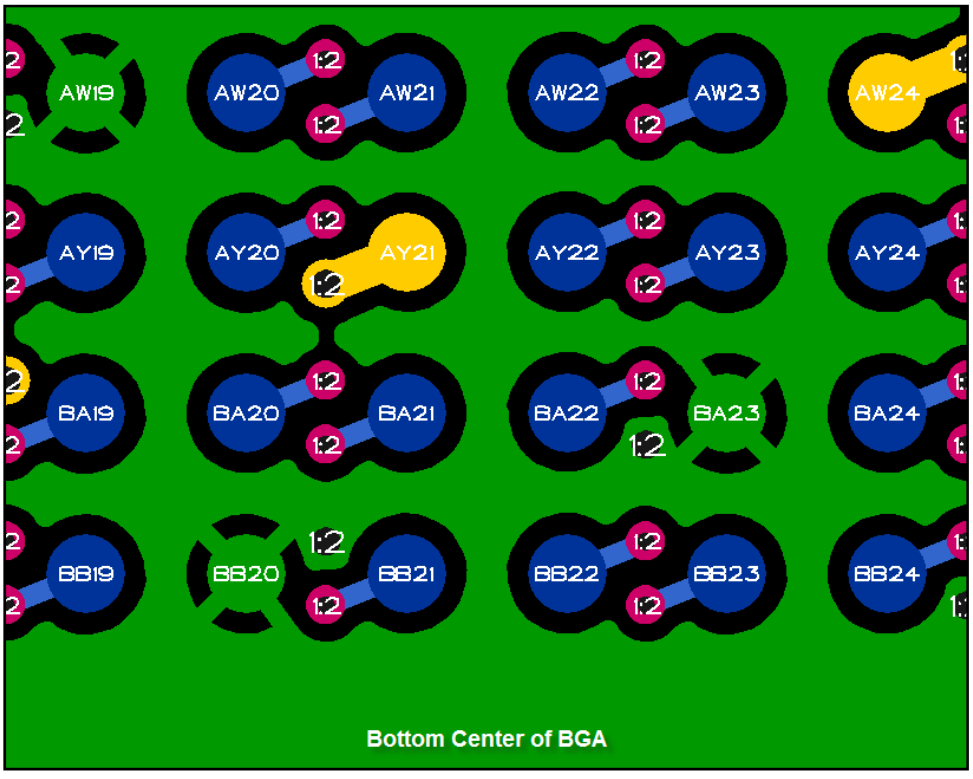


Figure 6-31: Layer 1 center via patterns (Test 3)

Notes

- The vias in the center area of the BGA are aligned either vertically or horizontally and diagonally in the corners.
- This fanout pattern again uses the basic principle of swinging the vias to align them into columns.

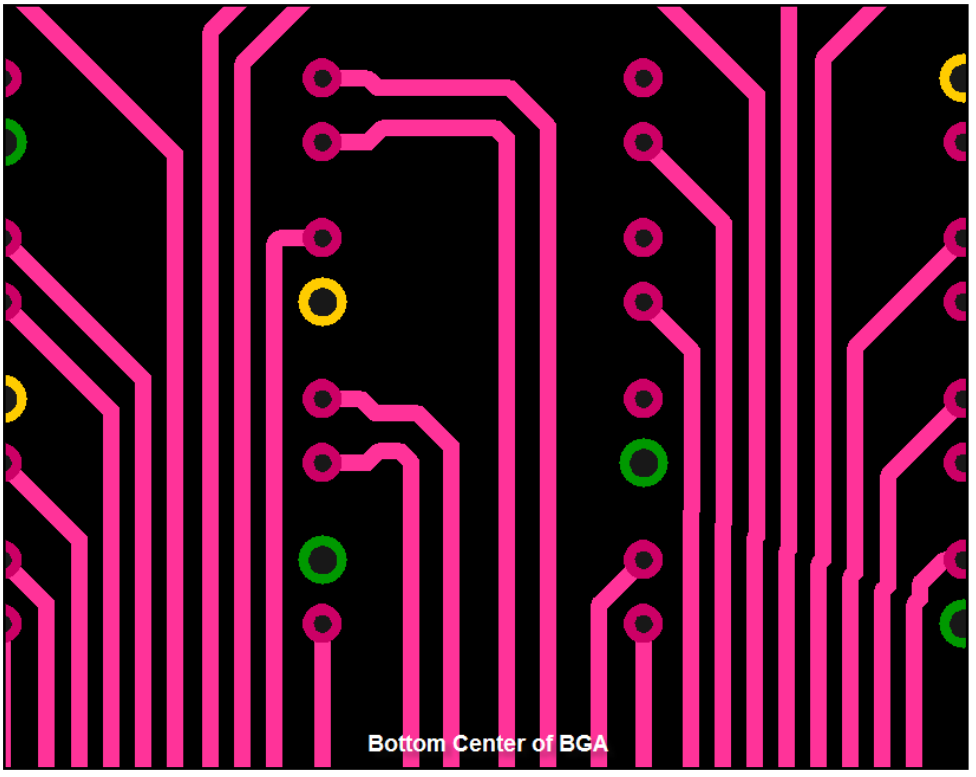


Figure 6-32: Layer 2 center via patterns (Test 3)

Notes

- This method of breakout also allows for spacing requirements of differential pairs. Remember that if through-vias are used, then only one trace can fit between the array of vias under the BGA.

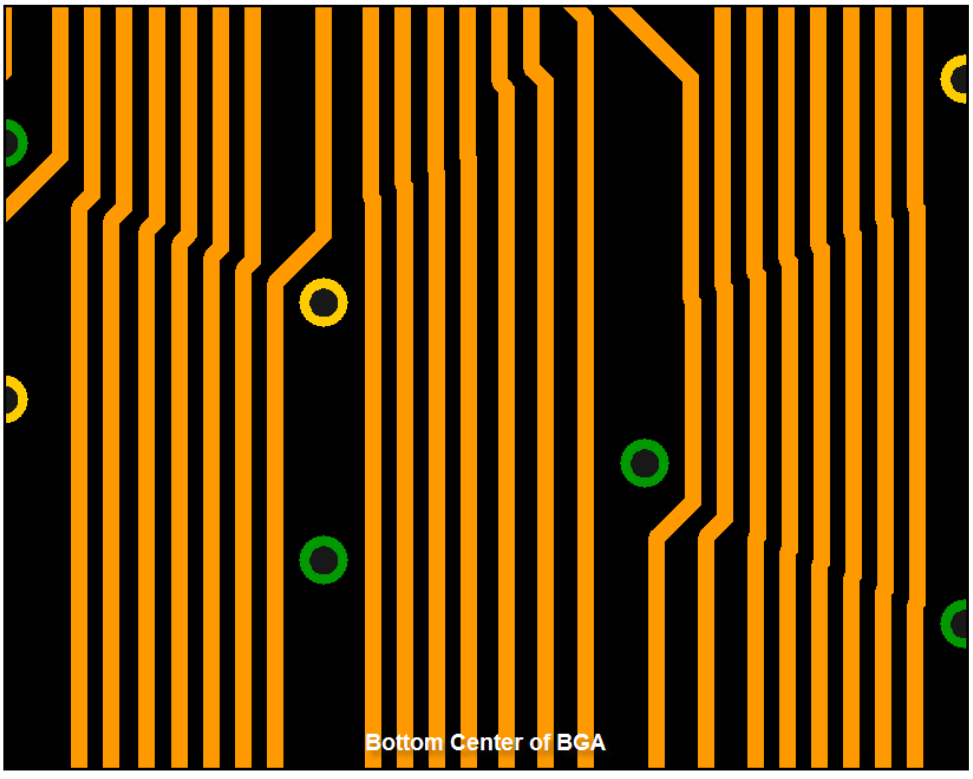


Figure 6-33: Layer 3 center via patterns (Test 3)

Test 3 Breakout Images

Figures 6-34 through 6-36 show the breakouts on all layers using the NSEW method. The total number of signal layers required to breakout this device was three.

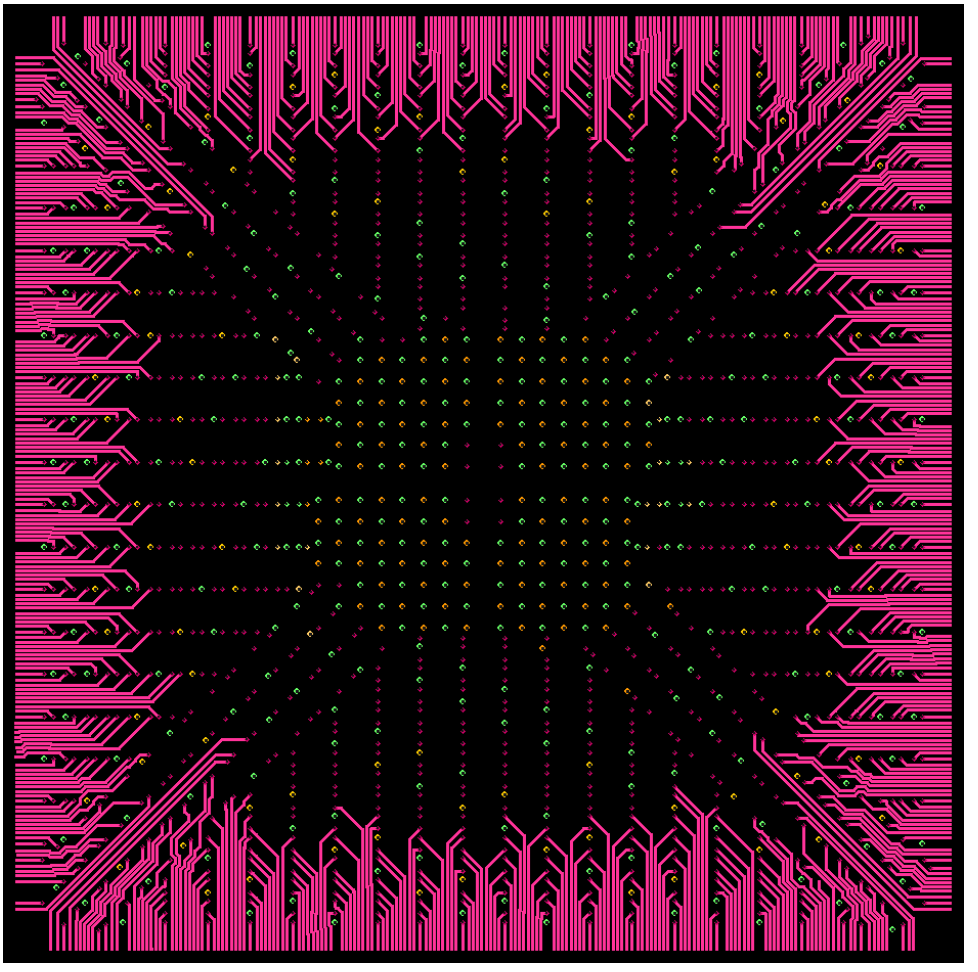


Figure 6-34: First signal layer (Test 3)

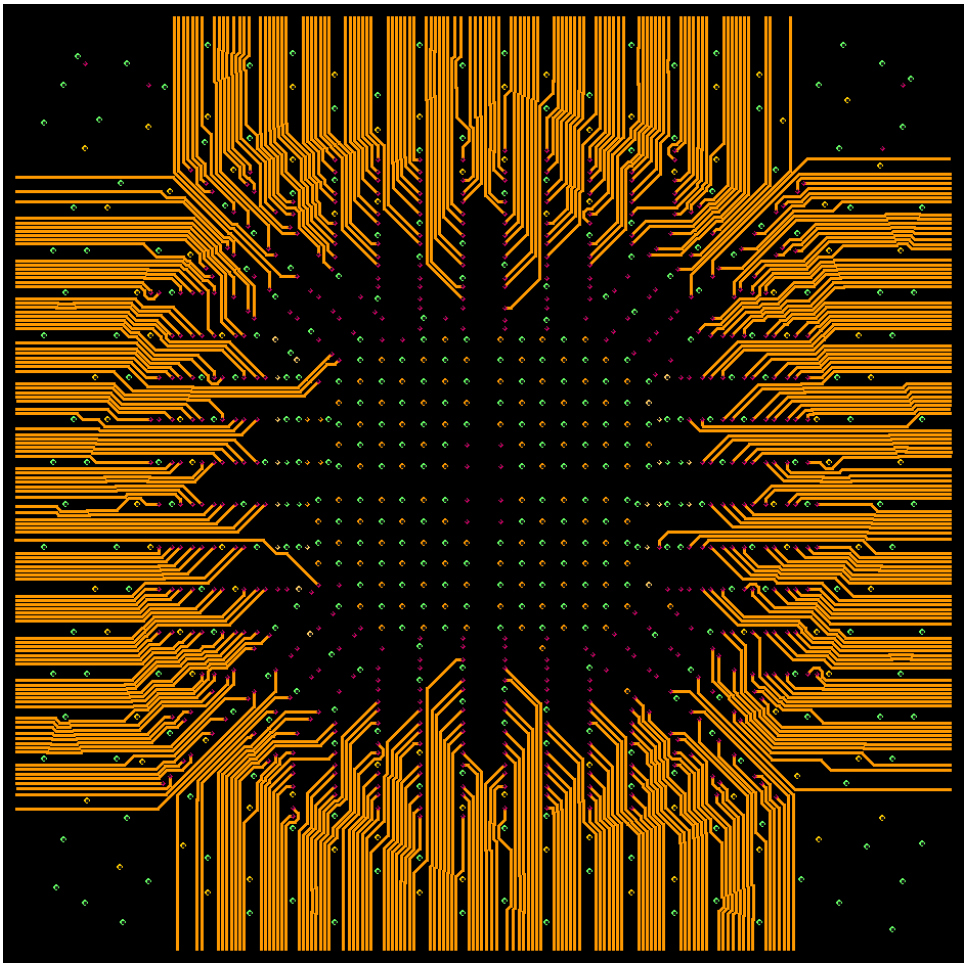


Figure 6-35: Second signal layer (Test 3)

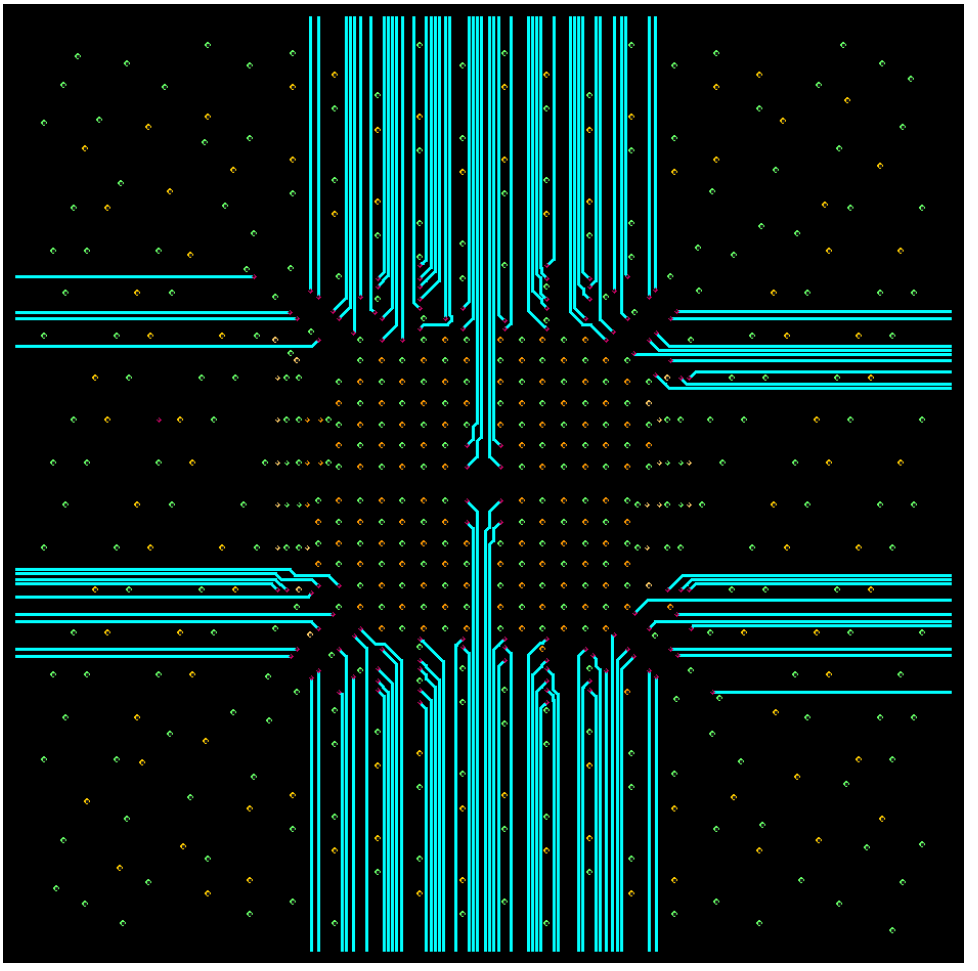


Figure 6-36: Third signal layer (Test 3)

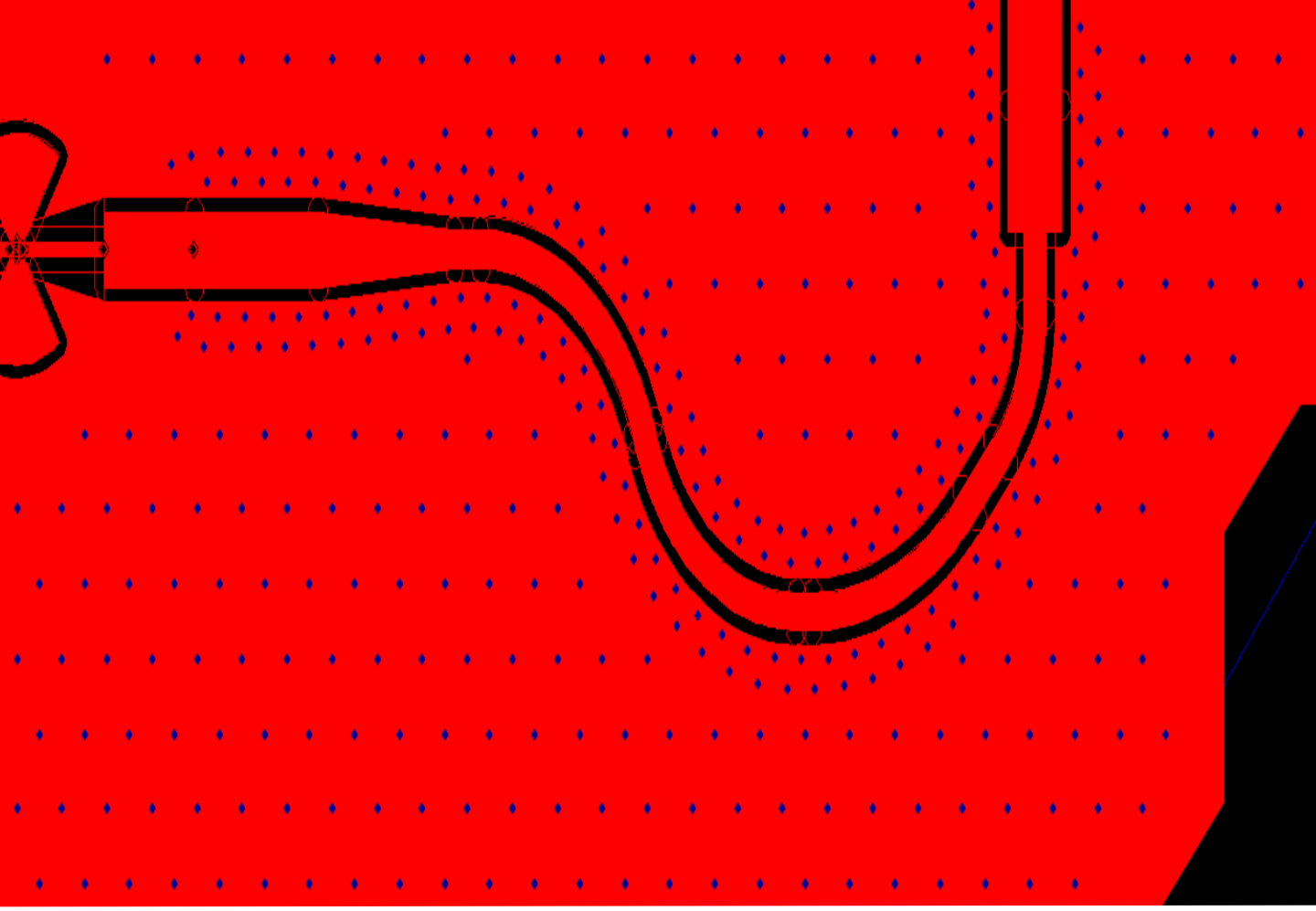
Test 3 Summary

- Applying NSEW breakouts with good fanout patterns enables breakouts on large BGAs in 3 signal layers
- With increased spacing for differential pairs, it probably could be done on 6 signal layers
- The any-layer-via eliminates via stubs
- Using smaller feature sizes makes a significant difference

- If over 2000 pins and 0.8mm pitch, ALIVH is a great solution if you want absolute minimum layer count

Summary

Although 0.8mm pin-pitch BGAs are clearly more difficult to route, using micro-vias and specifically any-layer-vias make the task quite reasonable. When 0.8mm BGAs with over 2000 pins are commonplace, I am hopeful that the any-layer-via method will have been adopted world-wide.



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Chapter Seven - Software for Generating BGA Fanouts

In this second edition, I am adding this chapter to describe how to automatically add fanouts using Mentor Graphics software according to the principles espoused in the rest of this book. This software is available in Expedition PCB and BoardStationXE release 2007.3.

The purpose of this dialog is to automatically generate effective fanout patterns for large BGAs that will increase the route density and potentially reduce the number of layers needed for routing. The general concept applied is to swing the fanouts into columns and rows to provide significantly greater route density.

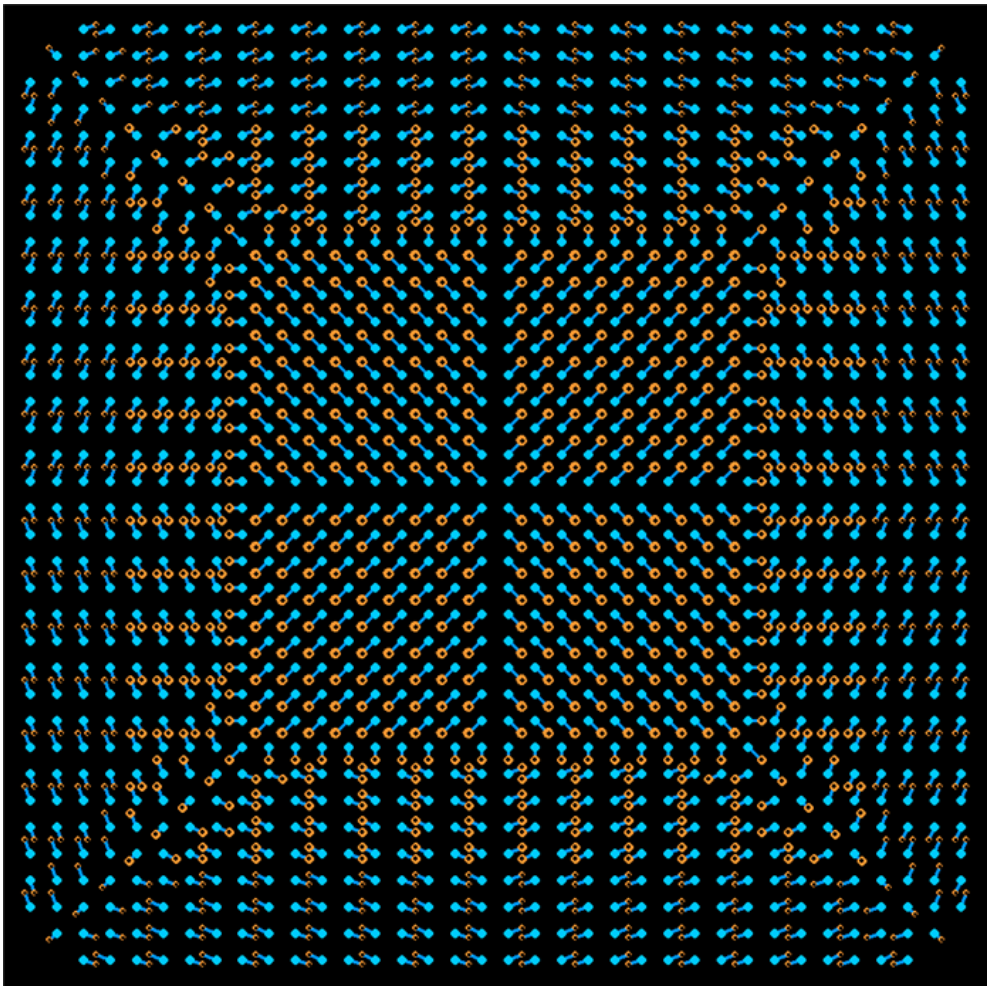


Figure 7-1: Example fanouts generated automatically

Method

This dialog uses the concept of “Regions” (as described in chapter 4) in which the BGA is divided into four areas; each area should get a different via pattern to optimize the route density.

Regions

Figure 7-2 shows four regions plus the Diagonal Via area. Each region has its own characteristics and allows the user to have some flexibility in the fanout via pattern style.

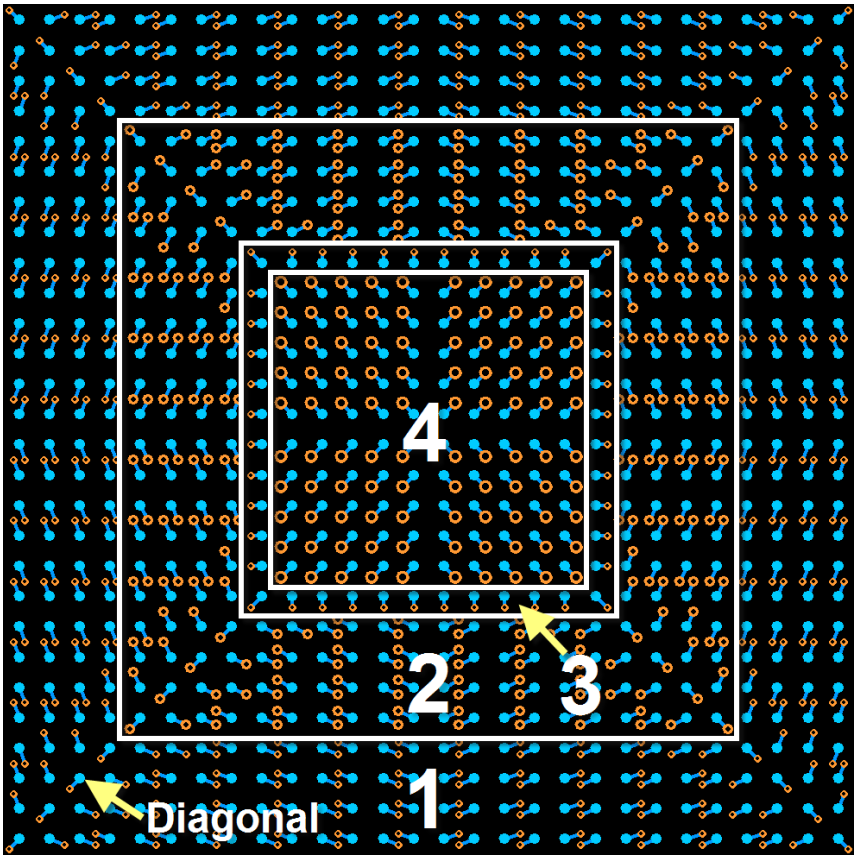


Figure 7-2: Fanout regions

Adding Blind and Through-Vias

This section of the application is used to add the blind-vias and through-vias that attach to the ball pads on the mount side of the BGA.

Region 1

This region consists of the BGA pins around the perimeter of the BGA. The number of rows included in this region is user definable. Usually the fanouts in this region can just have a short 1:2 or 1:3 via span and will not require a buried via because with the appropriate choice of rows, you can route all of these escapes on the buildup layers (two and/or three).

By modifying the via-pad options, you can get a variety of patterns as shown in figure 7-3.

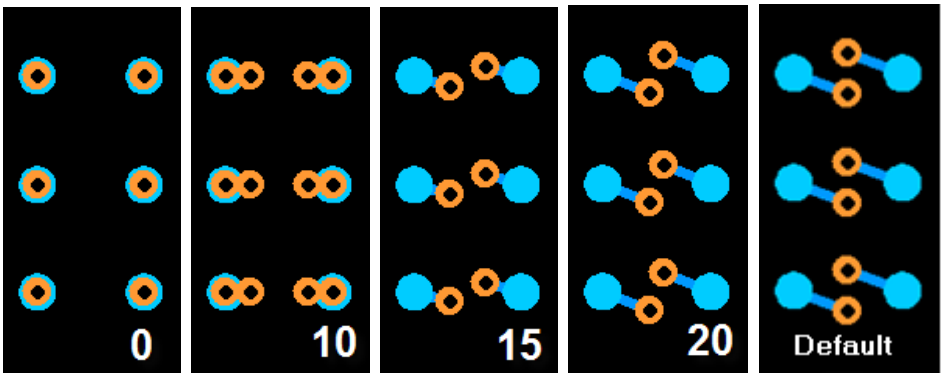


Figure 7-3: Effects of changing via-pad spacing in region 1 and 2

Region 2

This region contains the BGA pins inside Region 1 and extends into the BGA with a user defined number of rows. The patterns that can be created are the same as in region 1. It is likely that the via span for region 2 would be some blind via that extends from layer 1 down to layer 3 or 4 – depending on your stackup.

Region 3

This region is a transition area between Region 2 and Region 4. Region 4 will get some kind of dog-bone pattern and it conflicts with the Region 2 pattern and without a transition pattern, the vias would have DRC errors.

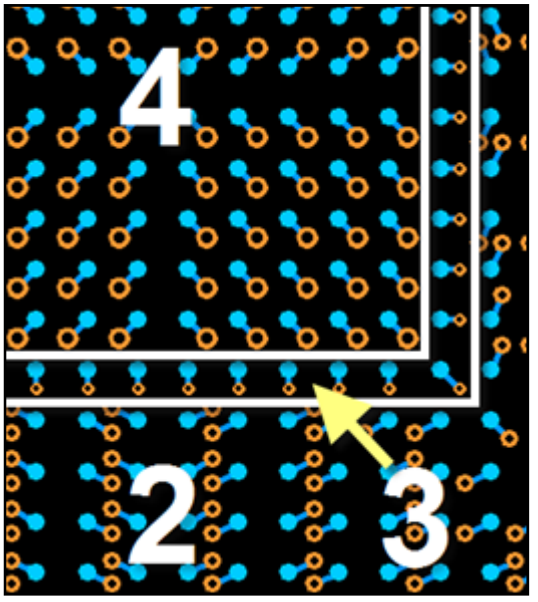


Figure 7-4: Region 3 transition pattern

Region 4

All the remaining BGA pins inside of the other regions are in Region 4. A dog-bone pattern is used and the user has control over the center to center spacing between the via and ball pad. Most likely this region will use a through-via since the pins in the center are usually power and ground.

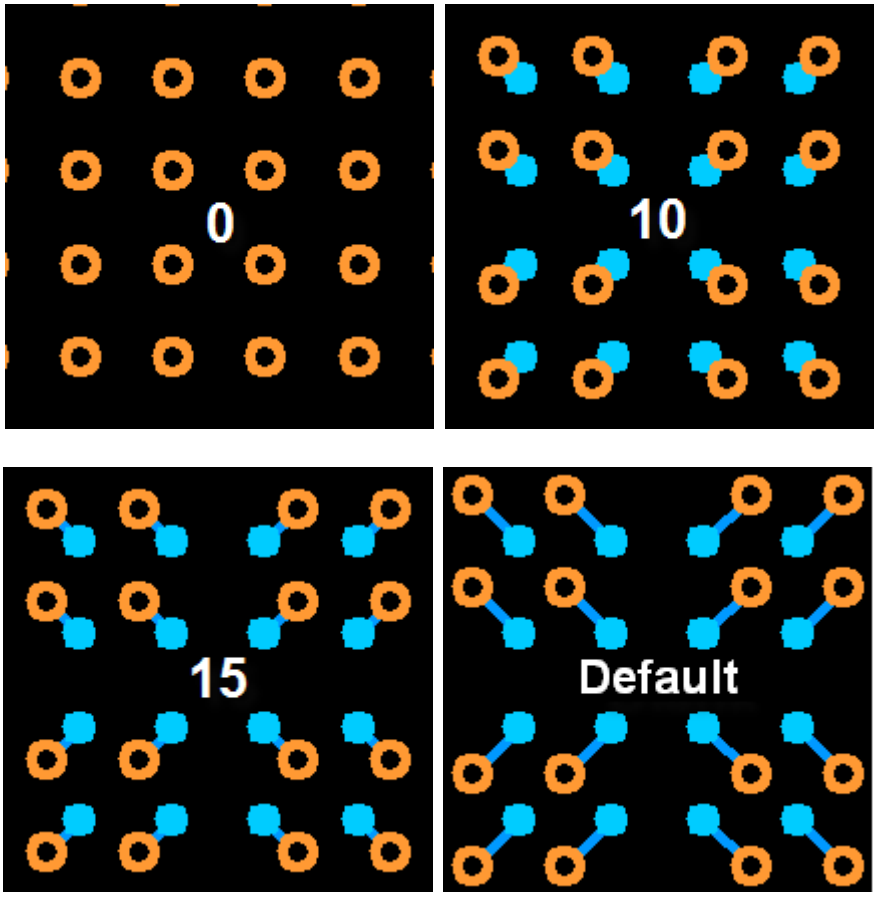


Figure 7-5: Effects of changing via-pad spacing in region 4

Adding Buried Vias

The intent of this section is to add buried-vias that attach to the blind-vias added in the previous section. Then you can add additional vias to the buried-vias and extend the total fanout through the board.

Generally I recommend adding buried vias for the ball pads in Region 2 if and only if you have enough rows assigned to that region that it is not possible to escape route all of them on just a single layer.

You may also want to use this section to define fanouts that go all the way through the board for the power and ground pins. To accomplish this, you should use the Net Filter and thereby select only the power and ground pins that should have the defined fanout pattern applied.

Via Locations

- **Default** – If you leave the two fields blank for a given span, then we apply a default spacing and angle that results in the following:
  - The initial buried-via span is placed directly underneath the ball pad.

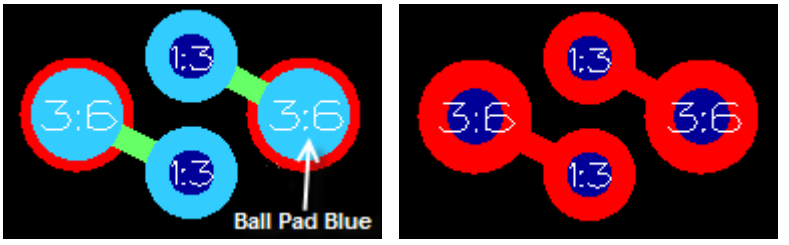


Figure 7-6: Default buried via pattern

  - The blind via span added to the buried via is placed directly underneath the mount-side blind-via.

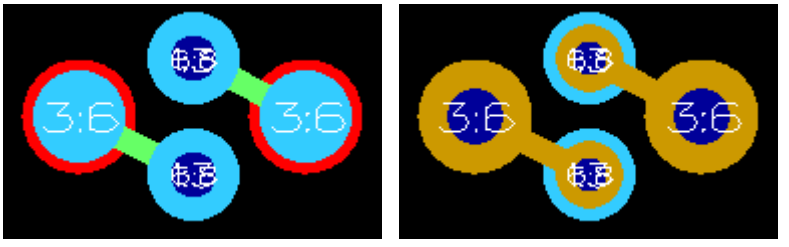


Figure 7-7: Default blind via

Via-Via Spacing –You can use this parameter to adjust the distance that the via-span has from the previous span.

- For example, if you change the spacing to “30th” then the via will be pushed out along the same angle.

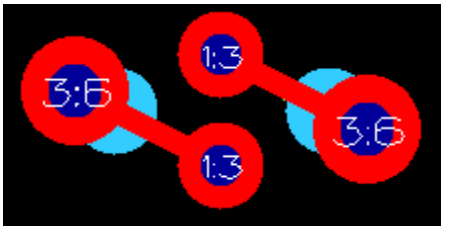


Figure 7-8: Layer 1 and layer 6 view

Angle – The angle controls the angle of the trace being added and of course affects the location of the via span.

- This angle is relative to the previous span. For example, a 0° angle will result in the trace continuing in the same direction as the previous span.

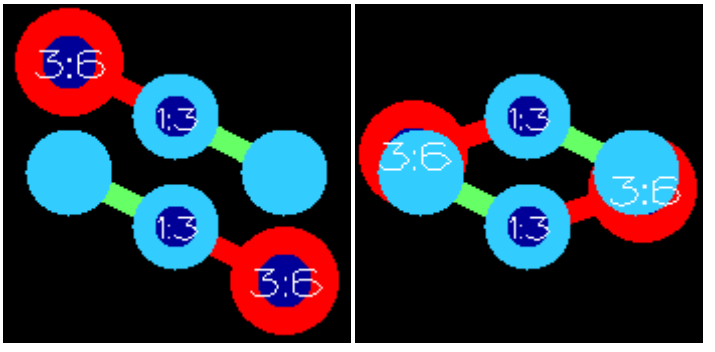


Figure 7-9: 0° angle and 45° angle

Additional Example

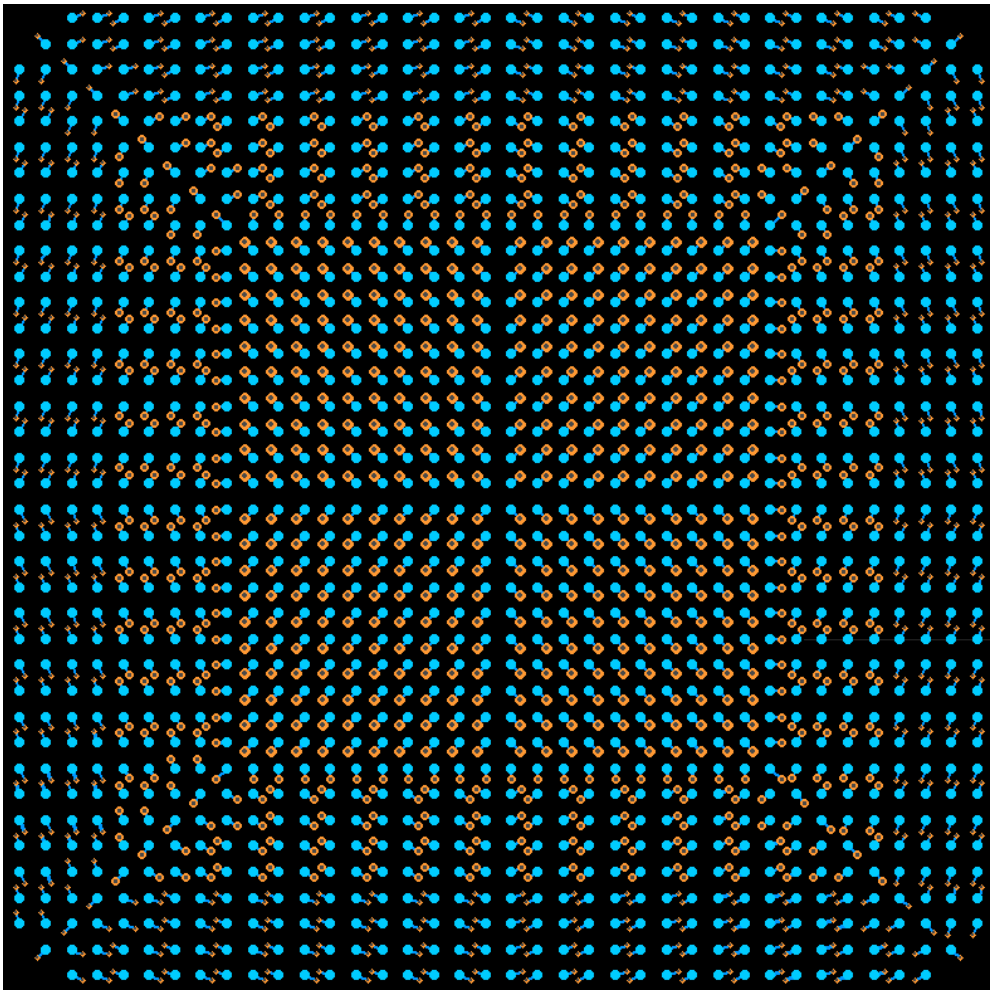


Figure 7-10: Variations on the default patterns

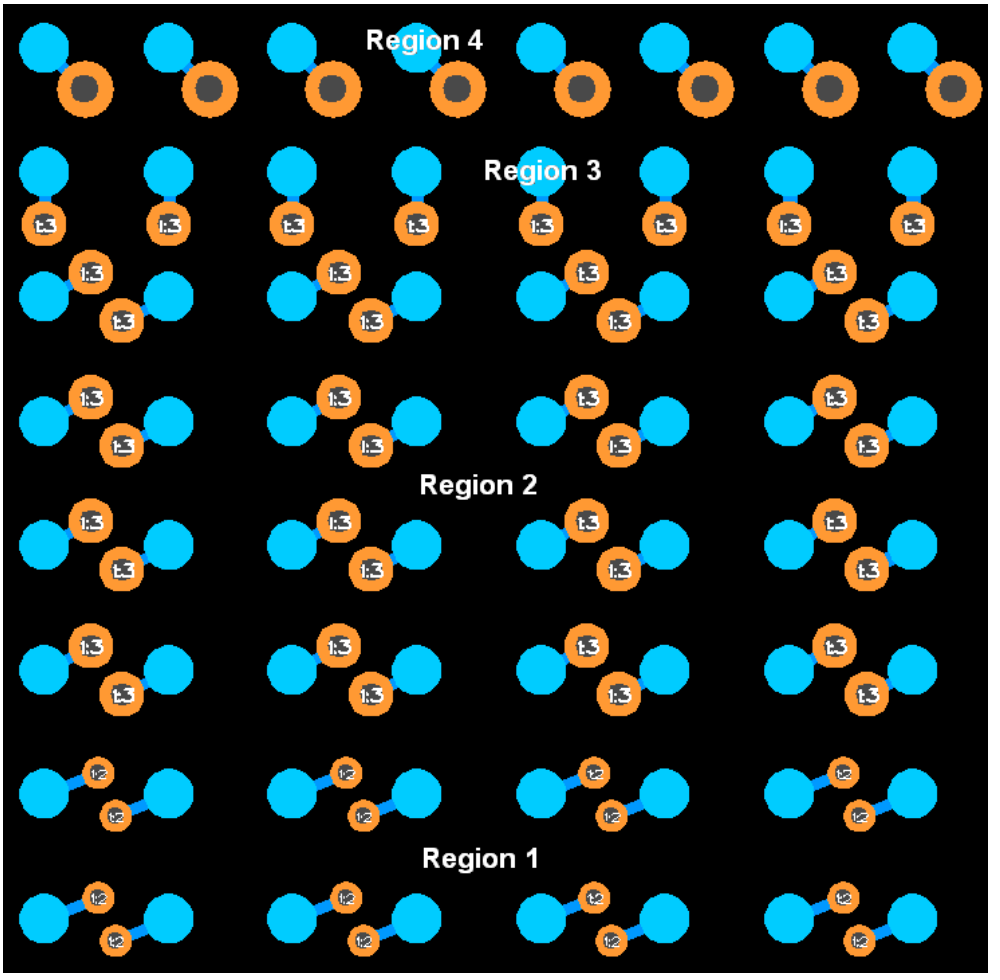


Figure 7-11: Variations on the default patterns details

Conclusion

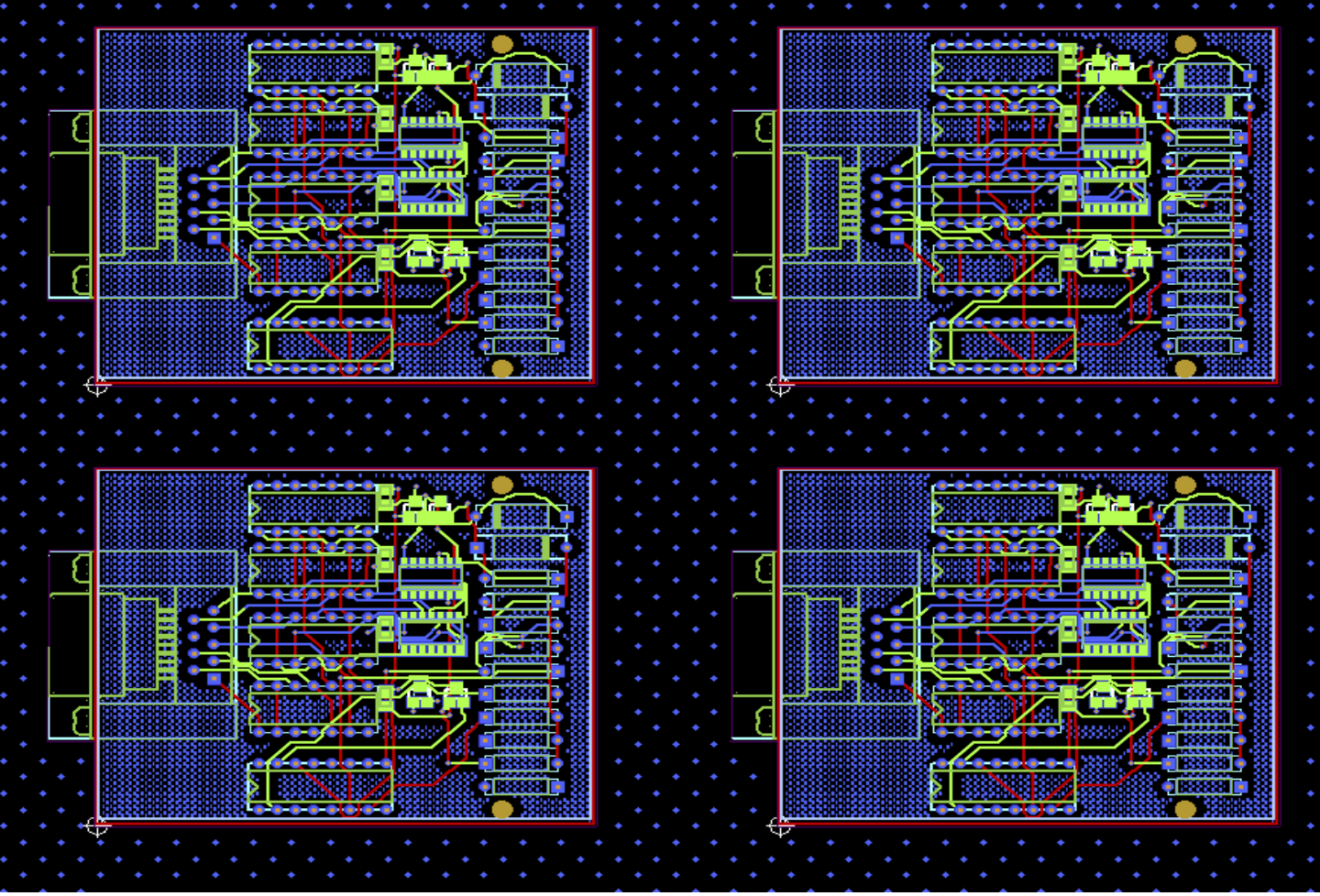
One of the factors that make routing large BGAs so difficult is the high number of variables involved in the process. For example, while one fanout method may work with one set of design rules, it may not work with others. I believe the solutions explored in this book involve sufficient variety to cover a broad spectrum of design challenges.

The most important technique for meeting your layer reduction and signal integrity goals is applying an effective fanout pattern that increases route density. Usually each BGA will require two or three different via patterns for best routing results. At a minimum, the fanout patterns presented in this book should give you some valuable insight to what is possible; at best, you will be able to apply these patterns directly to the design challenges faced in the near future.

Once the fanout patterns are established, the escape traces do help the routing process. The chapter on Layer Biased Breakouts demonstrates a significant improvement in to overall routing completion rates.

The research conducted during the process of writing this book is also the source for the functional enhancements to Mentor Graphics Expedition PCB and Board Station XE as described in chapter seven.

Component technology and fabrication methods will continue to evolve; however, the design principles revealed in this book should apply for many years to come.



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About the Author

Charles Pfeil is an Engineering Director at Mentor Graphics, Systems Design Division. He was the original product architect for Expedition PCB and is an inventor of XtremePCB, TeamPCB and XtremeAutoRoute. Charles has been in the PCB industry over 40 years as a designer, owner of a service bureau, and has also worked in marketing and/or engineering management at Racal-Redac, ASI, Cadence, PADS, and VeriBest. He can be contacted through email at charles_pfeil@mentor.com

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BGA Breakouts and Routing

Effective Design Methods for Very large BGAs

Second edition

There are many benefits to using the BGA package; however, its greatest asset, the ability to provide an extremely dense array of thousands of pins, also turns out to be a tremendous problem for PCB designers.

The BGA density and pin count continues to increase; yet, our ability to effectively design with these devices has not kept pace. Fortunately, significant advancements in PCB fabrication technology have enabled further miniaturization in the manufacturing process. These improvements, along with new software and design methods specifically for BGAs provide a means to successfully design using these devices.

This book explores the impact of dense BGAs with high pin-count on PCB design and provides solutions for inherent design challenges.

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