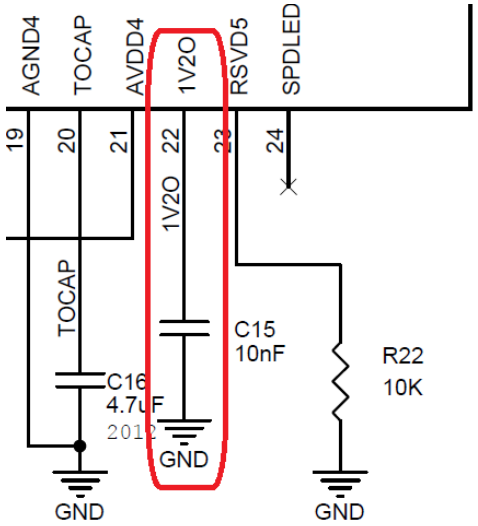
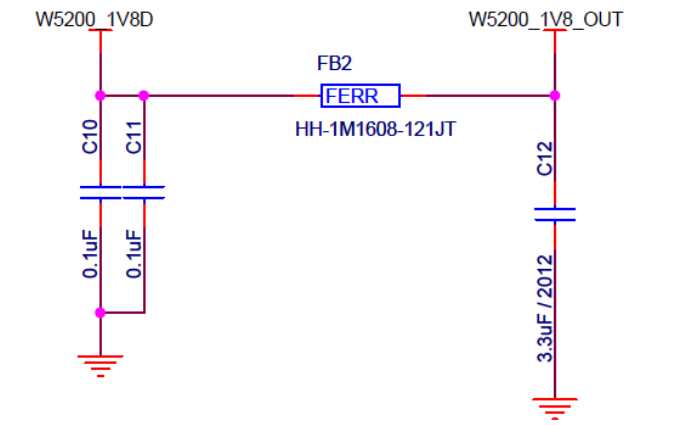
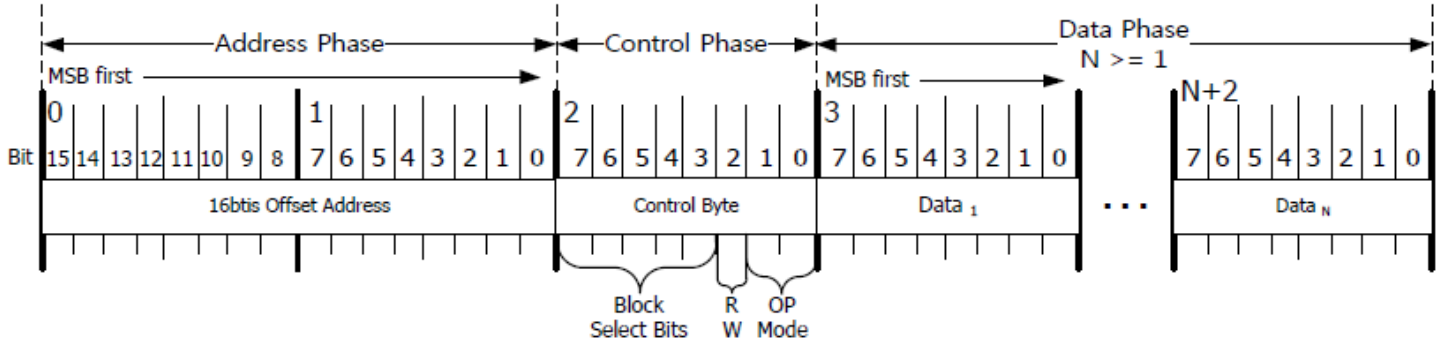
	W5500	W5200
Chip Manufacturing process	0.13um	0.18um
Package type	48 **LQFP** (7*7 mm^2)	48 **QFN**(7*7)
Operation voltage	IO Voltage: 3.3V Core Voltage: **1.2V**	IO Voltage: 3.3V Core Voltage: **1.8V**
Socket	8 Sockets	8 Sockets
SPI Communication Frame	**(*)W5500 SPI Frame**	**(**)W5200 SPI Frame**
SPI speed	**theoretical design speed is 80MHz, minimum guaranteed speed of the SCLK is 33.3 MHz)**	
PPPoE	PPPoE function is supported by firmware	**Hardware** / Firmware both supported.
Interface	SPI	SPI / **Indirect bus mode**
Core Power Design guide	LDO(3.3->1.2v Internally connected) 	Circuit is needed to connect the LDO output externally to the chip. **Chip Out: W5200 Pin14** **Chip In : W5200 Pin8,25** 
PHY Power Down mode	PHY's Power down mode must be set at the **Firmware's PHY Register**	PHY's Power down mode can be set to **external pin**
Weak On LAN	Only WOL over UDP is supported	WOL over Ethernet is supported
PHY Mode setting	PHY mode setting is possible in the Firmware	
Indicate LED	4 output LED SPD / DUP / **ACT** / Link	3 ED SPD / DUP / Link

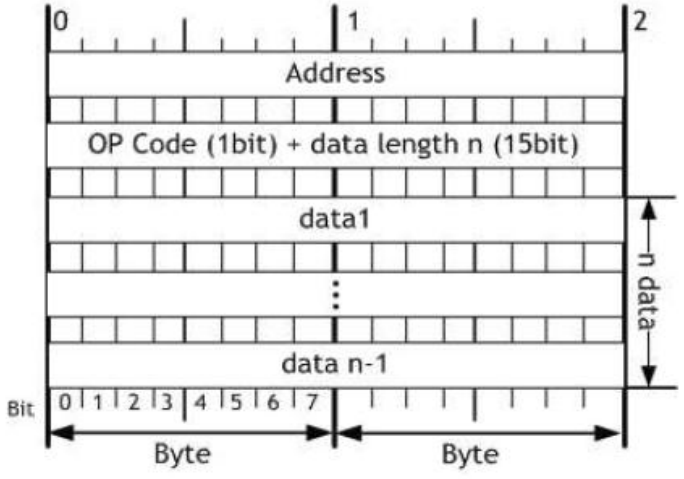
Normal operation Temperature	- Below 45 °C	- Around 70 °C
Auto MDIX	Auto MDIX function is **not available**	Auto MDIX is available
Power consumption	Typical **132mA**	Typical 160mA

(*)W5500 SPI Frame



SPI Frame Format

(**)W5200 SPI Frame



W5200 SPI Frame Format