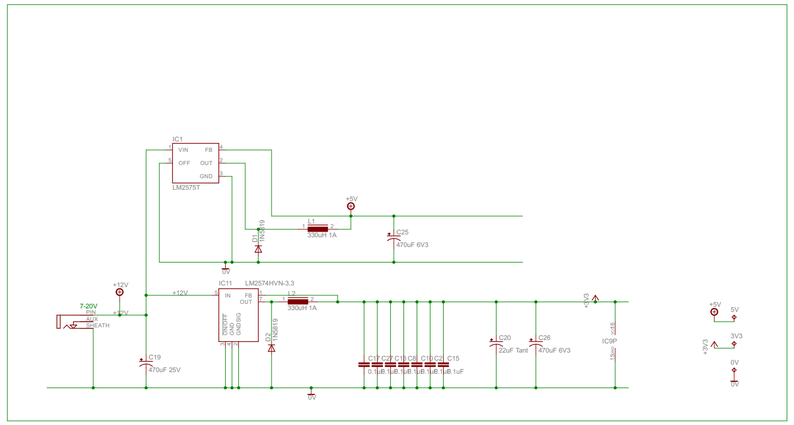
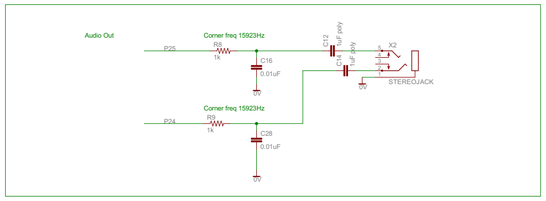
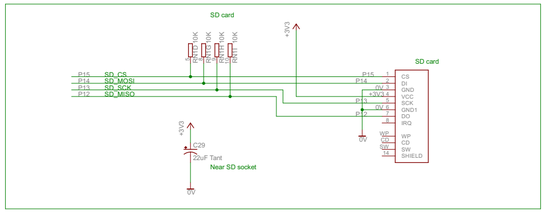
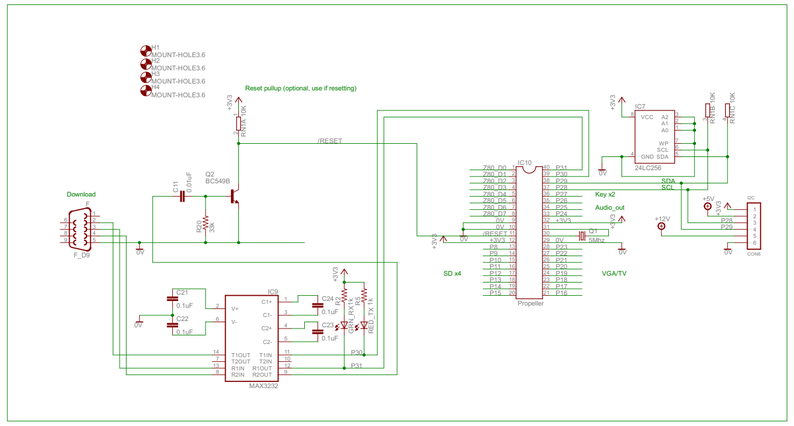
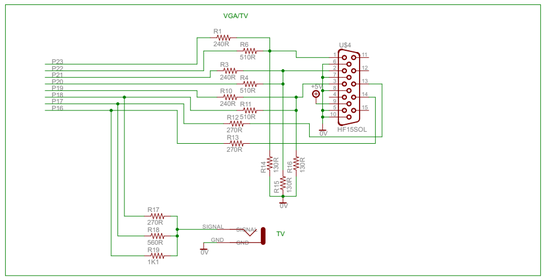
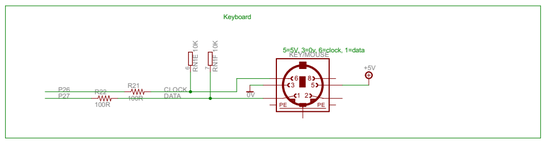

IC1
LM2575T
VIN
FB
OFF
OUT
GND
D1
1N5819
L1
330uH 1A
+5V
C25
470uF 6V3
IC11
LM2574HVN-3.3
IN
FB
OUT
ON/OFF
GND/SG
L2
330uH 1A
D2
1N5819
+12V
7-20V
PWR
AUX
BATH
C19
470uF 25V
C17 C27 C18 C28 C14 C24 C15
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF
C20
22uF Tant
C26
470uF 6V3
+3V3
IC3P
1N4148
5V
3V3
0V

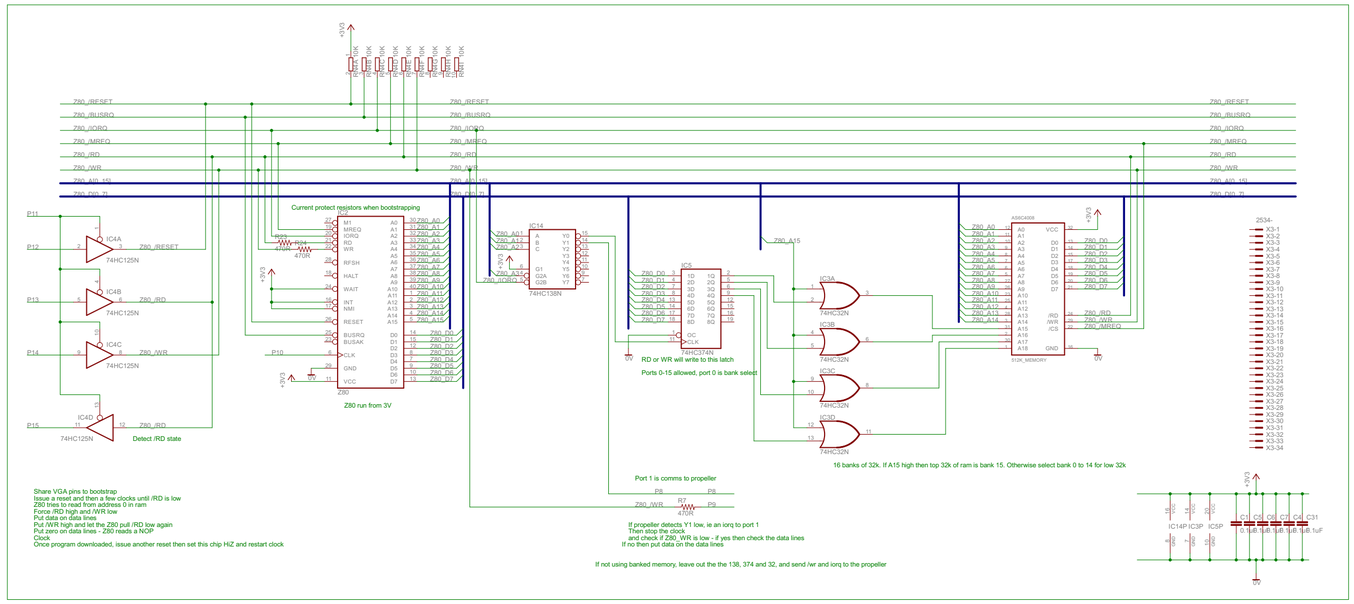

Audio Out
Corner freq 15923Hz
P25
R8
1k
C16
0.01uF
C12
C13
X2
STEREOJACK
Corner freq 15923Hz
P24
R9
1k
C28
0.01uF


SD card
R5 10K
R6 10K
R7 10K
R8 10K
RNT1 10K
+3V3
P15 SD_CS
P14 SD_MOSI
P13 SD_SCK
P12 SD_MISO
SD card
CS
DI
GND
VCC
SCK
GND1
DO
IRQ
WP
CD
SW
SHIELD
C29
22uF Tant
Near SD socket


M1
M2
M3
M4
MOUNT-HOLE3.6
Reset pullup (optional, use if resetting)
R14 10K
/RESET
Download
F_D9
C11
0.1uF
Q2
BC549B
R20
3K
IC7
24LC256
VCC
A2
A1
A0
WP
SCL
GND SDA
R15 10K
R16 10K
SDA
SCL
IC10
Propeller
Z80_D0
Z80_D1
Z80_D2
Z80_D3
Z80_D4
Z80_D5
Z80_D6
Z80_D7
0V
/RESET
+3V3
P8
P9
P10
P11
P12
P13
P14
P15
P31
P30
P29
P28
P27
P26
P25
P24
P23
P22
P21
P20
P19
P18
P17
P16
Key x2
Audio_out
C1
10uhz
SD x4
VGA/TV
IRQ
+5V
+12V
I2C
CONN
C21
0.1uF
C22
0.1uF
IC9
MAX232
V+
V-
C1+
C1-
C2+
C2-
T1OUT
T2OUT
R1IN
R2IN
T1IN
T2IN
R1OUT
R2OUT
C24
0.1uF
C23
0.1uF
R17 1k
R18 1k
RED_TX
GRN_RX


VGA/TV
R1
340R
R6
510R
R2
240R
R4
510R
R10
240R
R11
510R
R13
240R
R12
510R
R15
270R
R16
270R
U54
HF15SOL
R14
560R
R18
560R
R19
150R
+5V
R17
270R
R19
560R
R18
1k1
SIGNAL
GND
TV


Keyboard
R5 10K
R6 10K
5=5V, 3=0v, 6=clock, 1=data
PS2-MINI-DIN
+5V
P26
P27
R22
100R
R21
100R
CLOCK
DATA


+3V3
R1 10K
R2 10K
R3 10K
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
Z80_/RESET
Z80_/BUSRQ
Z80_/IORQ
Z80_/MREQ
Z80_/RD
Z80_/WR
Z80_A0_15
Z80_D0_7
P11
P12
P13
P14
P15
IC4A
IC4B
IC4C
IC4D
74HC125N
Z80_/RESET
Z80_/RD
Z80_/WR
Detect /RD state
Current protect resistors when bootstrapping
R24
470R
M1
MREQ
IORQ
RD
WR
RFSH
HALT
WAIT
INT
NMI
RESET
BUSRQ
BUSAK
CLK
GND
VCC
Z80
Z80 run from 3V
IC14
74HC138N
Z80_A01
Z80_A12
Z80_A14
Z80_/IORQ_32
IC5
74HC374N
RD or WR will write to this latch
Ports 0-15 allowed, port 0 is bank select
Z80_A15
IC3A
IC3B
IC3C
IC3D
74HC32N
A56C4008
512K_MEMORY
/RD
/WR
/CE
16 banks of 32k. If A15 high then top 32k of ram is bank 15. Otherwise select bank 0 to 14 for low 32k
2534-
X3-1
X3-2
X3-3
X3-4
X3-5
X3-6
X3-7
X3-8
X3-9
X3-10
X3-11
X3-12
X3-13
X3-14
X3-15
X3-16
X3-17
X3-18
X3-19
X3-20
X3-21
X3-22
X3-23
X3-24
X3-25
X3-26
X3-27
X3-28
X3-29
X3-30
X3-31
X3-32
X3-33
X3-34
Share VGA pins to bootstrap
Issue a reset and then a few clocks until /RD is low
Z80 tries to read from address 0 in ram
Force /RD high and /WR low
Put data on data lines
Put /WR high and let the Z80 pull /RD low again
Put zero on data lines - Z80 reads a NOP
Clock
Once program downloaded, issue another reset then set this chip HiZ and restart clock
Port 1 is comms to propeller
P8
P9
Z80_/WR
R7
470R
If propeller detects Y1 low, ie an iorq to port 1
Then stop the clock
and check if Z80_WR is low - if yes then check the data lines
If no then put data on the data lines
If not using banked memory, leave out the the 138, 374 and 32, and send /wr and iorq to the propeller
IC14P
IC3P
IC5P
C31
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF