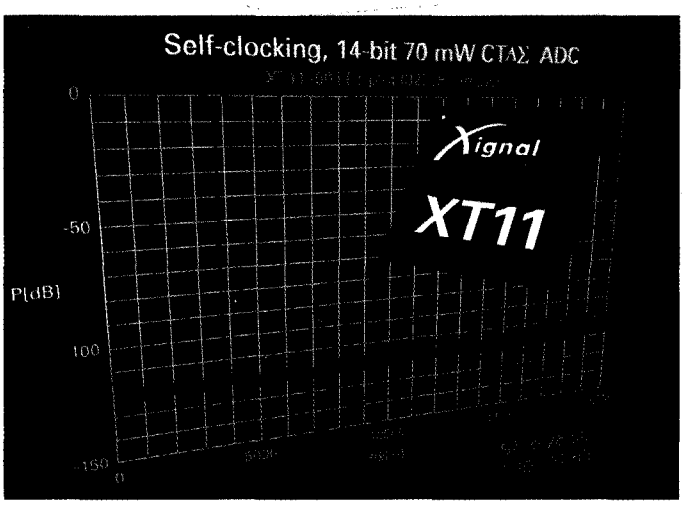
12- and 14-bit ADCs break the 100 mW power barrier

Xignal Technologies AG has launched the industry's lowest power, 14-bit and 12-bit, 40 MHz analog-to-digital converters (ADCs). Based on the company's recently announced breakthrough in Continuous Time Delta Sigma (CT¢Σ) technology, the 12-bit (XT11200) and 14-bit (XT11400) resolution devices consume only 70 mW while operating at 20-40 MSPS data rate. This is half the power consumption of the nearest best-in-class alternatives and the first time such performance has been available at the sub-100 mW power level, and in this instance with increased integration to simplify system design. These new ADCs eliminate costly and power-hungry anti-alias filters. They further simplify system design by providing an on-chip, precision (low jitter) sample clock. Additionally, the devices are easy to drive, needing no differential input buffer. XT11x00 ADCs can handle 4 V peak-peak input signals while operating from a 1.2 V DC supply and they offer exceptional linearity and signal-to-noise (SNR) performance.

The XT11 family utilizes a fast, third-order continuous time delta sigma modulator, combined with an on-chip digital filter and tunable loop filter. These circuit innovations substantially reduce



the design effort needed to deploy a high performance data acquisition system. In addition, CT¢Σ architecture eliminates the need for external anti-aliasing filters allowing the ADC to sample the entire first Nyquist frequency zone (0 to 20 MHz) with almost no wasted bandwidth.

Despite offering a power Figure of Merit (FOM) half that of current pipeline ADCs, there is no trade-off in linearity or electrical performance. The XT11400 has a signal-to-noise ratio (SNR) of 76 dB and total harmonic distortion (THD) of –82 dB. The XT11200 turns in an SNR of 71 dB and THD of –78 dB.

Previous low-voltage ADCs have only been able to handle limited analog input signal ranges, typically less than the supply voltage. This works against achieving high SNR and low THD. Attempts to increase dynamic range have traditionally been at the expense of increased power consumption. In contrast, Xignal's ADCs can handle 4 V peak-peak signal levels — over three times their 1.2 V operating voltage.

Accurate clock signals are key to an ADC achieving high dynamic range; errors in clock signals (e.g. jitter) show up as errors in the ADC conversion process, and consequently a reduction in the SNR of the device. The XT11 family members utilize a proprietary self-clocking circuit that eliminates the need for an external highly accurate, complex clocking scheme. The on-chip clock is driven from an inexpensive external crystal (ranging from 13.5 to 27 MHz). An on-chip inductive resonator based PLL generates a clean (low jitter) sample clock that is also brought to an external pin and made available for use as an accurate reference clock for other components on the printed circuit board. This is ideal for parallel operation of multiple ADCs in multi-channel systems.

Xignal's CT¢Σ based XT11 family requires no sample and hold circuit to function, but rather uses a simple, current driven (resistive) input stage. This eliminates the need for expensive external differential drivers, reducing overall system cost, design time and system power.

The XT11400 & XT11200 are pin-compatible and are available in a 6 x 6 mm QFN 40 pin package.

The combination of low power and high dynamic range offered by the XT11 family makes these parts ideal for performance driven applications such as medical imaging, ultrasound, radar-based applications, communication systems, image sensing, and test and measurement.

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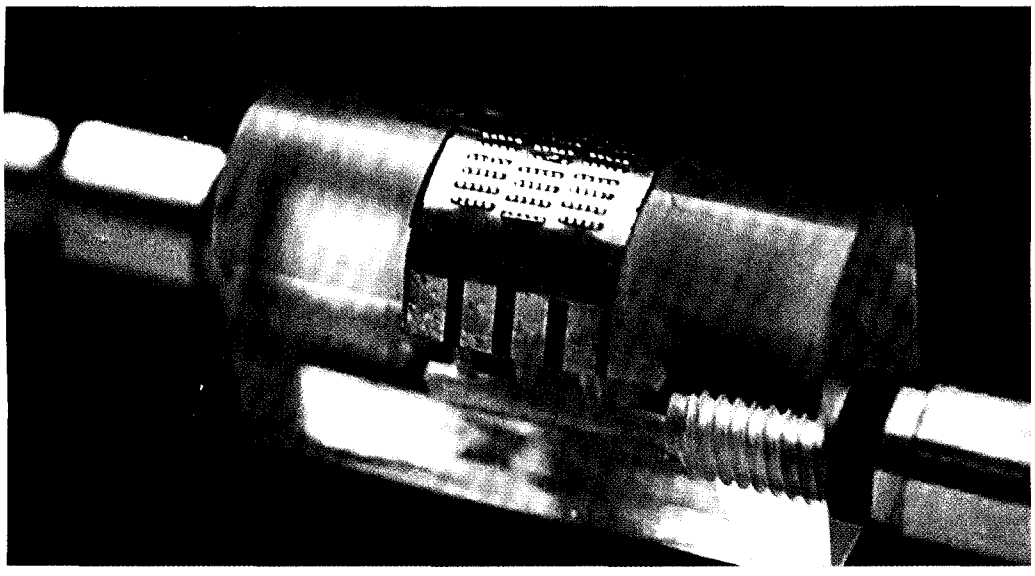
Further information from www.xignal.com



Micro size fuel cell made from polymeric and metal foil supplies 160 mW from 1 cm².

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