LP3988 Micropower, 150 mA Ultra Low-Dropout CMOS Voltage Regulator With Power Good

Check for Samples: LP3988

FEATURES

- **5-Bump Thin DSBGA Package**
- **SOT-23-5 Package**
- **Power-Good Flag Output**
- **Logic Controlled Enable**
- **Stable with Ceramic and High-Quality Tantalum Capacitors**
- **Fast Turn-On**
- **Thermal Shutdown and Short-Circuit Current Limit**

KEY SPECIFICATIONS

- **Input range: 2.5V to 6V**
- **Ooutput current: 150 mA**
- **PSRR at 10 kHz: 40 dB**
- **Quiescent current when shut down: ≤ 1µA**
- **(Typical) Fast Turn-On time: 100 µs**
- **Typical dropout with 150 mA load: 80 mV**
- **Junction temperature range for operation: −40°C to +80°C**
- **Output voltages: 1.85V, 2.5V, 2.6V, 2.85V, 3V, and 3.3V**

APPLICATIONS

- **CDMA Cellular Handsets**
- **Wideband CDMA Cellular Handsets**
- **GSM Cellular Handsets**
- **Portable Information Appliances**
- **Tiny 3.3V ± 5% to 2.85V, 150 mA Converter**

DESCRIPTION

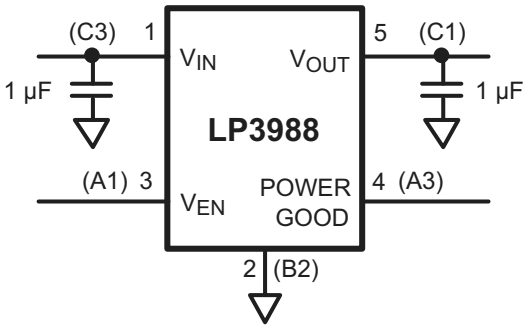
The LP3988 is a 150 mA low dropout regulator designed specially to meet requirements of Portable battery-applications. The LP3988 is designed to work with a space-saving, small 1µF ceramic capacitor. The LP3988 features an Error Flag output that indicates a faulty output condition.

The LP3988's performance is optimized for battery powered systems to deliver low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

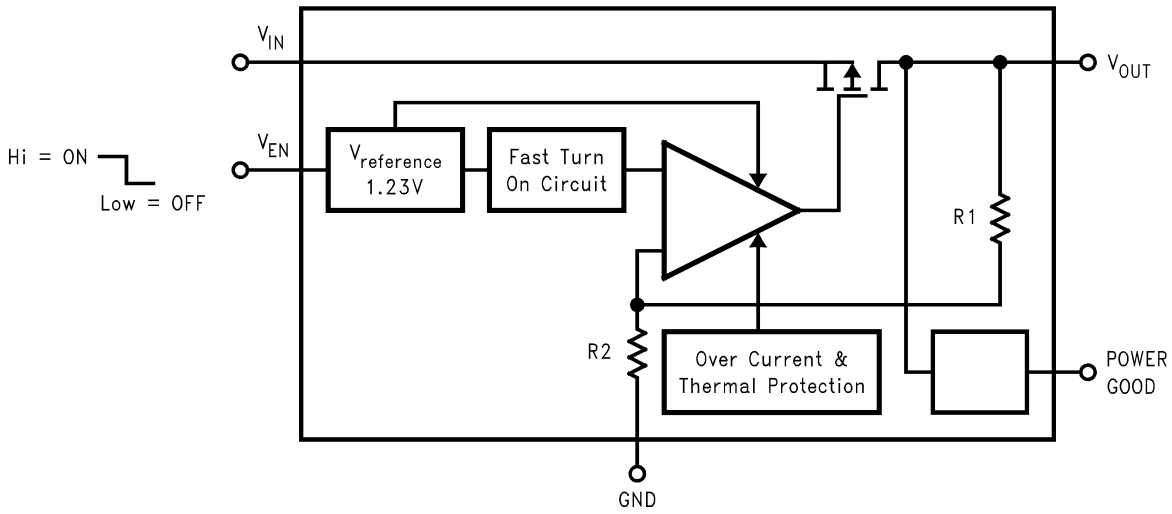
The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA, from a 2.5V to 6V input, consuming less than 1 µA in disable mode and has fast turn-on time less than 200 µs.

The LP3988 is available 5 pin SOT-23 package and 5-bump thin DSBGA package. Performance is specified for −40°C to +125°C temperature range and is available in 1.85, 2.5, 2.6, 2.85, 3.0 and 3.3V output voltages.



Note: Pin numbers in parentheses indicate DSBGA package pin out

Block Diagram



Pin Descriptions

Name	DSBGA	SOT-23	Function
V_{EN}	A1	3	Enable Input Logic, Enable High
GND	B2	2	Common Ground
V_{OUT}	C1	5	Output Voltage of the LDO
V_{IN}	C3	1	Input Voltage of the LDO
Power Good	A3	4	Power Good Flag (output): open-drain output, connected to an external pull-up resistor. Active low indicates an output voltage out of tolerance condition.

Connection Diagrams

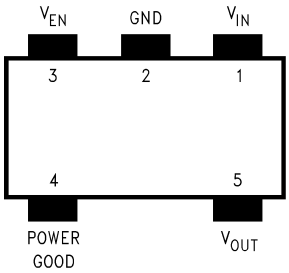


Figure 1. Top View
SOT-23-5 Package (DBV)
See Package Number DBV (R-PDSO-G5)

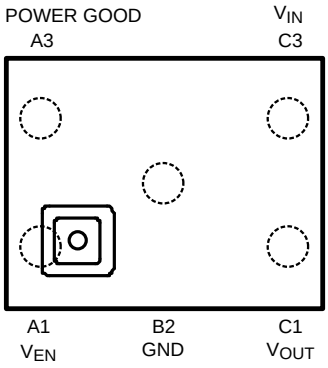


Figure 2. Top View
5 Bump DSBGA Package (YZR)
See Package Number YZR0005

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V_{IN}	−0.3 to 6.5V
V_{OUT}, V_{EN}, PowerGood (applies only to DSBGA)	−0.3V to (V_{IN}+0.3V), with 6V max
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Lead Temp, Pad Temp.	235°C
Power Dissipation (4) SOT-23-5 DSBGA	 364 mW 314 mW
ESD Rating (5)	
Human Body Model	2 kV
Machine Model SOT-23-5 DSBGA	 150V 200V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Recommended Operating Conditions do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/\theta_{JA}$where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364mW rating appearing under Absolute Maximum Ratings for the SOT-23-5 package results from substituting the Absolute Maximum junction temperature, 150°C, for T_J, 70°C for T_A, and 220°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C. Same principle applies to the DSBGA package.
(5) The human body model is 100 pF discharged through 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

RECOMMENDED OPERATING CONDITIONS (1) (2)

V_{IN} (3)	2.5V to 6V
V_{OUT}, V_{EN}	0 to V_{IN}
Junction Temperature	−40°C to +125°C
Junction-to-Ambient Thermal Resistance (θ_{JA}) SOT-23-5 DSBGA	 220ºC/W 255ºC/W
Maximum Power Dissipation (4) SOT-23-5 DSBGA	 250 mW 216 mW

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Recommended Operating Conditions do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) The minimum V_{IN} is dependant on the device output option.For $Vout_{(NOM)}$ < 2.5V, $V_{IN(MIN)}$ will equal 2.5V. For $Vout_{(NOM)}$ >= 2.5V, $V_{IN(MIN)}$ will equal $Vout_{(NOM)}$ + 200 mV.
(4) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250 mW rating appearing under Recommended Operating Conditions for the SOT-23-5 package results from substituting the maximum junction temperature for operation, 125°C, for T_J, 70°C for T_A, and 220°C/W for θ_{JA} into () above. More power can be dissipated at ambient temperatures below 70°C . Less power can be dissipated at ambient temperatures above 70°C. The maximum power dissipation for operation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C. Same principle applies to the DSBGA package.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{EN} = 1.8V, V_{IN} = V_{OUT} + 0.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	−20°C ≦ T_J ≦ 125°C, SOT-23-5 −40°C ≦ T_J ≦ 125°C, SOT-23-5		−2 **−3** **−3.5**	2 **3** **3.5**	% of $V_{OUT(nom)}$
		−40°C ≦ T_J ≦ 125°C, DSBGA		**-3**	**3**	
	Line Regulation Error	V_{IN} = $V_{OUT\ (NOM)}$ + 0.5V to 6.0V		−0.15 **−0.2**	0.15 **0.2**	%/V
	Load Regulation Error (3)	I_{OUT} = 1 mA to 150 mA			0.005 **0.007**	%/mA
PSRR	Power Supply Rejection Ratio	V_{IN} = $V_{OUT(nom)}$ + 1V, f = 1 kHz, I_{OUT} = 50 mA (Figure 5)	65			dB
		V_{IN} = $V_{OUT(nom)}$ + 1V, f = 10 kHz, I_{OUT} = 50 mA (Figure 5)	45			
I_Q	Quiescent Current	V_{EN} = 1.4V, I_{OUT} = 0 mA	85		120	µA
		V_{EN} = 1.4V, I_{OUT} = 0 to 150 mA	140		**200**	
		V_{EN} = 0.4V	0.003		**1.0**	
	Dropout Voltage (4)	I_{OUT} = 1 mA	1		**5**	mV
		I_{OUT} = 150 mA	80		115 **150**	
I_{SC}	Short Circuit Current Limit	(5)	600			mA
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1µF	220			µVrms
C_{OUT}	Output Capacitor	Capacitance (6)		**1**	**20**	µF
		ESR (6)		**5**	**500**	mΩ
TSD	Thermal Shutdown Temperature		160			°C
	Thermal Shutdown Hysteresis		20			°C
Enable Control Characteristics						
I_{EN}	Maximum Input Current at EN	V_{EN} = 0 and V_{IN} = 6.0V			**0.1**	µA
V_{IL}	Logic Low Input threshold	V_{IN} = 2.5V to 6.0V			**0.5**	V
V_{IH}	Logic High Input threshold	V_{IN} = 2.5V to 6.0V		**1.2**		V

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(5) Short circuit current is measured on input supply line after pulling down V_{OUT} to 95% $V_{OUT(nom)}$.
(6) Specified by design. Not production tested. The capacitor tolerance should be ±30% or better over the full temperature range. The full range of operating conditions such as temperature, DC bias and even capacitor case size for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitor types are recommended to meet the full device temperature range.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified: V_{EN} = 1.8V, V_{IN} = V_{OUT} + 0.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
Power Good						
V_{THL} V_{THH}	Power Good Low threshold High Threshold	% of V_{OUT} (PG ON) Figure 4 % of V_{OUT} (PG OFF) Figure 4 (7)	93 95	90 92	95 98	%
V_{OL}	PG Output Logic Low Voltage	$I_{PULL-UP}$ = 100µA, fault condition	0.02		**0.1**	V
I_{PGL}	PG Output Leakage Current	PG Off, V_{PG} = 6V	0.02			µA
T_{ON}	Power Good Turn On time, (8)	V_{IN} = 4.2V	10			µs
T_{OFF}	Power Good Turn Off time, (8)	V_{IN} = 4.2V	10			µs

(7) The low and high thresholds are generated together. Typically a 2.6% difference is seen between these thresholds.
(8) Turn-on time is measured between the enable input just exceeding VIH and the output voltage just reaching 95% of its nominal value.

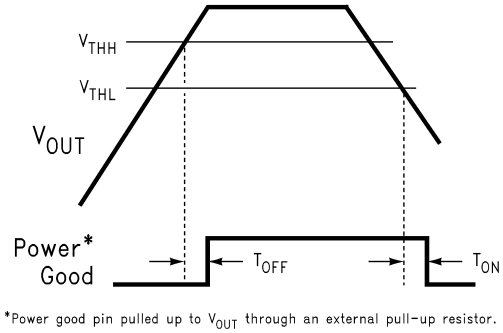


Figure 3. Power Good Flag Timing

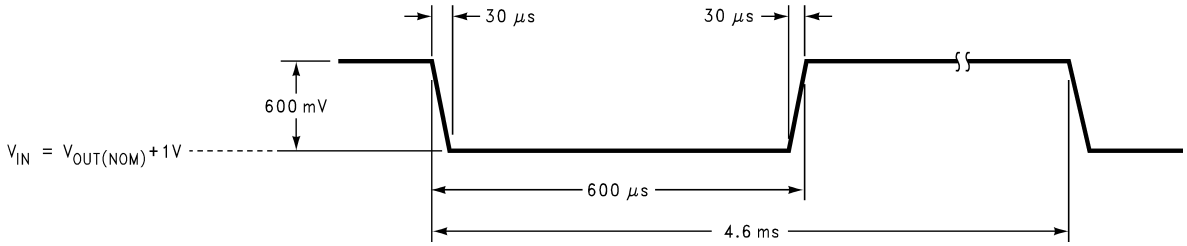


Figure 4. Line Transient response Input Perturbation

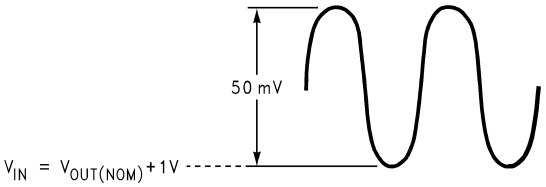


Figure 5. PSRR Input Perturbation

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT} + 0.2V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Ripple Rejection Ratio (LP3988-2.6)

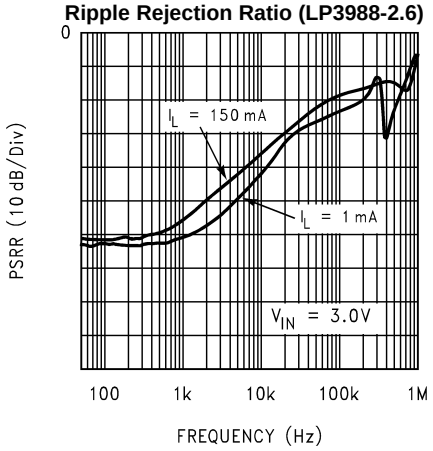


Figure 6.

Ripple Rejection Ratio (LM3988-2.6)

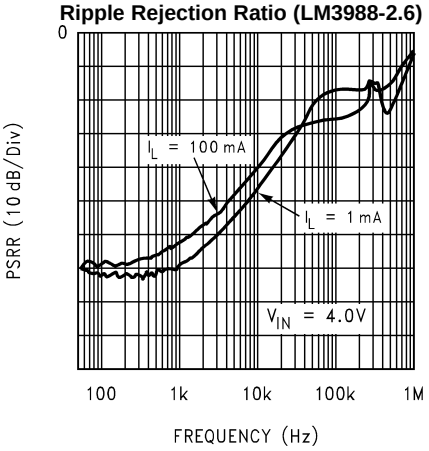


Figure 7.

Power-Good Response Time (LP3988-2.85) (flag pin pulled to V_{OUT} through a 100KΩ resistor)

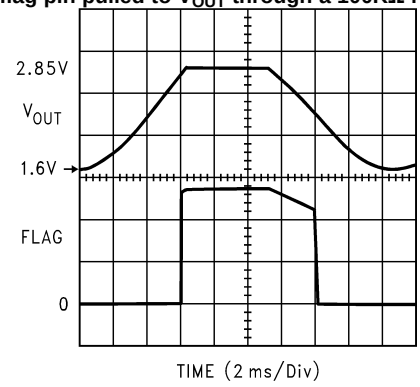


Figure 8.

Power-Good Response Time (LP3988-2.85) (flag pin pulled to V_{IN} through a 100KΩ resistor)

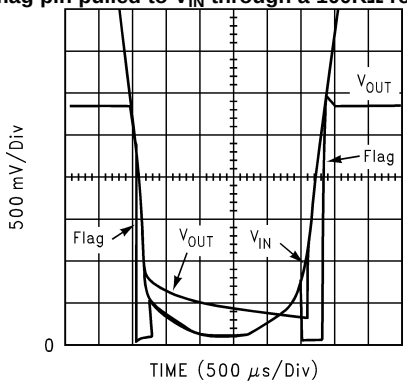


Figure 9.

Power-Good Response Time (LP3988-2.85) (flag pin pulled to V_{OUT} through a 100KΩ resistor)

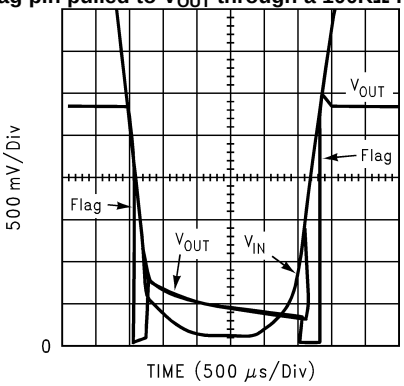


Figure 10.

Line Transient Response (LP3988-2.85)

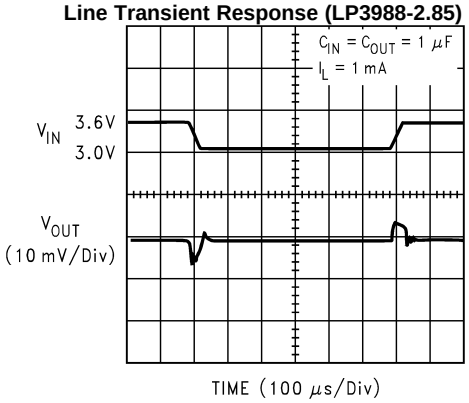


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT} + 0.2V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Line Transient Response (LP3988-2.85)

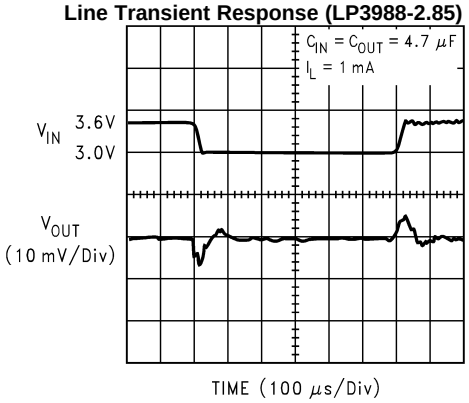


Figure 12.

Power-Up Response

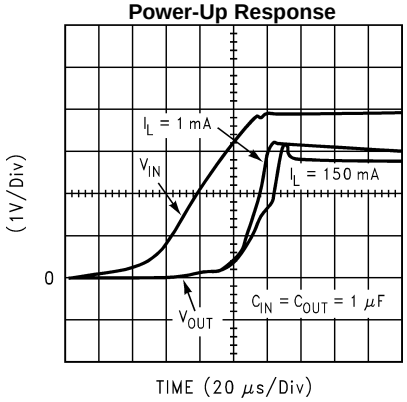


Figure 13.

Enable Response

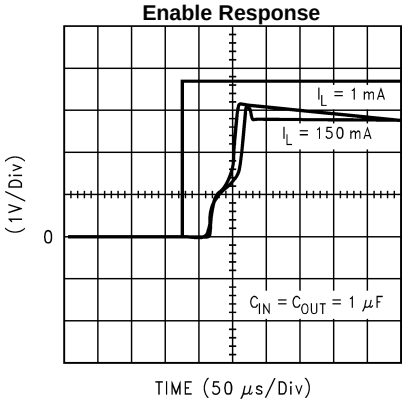


Figure 14.

Enable Response

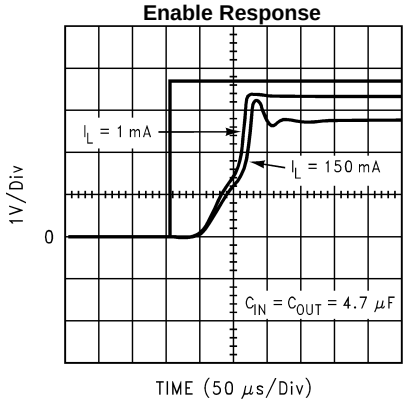


Figure 15.

Load Transient Response

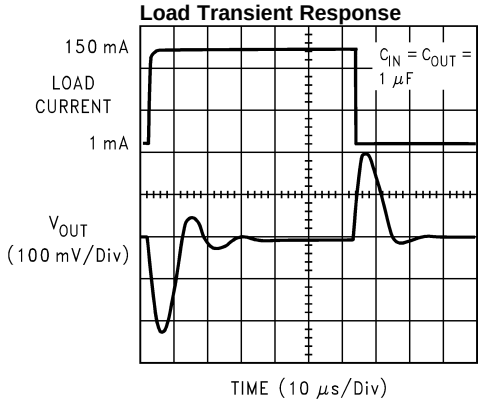


Figure 16.

Load Transient Response

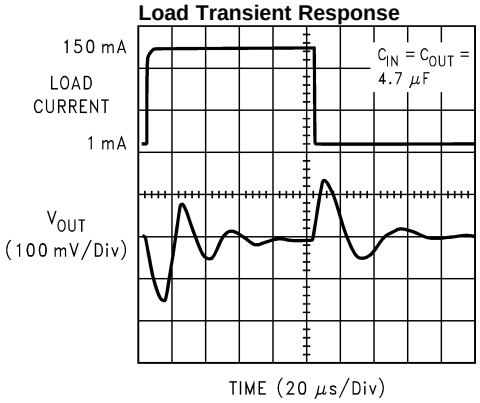


Figure 17.

APPLICATION INFORMATION

External Capacitors

Like any low-dropout regulator, the LP3988 requires external capacitors for regulator stability. The LP3988 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitance of ≅ 1 µF is required between the LP3988 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1 µF over the entire operating temperature range.

Output Capacitors

The LP3988 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 1 to 22 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3988 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 mΩ to 500 mΩ).

No-Load Stability

The LP3988 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

Capacitor Characteristics

The LP3988 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3988.

The ceramic capacitor's capacitance can vary with temperature. Most large value ceramic capacitors (≅ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

On/Off Input Operation

The LP3988 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Fast On-Time

The LP3988 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turn on time.

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3988IMF-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFSB	Samples
LP3988IMF-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFAB	Samples
LP3988IMF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LH5B	Samples
LP3988IMFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFSB	Samples
LP3988IMFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDLB	Samples
LP3988IMFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFAB	Samples
LP3988IMFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LH5B	Samples
LP3988ITL-1.85/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		8	Samples
LP3988ITL-2.6/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP3988ITL-2.85/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP3988ITLX-1.85/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		8	Samples
LP3988ITLX-2.6/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP3988ITLX-2.85/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LP3988 :

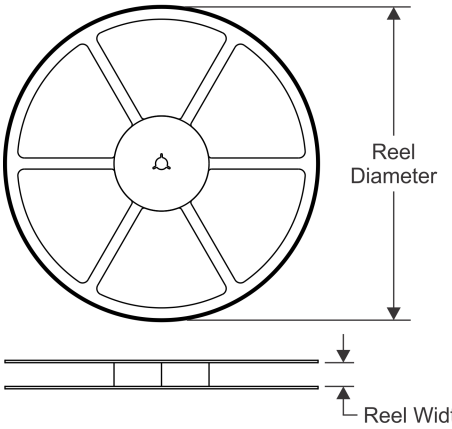
- Automotive: LP3988-Q1

NOTE: Qualified Version Definitions:

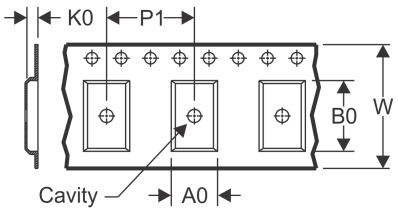
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

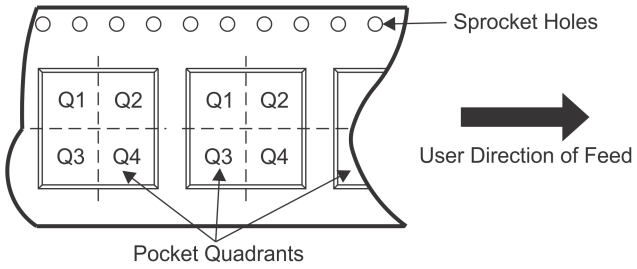


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

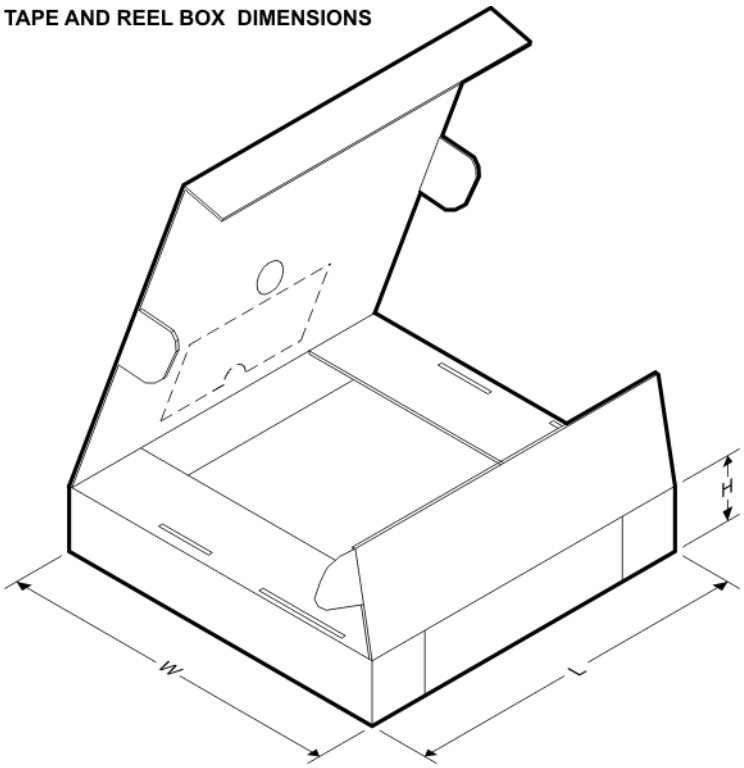
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3988IMF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMF-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988ITL-1.85/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3988ITL-2.6/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3988ITL-2.85/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3988ITLX-1.85/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3988ITLX-2.6/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3988ITLX-2.85/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

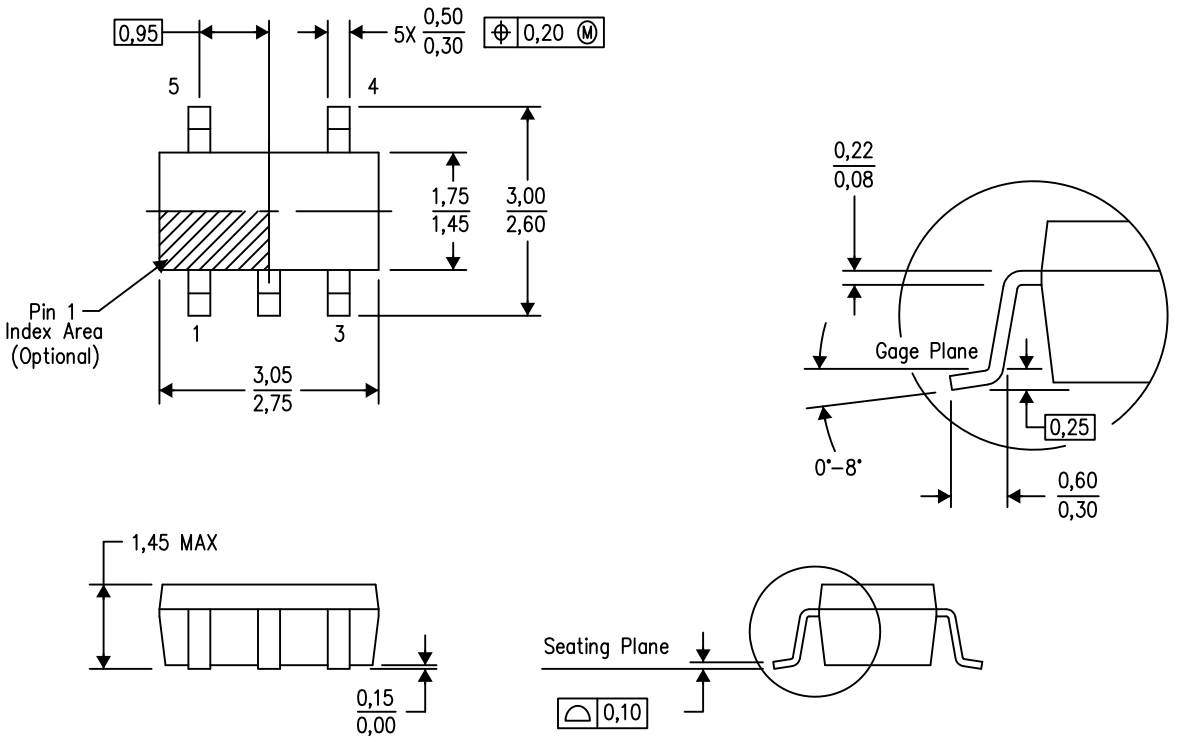
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3988IMF-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3988IMF-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3988IMF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3988IMFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3988IMFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3988IMFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3988IMFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3988ITL-1.85/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3988ITL-2.6/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3988ITL-2.85/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3988ITLX-1.85/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3988ITLX-2.6/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3988ITLX-2.85/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0

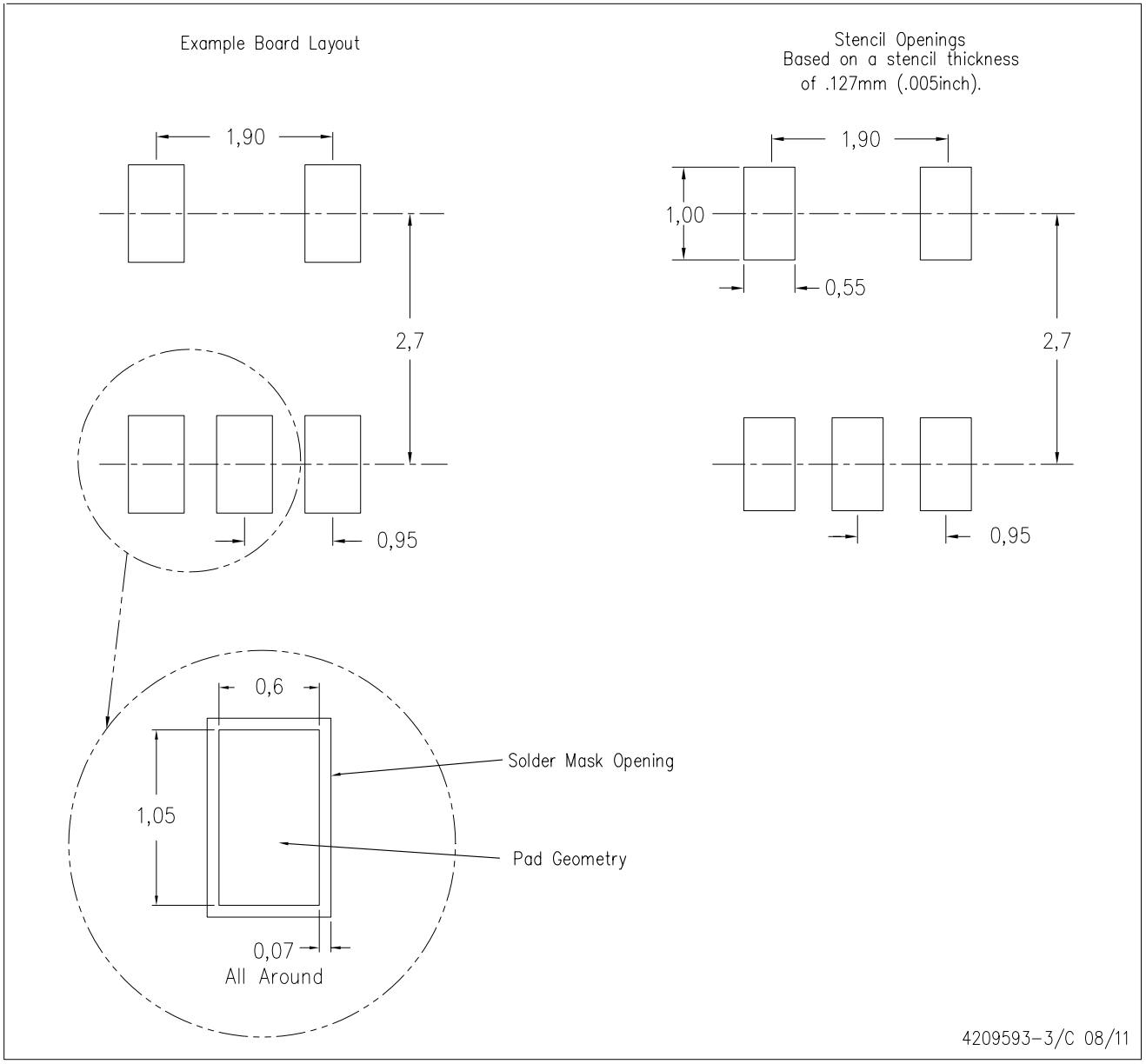
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

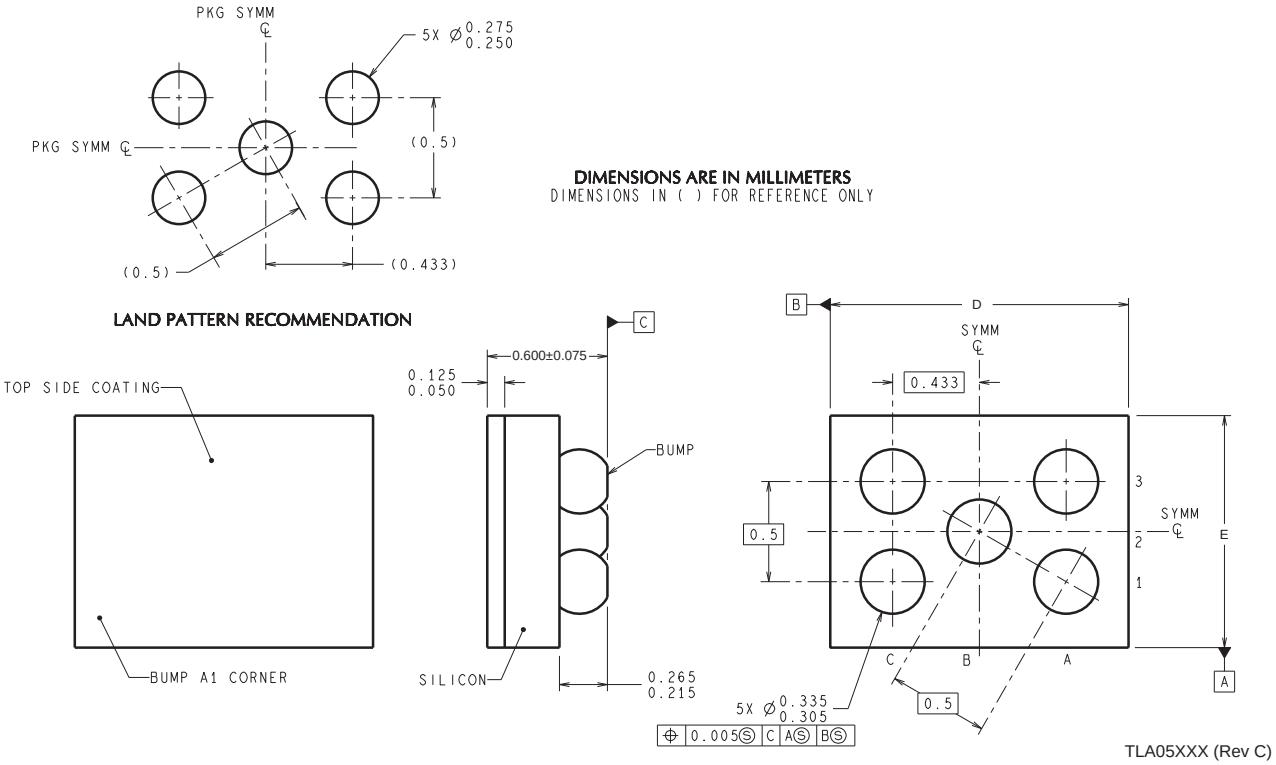
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZR0005



D: Max = 1.502 mm, Min =1.441 mm

E: Max = 1.045 mm, Min =0.984 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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