SPECIFICATION

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DEVICE SPECIFICATION for

TFT LCD Module

Model No.

LQ020B8UB02

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1. Application

This document is applied to LQ020B8UB02, SHARP's active matrix LCD(Liquid Crystal Display) module, which is suitable for mobile application, such as a cellular phone.

2. Overview

LQ020B8UB02 is composed of a glass panel, driving IC's, a backlight system with three LED(Light-Emitting Diode)'s, and a metal frame. A frame memory is embedded in one of the IC's, and no driving signal is required for still pictures. No LED driver is mounted. This panel is normally white.

The trans-reflective glass panel works sufficiently under whichever bright or dark circumstances. Reduced color mode allows lower power consumption by decreasing colors from 65,536 to eight. In addition, partial scanning is appropriate for a mobile phone. This is a manner of refreshing only limited lines as is illustrated below:

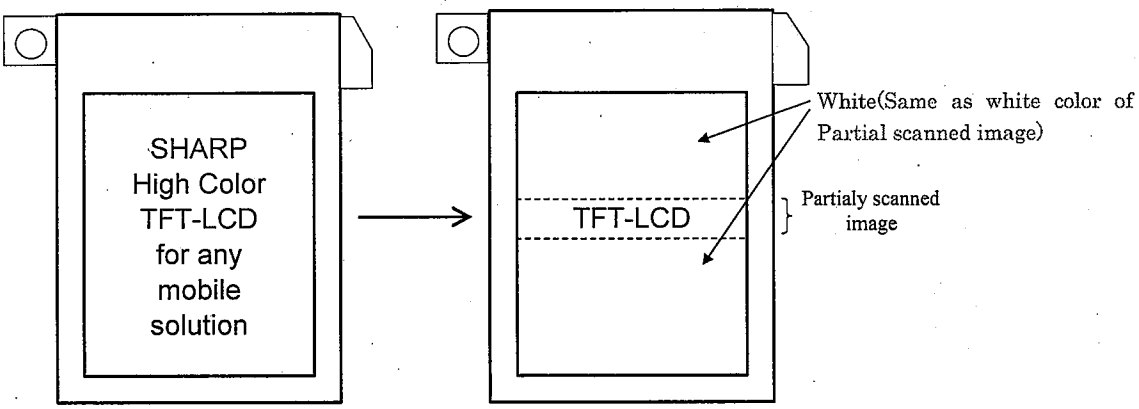


Fig. 1 Partial scanning

The diagonal size of the active area is 1.97 inches. The display panel performs 132 × RGB × 162 dot resolution and 65,536 color depth. Amorphous Silicon TFT(Thin Film Transistor) technology realizes faster response time, and it is fit for movies.

3. Mechanical Specifications

Table 1

Parameter	Specification	Unit	Remark
Screen size (diagonal)	5.01	cm	
	1.97	inch	
Active area size	31.68 (H) × 38.88 (V)	mm	
Pixel format	132 (H) ×162 (V) (1 pixel = R + G + B dots)	pixels	
Pixel pitch	0.24 (H) × 0.24 (V)	mm	
Pixel configuration	R, G, B vertical stripe		
Outline dimensions	39.1 (W) × 58.0 (H) × 3.4 (D)	mm	[Note 3-1]
Mass	12.5±0.5	g	
Surface treatment	Clear hard-coating 2H Anti-Reflection Diffuser=0%		
COG-ACF FPC-ACF	AC-8403(Hitachi Chemical) AC-7106(Hitachi Chemical)		

[Note 3-1] Protrusions and FPC(Flexible Printed Circuit) are excluded. For more detailed information, refer to Appendix A attached on the last page.

4. Input / Output Terminal

LCD-side connector: 55560-0201 (Molex)
Mating connector: 54722-0201(Molex)

Table 2

Pin No.	Symbol	I/O	Description	Remark
3	VDDI	Power supply	Power supply for digital circuits	
10	VDD	Power supply	Power supply for analog circuits	
11,12	GND	Ground		
20	RESX	Input	Reset signal (low active)	
19	CSX	Input	Chip select	
18	WRX	Input	Memory write enable (low active)	
17	RDX	Input	Memory read enable (low active)	
16	A0	Input	Address bit. Low level represents a command byte is currently on the MPU(Micro Processing Unit) bus, and high level shows a parameter byte.	
15	D0	Bi-directional	(LSB)	
14	D1	Bi-directional		
13	D2	Bi-directional		
8	D3	Bi-directional	8-bit MPU bus	
7	D4	Bi-directional	Command (A0 = low) or parameter (A0 = high)	
6	D5	Bi-directional		
5	D6	Bi-directional		
4	D7	Bi-directional	(MSB)	
9	PSD	Output	PSD signal	*1
2	VLED+	Power supply	LED power supply (anode)	
1	VLED–	Power supply	LED power supply (cathode)	

Also refer to Appendix A "Outline dimension" and Appendix B "Assignment of I/O Pin".

*1 PSD=H: Panel scanning timing, PSD=L: Panel non-scanning timing
PSD pin must be OPEN or Terminated when not use, since this pin is for output.

5. Absolute Maximum Ratings

Table 3

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage for digital	VDDI	–0.3	+2.2	V	
Supply voltage for analog	VDD	–0.3	+3.6	V	
Input voltage	V_I	–0.3	VDDI + 0.3	V	[Note 5-1]
Output voltage	V_O	–0.3	VDDI + 0.3	V	[Note 5-2]
Output voltage	V_O	–0.3	VDD + 0.3	V	[Note 5-3]
Storage temperature	T_{stg}	–40	+85	°C	[Note 5-4]
Operating temperature	T_{opa}	–30	+70	°C	
LED input current	I_{LED}	0	30	mA	[Note 5-5]
LED power dissipation	P_{LED}	—	120	mW	[Note 5-5]

[Note 5-1] Applied to RESX, WRX, RDX, A0, D0 through D7

[Note 5-2] Applied to D0 through D7

[Note 5-3] Applied to PSD

[Note 5-4] Humidity: 95% RH max. at Ta (ambient temperature) ≤ 40°C.
Wet-bulb temperature is 39°C or less at Ta > 40°C.
No condensation.

[Note 5-5] Per one LED. Ta=25℃
Please refer to the below graph in the case of Ta>25℃

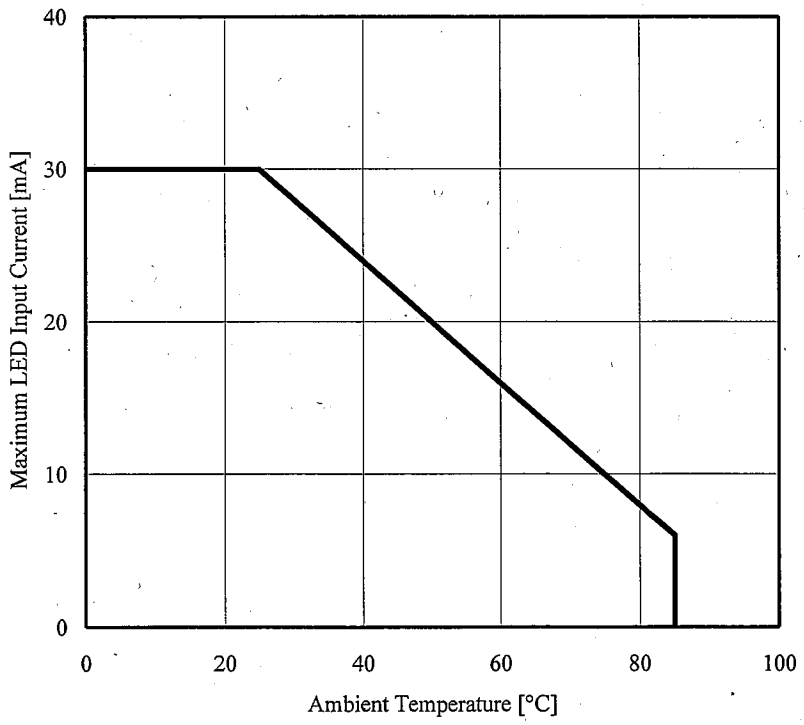


Fig. 2 The derating curve of LED

6. Electrical Characteristics

6-1. Recommended operating conditions

Table 4 Ta = -30~70°C

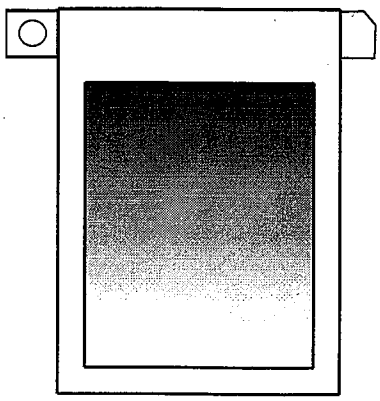
Parameter	Min.	Typ.	Max.	Unit	Remark
Power Supply VDDI					
Supply voltage	1.65	1.8	1.95	V	[Note 6-1]
Current consumption (Active mode)	—	0.35	0.55	mA	[Note 6-2]
Current consumption (Still mode)	—	0.14	0.23	mA	[Note 6-2]
Current consumption (Partial mode)	—	0.07	0.12	mA	[Note 6-2]
Power Supply VDD					
Supply voltage	2.6	2.78	2.9	V	[Note 6-1]
Current consumption (Active mode)	—	1.8	2.8	mA	[Note 6-2]
Current consumption (Still mode)	—	0.6	0.91	mA	[Note 6-2]
Current consumption (Partial mode)	—	0.23	0.40	mA	[Note 6-2]
Digital signals					
Input voltage(Low)	0	—	0.3×VDDI	V	[Note 6-3]
Input voltage(High)	0.7×VDDI	—	VDDI	V	[Note 6-3]
Output voltage(Low)	0	—	0.2×VDDI	V	[Note 6-4]
Output voltage(High)	0.8×VDDI	—	VDDI	V	[Note 6-4]
Output voltage(Low)	0	—	0.4	V	[Note 6-5]
Output voltage(High)	VDD-0.4	—	VDD	V	[Note 6-5]
Leakage current	–10	—	10	μA	[Note 6-3]

[Note 6-1] Transient characteristics
Reset sequence, or power on process: Refer to Power On Sequence (9-1-1.Initial configuration)
[Note 6-2] The operating modes:

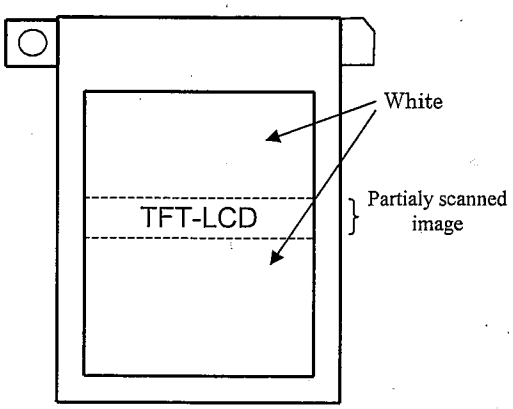
Operating mode	Number of colors	MPU Access Frame rate	Partial scanning	Panel scan rate	LED
Active mode(Mode1)	65,536	15 frames / sec	Full screen	49Hz	ON or OFF
Still mode(Mode2)	65,536	5 frames / sec	Full screen	12Hz	OFF
Partial mode(Mode3)	8	5 frames / sec	40 lines	6Hz	OFF

Current situations are shown below. (Panel scan rate is a rough estimation.)

Active/Still mode : 32-gray-bar



Partial mode : Black "TFT-LCD" in white background



[Note 6-3] Applied to RESX, WRX, RDX, A0, and D0 through D7
[Note 6-4] Applied to D0 through D7
[Note 6-5] Applied to PSD

6-2. Backlight driving

Table 5 Ta=25℃

Parameter	Min.	Typ.	Max.	Unit	Remark
LED supply voltage		—	12.0	V	
LED forward current		15	20	mA	[Note 6-6]

[Note 6-6] Per one LED.

LED:NSCW215T(NICHIA CORPORATION)

Luminous Intensity : Rank S

Color Ranks : b3,b5

6-3. AC Characteristics

* The upper and lower threshold levels are 70% and 30% of VDDI voltage, respectively.

Table 6 Specify at I/O Connector, Ta=-30～70°C

Parameter	Description	Min.	Max.	Unit	Remark
Chip select CSX					
t_{AWC8}	Address setup time	0	—	ns	
t_{AHC8}	Address hold time	0	—	ns	
Address A0					
t_{AW8}	Address setup time	10	—	ns	
t_{AH8}	Address hold time	10	—	ns	
Write to LCD					
t_{CYC}	Write cycle	330	—	ns	
t_{CCLW}	Control pulse low duration	50	—	ns	
t_{CCHW}	Control pulse high duration	280	—	ns	
t_{DS8}	Data setup time	50	—	ns	
t_{DH8}	Data hold time	10	—	ns	
Read from LCD					
t_{CYC2}	Read cycle	450	—	ns	
t_{CCLR}	Control pulse low duration	140	—	ns	
t_{CCHR}	Control pulse high duration	300	—	ns	
t_{ACC8}	Read access time	—	140	ns	Load = 100pF
t_{OH8}	Output disable time	10	50	ns	Load = 100pF
Transient timings					
t_r	Rising time	—	10	ns	
t_f	Falling time	—	10	ns	
Reset timings					
t_{RW1}	Negative pulse width	20	—	μs	[Note 6-7]
t_{RW2}	Negative pulse width	—	2	μs	[Note 6-8]
t_{RT}	Initializing time	—	1000	μs	

PSD timings					Load = 10pF
t_{PSW}	PSD pulse width	8.0	12.5	ms	Mode1,2
t_{PSW}	PSD pulse widt	2.5	3.9	ms	Mode3(40Line)
t_{FPS}	Front poach of Panel scan	190	300	µs	Mode1,2,3
t_{BPS}	Back poach of Panel scan	190	300	µs	Mode1,2
t_{BPS}	Back poach of Panel scan	420	650	µs	Mode3

[Note 6-7] Reset Time t_{RW1} can assure a certain reset action.

[Note 6-8] Reset Time t_{RW2} can assure NO reset action.

[Note 6-9] In the case of Reset Time(t_{RW}) is 2us~20us, reset action is not assured.

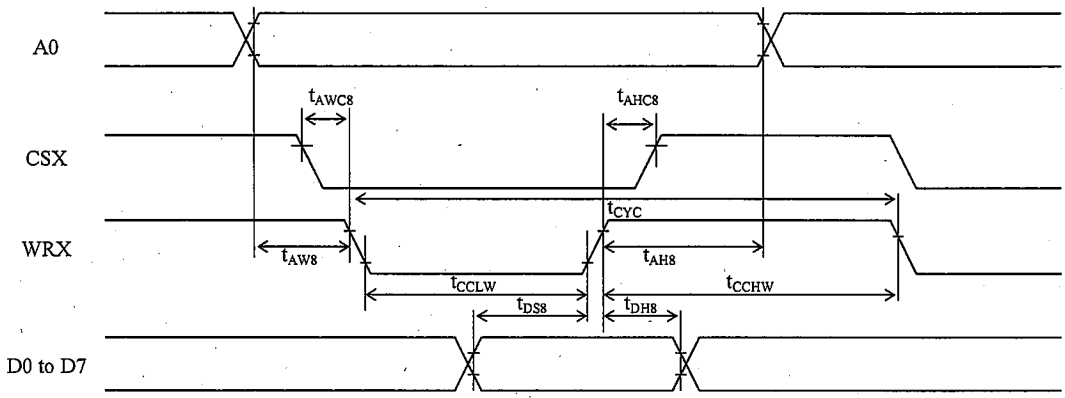


Fig. 3 MPU Bus timing (Writing a command or parameter to LCD)

※ When the function of CSX is not employed, CSX has to be connected with GND.

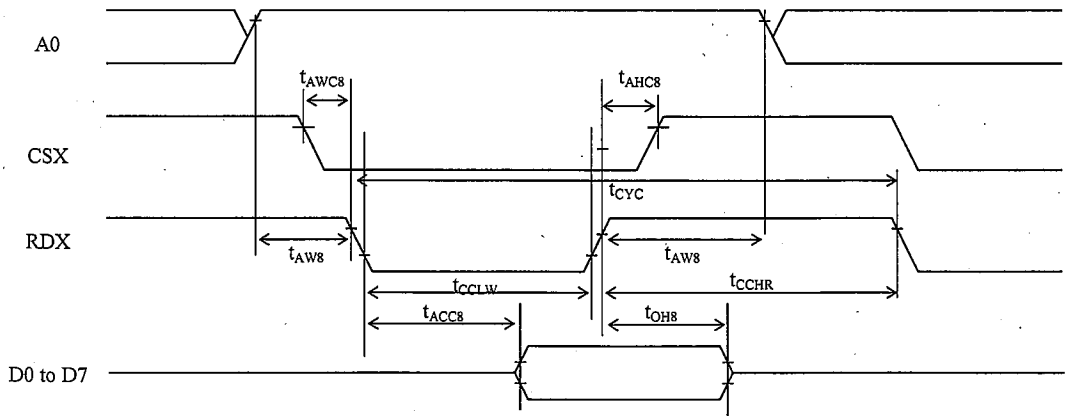


Fig.4 MPU Bus timing (Reading a parameter from LCD)

※ When the function of CSX is not employed, CSX has to be connected with GND.

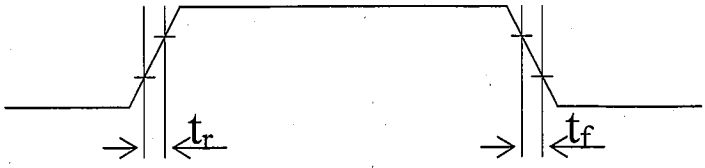


Fig.5 The regulations of transient timing

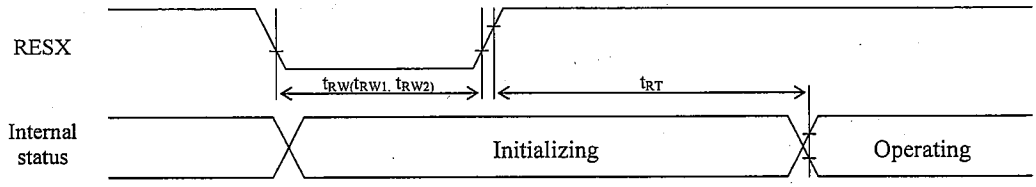


Fig. 6 The regulations of reset timing

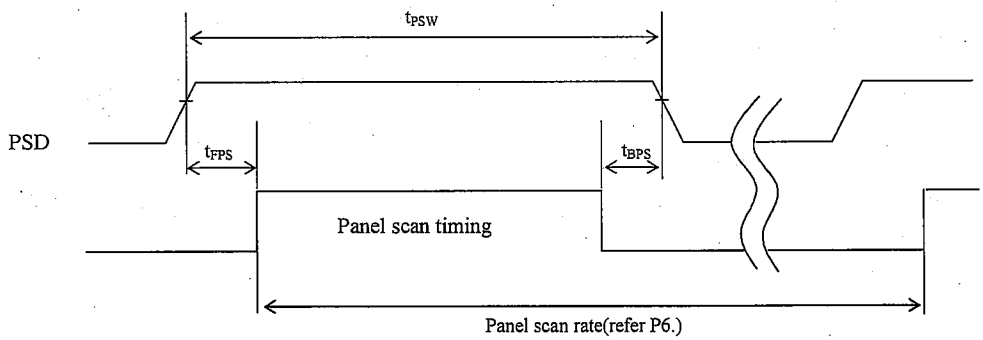


Fig. 7 The regulations of PSD timing

PSD is the signal to be produced corresponding to the writing timing from the driver to LCD panel. Tearing effect can be prevented by accessing MPU (Write RAM) during PSD Low period.(1 period)

7. MPU Bus Protocol

7-1. Summary of memory addressing

The control IC on the glass panel has a video memory, or a frame buffer, which contains an image to display. In advance of memory access, you have to initialize two kinds of address registers that represent diagonal coordinates of the rectangular region whose contents you are want to update or refer to.

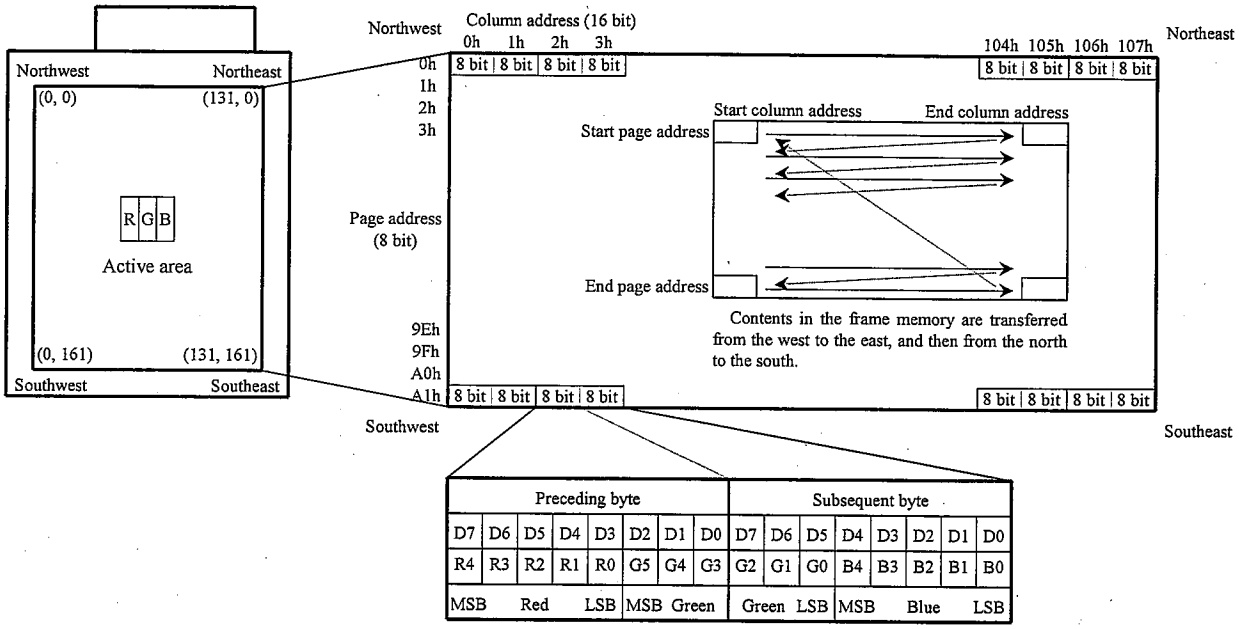


Fig. 8 Memory map

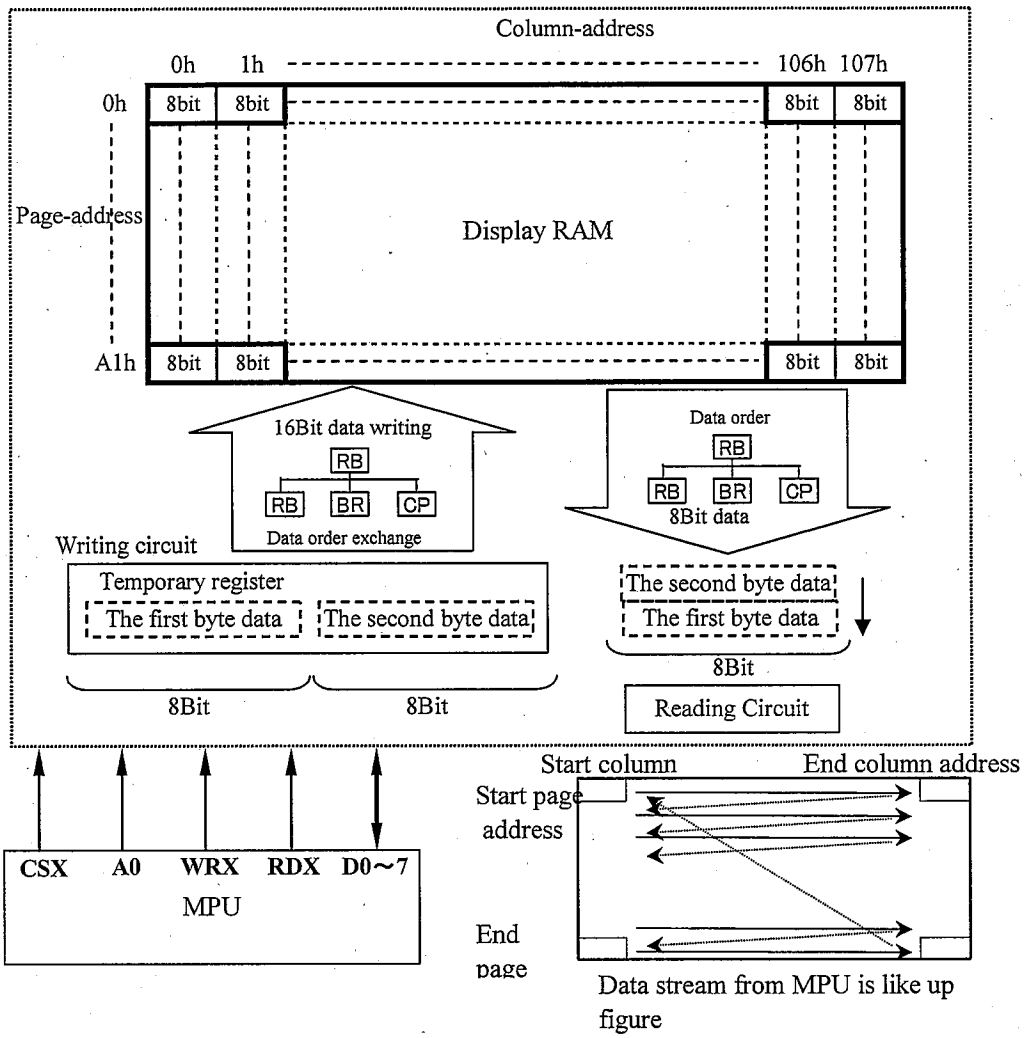
For efficient memory access, the IC also has an internal pointer that addresses what pixel you are to access next. At every memory access the pointer is automatically updated as following: at first the pixel pointed by the pointer transfers from the left to the right, and then memory access is performed downward. When the whole image access has been done completely, the pointer returns to the start page and column address.

You can find the relationship between the active area and the memory map in the figure above. It also tells the format of color code. Take care of the byte order and the least significant bits; three sub-pixel formats are available. The letter "h" means hexadecimal notation.

Though it is possible to write video data of each pixel from MPU by using 3 pixel format modes, those data are mapped only by RB mode in the frame memory, which is shown Fig. 8.

7-2. Display RAM

132×(8+8)×162 bits bit-mapped display memory is incorporated. The display memory organization is 2112 bits ((8+8)×132) for column address,162 bits for page address. This enables 132×162 bits display with 65536 colors(32×64×32).



Because the data of 16 bit is necessary for the writing of display data for 1 pixel, the data writing for 1 pixel is completed by 2 bytes of the MPU access. The writing data is stored in the temporary register to correspond with the RGB data structure (3 kinds, Pixel Format command) of display data sent from MPU, and the data order is exchanged when the second data is accessed from MPU, then display RAM is written.

Therefore be sure to make data writing by 2 bytes of data unit. The data writing is finished with 1 byte of data, the data writing to RAM is not assured. When the display RAM is read, the address designated by column address and page address is read at the unit of 8 bits.

Data is read out by a byte, one by one, when it is read from RAM, and the data sequence is in accordance with the setting of Pixel format.

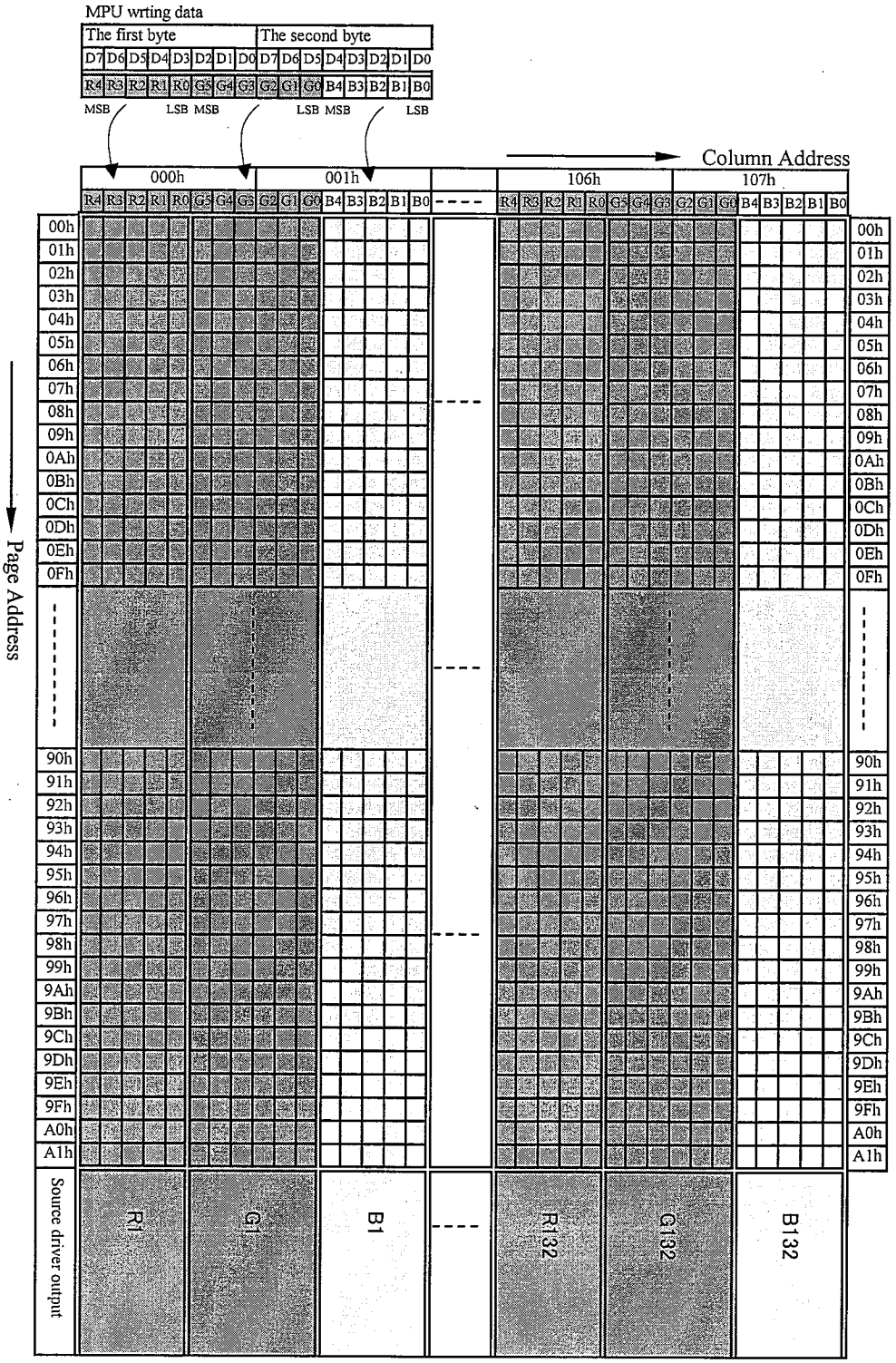
Column address and page address are incremented by address control register automatically. The increment is done every display RAM reading or writing from MPU.

Because address set outside of effective address area in each access mode is prohibited, do not make address set outside of the area.

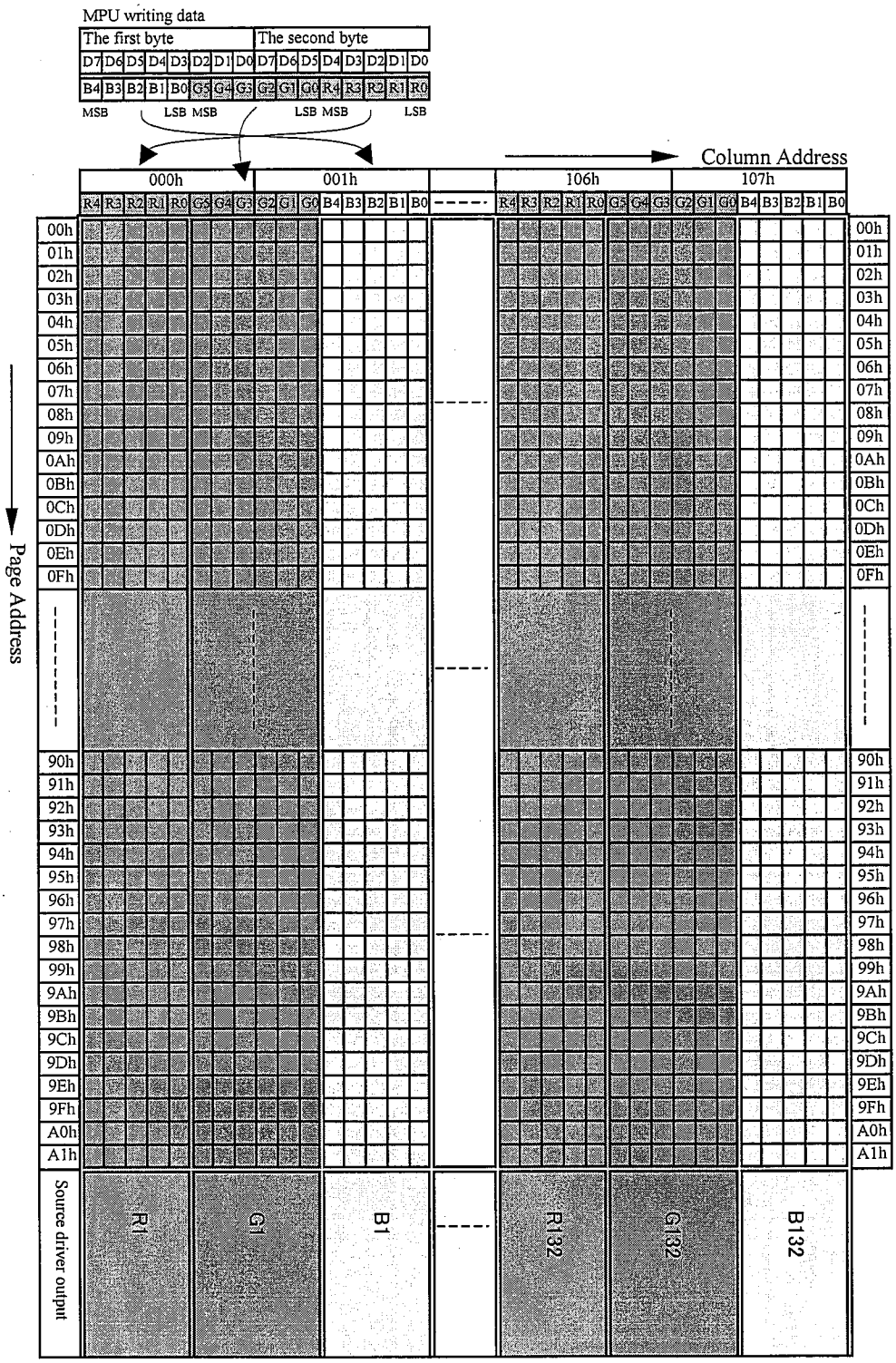
7-3. The relation between Display RAM and Address

3 pixel format modes are available. Those displayed data are mapped only by one mode in Display RAM.

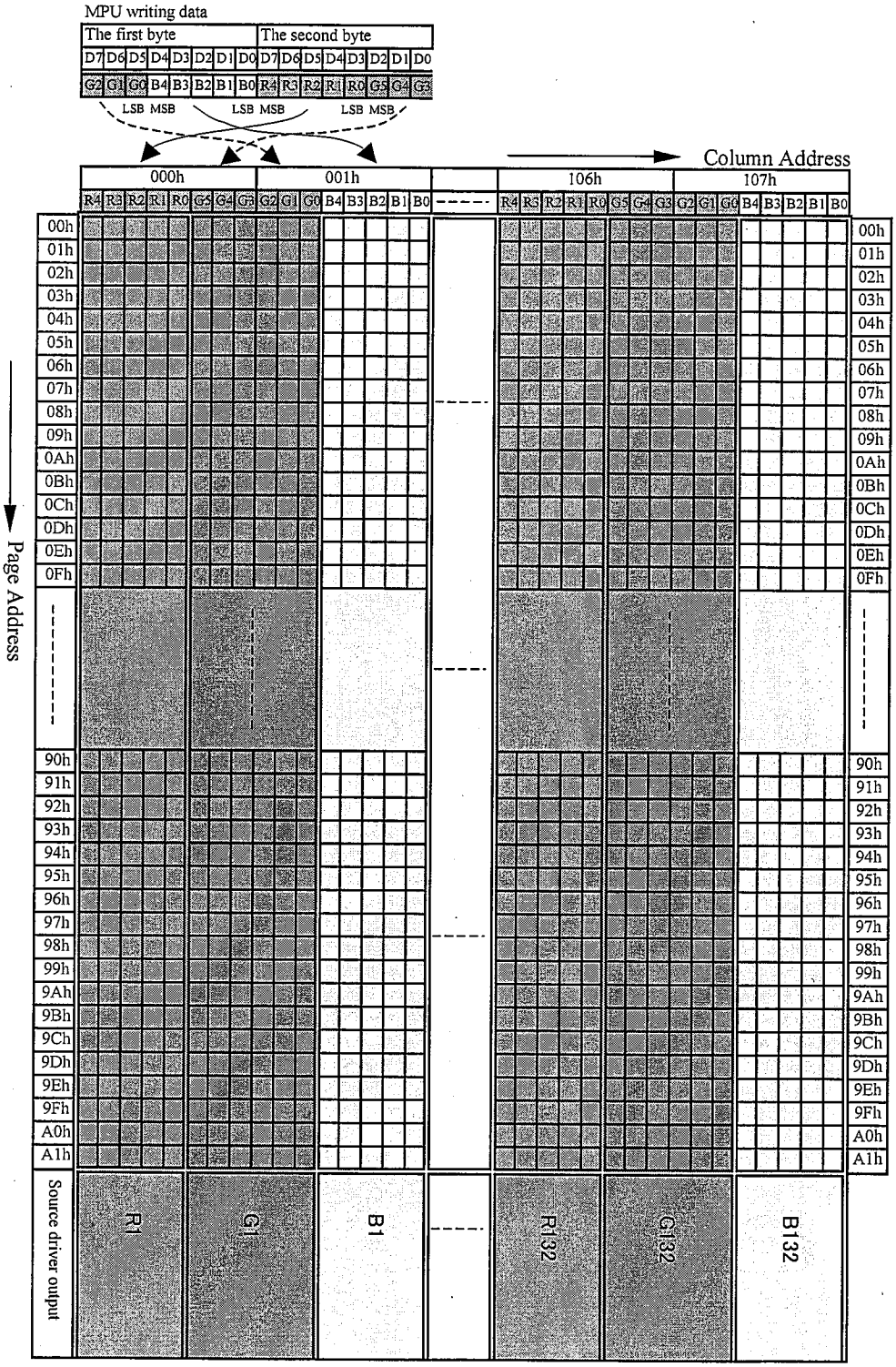
(1) Displayed Data : RB mode



(2) Displayed Data : BR mode



(3) Displayed Data : CP mode



7-4. Significance of Data bit

The significance of each signals is shown below. The signals of the same column have the same significance. Then MSB(Most Significant Bit) are R4, G5, and B4 , and LSB(Least Significant Bit) are R0, G0, and B0.

Significance	More ⟷ Less					
R	R4	R3	R2	R1	R0	
G	G5	G4	G3	G2	G1	G0
B	B4	B3	B2	B1	B0	

Table 8

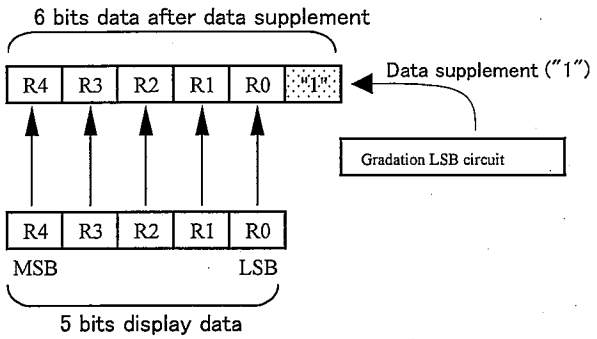
		R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
Primary colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
	Cyan	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Blue gradation	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
	↓	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	Brighter	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Red gradation	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	↑	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↓	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	Brighter	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Green gradation	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	↑	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	↓	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0
	Brighter	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0

7-5. Gradation LSB control

At the time of display with gradation, green has 64-level gradation by adjacent 6 bits data, and Red and Blue have 32-level gradation by adjacent 5 bits data.

Red and Blue selects 32-level gradation out of 64-level gradation by using the 5 bits written in the corresponding RAM area and the 1 bit supplemented by the gradation LSB circuit.

The gradation LSB circuit always supplement "1" as the data of LSB.

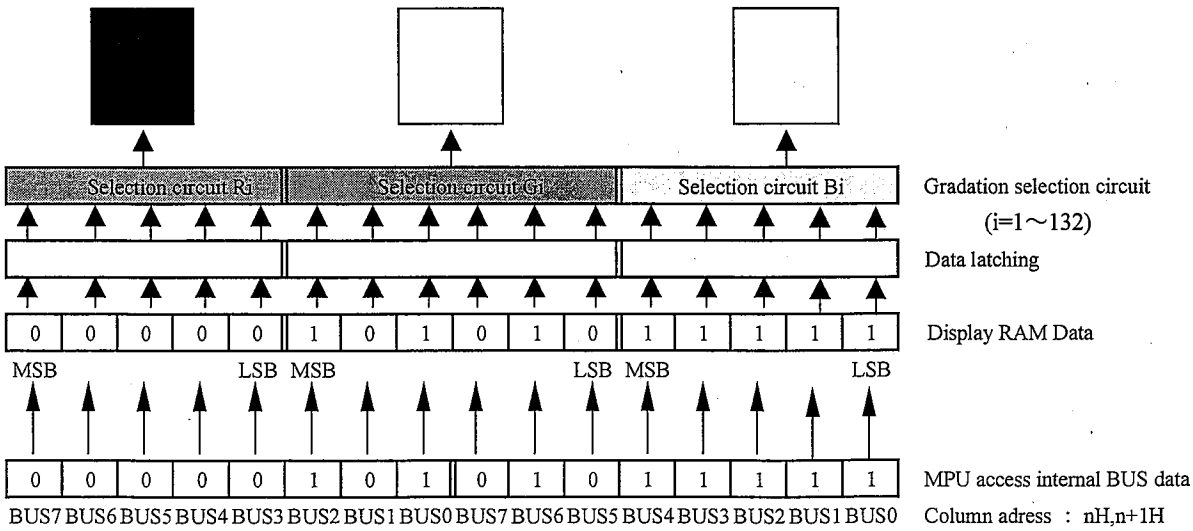


Gradation LSB circuit

7-6. Low Power 8 color mode

The setting of CNUM="1" makes 8 color mode by Low Power Enable. Because the gradation levels used in this mode are highest gradation and lowest gradation, and circuits to make other gradation are stopped, the power consumption is lowered.

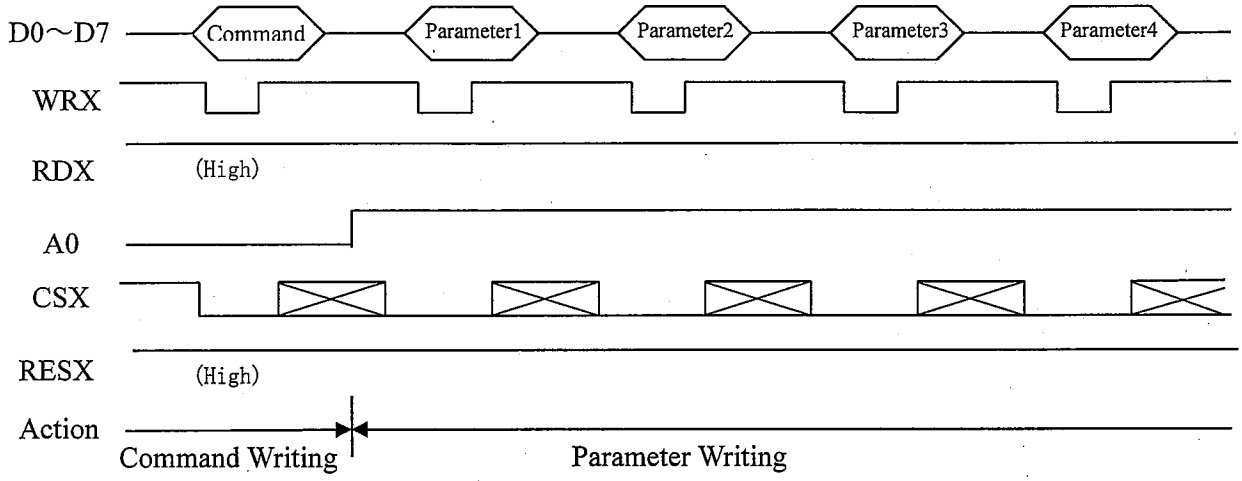
According to the value of MSB, the highest gradation (White) is displayed in case of "1", and the lowest gradation(Black) is displayed in case of "0".



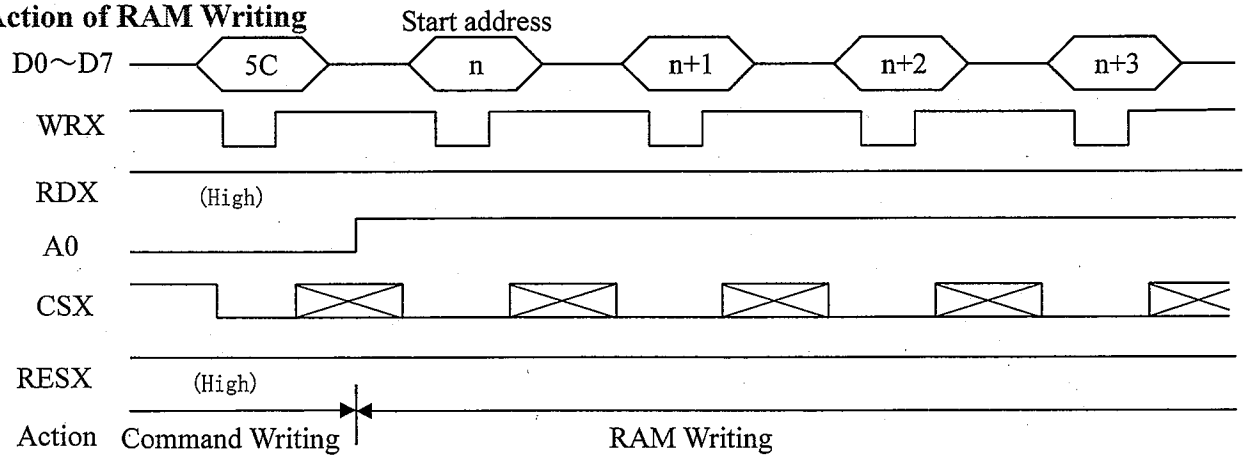
7-7. Access to Register and Display RAM

Access to register and display RAM can be done by CSX, A0, WRX, RDX, and D0~D7. When CSX is "L", the register and RAM becomes accessible. A0 indicates whether D0~D7 is command or parameter.

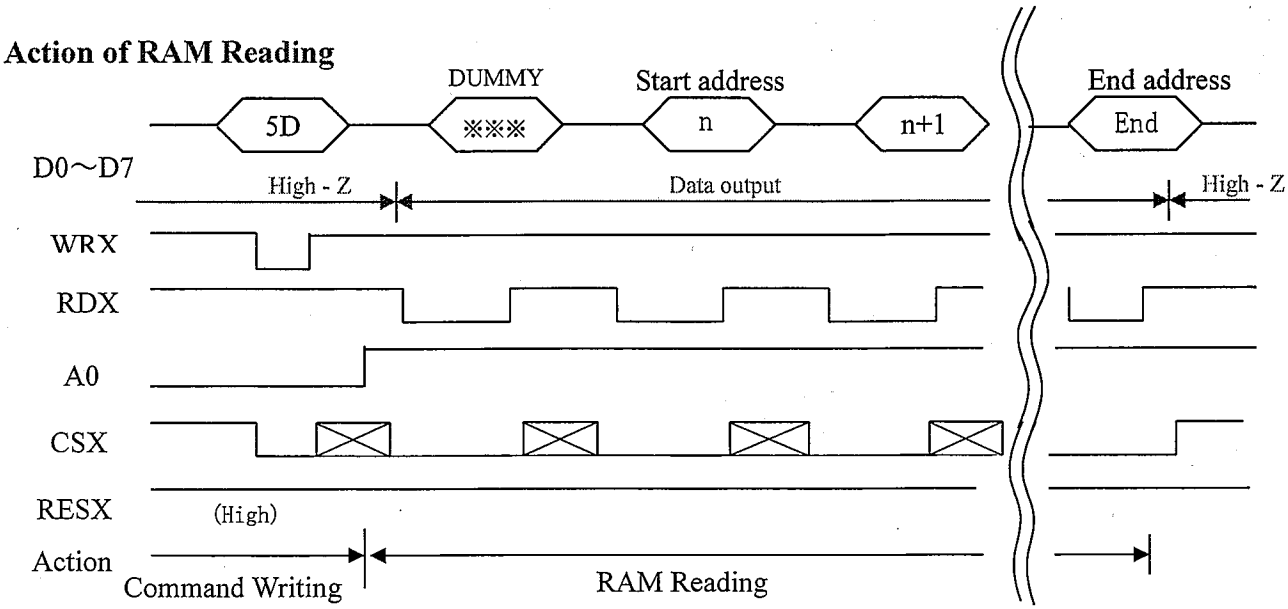
Action of Writing



Action of RAM Writing



Action of RAM Reading



8. Available commands

Table 7

Command (*)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	(†)	Description
Column Address	15	0	0	0	1	0	1	0	1	4	Set column address pointer
Page Address	75	0	1	1	1	0	1	0	1	2	Set page address pointer
Pixel Format	C8	1	1	0	0	1	0	0	0	1	Select byte order and sub-pixel format.
Write RAM	5C	0	1	0	1	1	1	0	0	(‡)	Write image data to the memory
Read RAM	5D	0	1	0	1	1	1	0	1	(‡)	Read image data from the memory
Display Normal	A6	1	0	1	0	0	1	1	0	0	Display positive image
Display Inverted	A7	1	0	1	0	0	1	1	1	0	Display negative image, or complementary colors
Sleep Disable	94	1	0	0	1	0	1	0	0	0	Get out of sleep mode and start scanning
Sleep Enable	95	1	0	0	1	0	1	0	1	0	Get into sleep mode and stop scanning
Low Power Enable	A8	1	0	1	0	1	0	0	0	3	Get into standby mode
Low Power Disable	A9	1	0	1	0	1	0	0	1	0	Get out of standby mode
Display Off	AE	1	0	1	0	1	1	1	0	0	Display a blank screen with no regard to the memory contents.
Display On	AF	1	0	1	0	1	1	1	1	0	Display the current memory contents.
Volume Control	C6	1	1	0	0	0	1	1	0	1	Adjust embedded electrical volume
Timing Control	CA	1	1	0	0	1	0	1	0	7(#)	Adjust to drive the glass panel
Non Operation	25	0	0	1	0	0	1	0	1	0	Non Operation
Read ID1	DA	1	1	0	1	1	0	1	0	0	Read ID Code 1
Read ID2	DB	1	1	0	1	1	0	1	1	0	Read ID Code 2
Reserved	00	0	0	0	0	0	0	0	0		Ignored
Reserved	AA	1	0	1	0	1	0	1	0		Ignored
Reserved	AB	1	0	1	0	1	0	1	1		Ignored
Reserved	BC	1	0	1	1	1	1	0	0		Ignored
Reserved	CB	1	1	0	0	1	0	1	1		Ignored
Reserved	E0	1	1	1	0	0	0	0	0		Ignored
Reserved	EE	1	1	1	0	1	1	1	0		Ignored

(*) Undefined instructions are inhibited.

(†) Number of following parameters

(‡) Depending upon the image size

(#) "1" at Internal Register Read mode

Command need to be executed in the condition of chip select (CSX="L").

Note that there are commands which have plural parameters and be sure to access to all parameters even in case of no update of parameters. Command set which is finished without access to all parameters is not assured, and may cause display error. In this case, the display can be back to normal by sending Commands and all parameters again.

Command code which is not specified is prohibited, but prohibited commands have no effect on the LCD module.

8-1. Column Address

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
15	0	0	0	0	1	0	1	0	1	Command byte
	1	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	Start column address (lower byte)
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	CS8	Start column address (upper byte)
	1	CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0	End column address (lower byte)
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	CE8	End column address (upper byte)

(Reset: {CS8～CS0} = 000H, {CE8～CE0} = 107H)
The Greek letter ' ϕ ' in the following table means "don't care".

Start address and end address in the column direction of display RAM is set. Data is set separately with upper 1 bit and lower 8 bits.

The possible value to use for CE8～CE0 of end address is 000H～107H, and 108H～1FFH is prohibited to use.

Also, the value of CE8～CE0 of end address need to be set with larger address than that of CS8 ～CS0 of start address, and smaller address is prohibited. When these prohibited settings are executed, the LCD module shows display error, but the display can be back to normal by sending Commands and correct parameters.

Since 1 pixel represents 2 bytes, Start column address can designate an even numbered address only, while, End column address can designate an odd numbered address only.

Access to display RAM is addressed by setting start and end addresses of column and page addresses.

Internal column address counter is incremented by +2 address automatically when 1 byte of data is written in display RAM. Page address is incremented by +1 address and column address is preset in column start address, in case of incrementing +2 address after reaching to end column address.

Page address is preset in page start address, in case of incrementing +1 address after reaching to end page address.

Namely, internal column address counter and internal page address counter are preset to start up position, after reaching to end column and end page addresses and incrementing each address.

8-2. Page Address

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
75	0	0	1	1	1	0	1	0	1	Command byte
	1	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Start page address
	1	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	End page address

(Reset: {PS7～PS0} = 00H, {PE7～PE0} = A1H)

Start address and end address in the page direction of display RAM is set.

The possible value to use for PS7～PS0 of start address is 00H～A1H, and A2H～FFH is prohibited to use.

The possible value to use for PE7～PE0 of end address is 00H～A1H, and A2H～FFH is prohibited to use.

The LCD module shows display error when any prohibited setting is executed, but the display can be back to normal by sending Commands and correct parameters.

8-3. Pixel Format

You can make a choice out of three color-codings, or sub-pixel formats. It is necessary to mention that the memory map is fixed and *unchangeable*. This command has no influence on the memory map, but takes effect only on the RGB format on the interface bus.

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
C8	0	1	1	0	0	1	0	0	0	Command byte
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	P1	P0	Sub-pixel format

			Preceding byte								Subsequent byte							
P1	P0	Description	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	RB mode	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
0	1	BR mode	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0
1	0	CP mode	G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3
1	1	RB mode	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

For R and B there are no signals have the same significance as that of G0, which are supplemented by an internal circuit and fed into the glass panel. Needless to say, if you have inverted MSB and LSB, the expected images would not appear.

8-4. Write RAM

This instruction makes transfer of image data from MPU to LCD. By this command, internal column address counter and page address counter is preset to start address. Take notice that you can choose a sub-pixel format favorable for your application. Refer to Pixel Format Command for detail.

RB mode

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
5C	0	0	1	0	1	1	1	0	0	Command byte
	1	R4	R3	R2	R1	R0	G5	G4	G3	Color code for the 1st pixel
	1	G2	G1	G0	B4	B3	B2	B1	B0	
	1	R4	R3	R2	R1	R0	G5	G4	G3	Color code for the 2nd pixel
	1	G2	G1	G0	B4	B3	B2	B1	B0	
	1	R4	R3	R2	R1	R0	G5	G4	G3	Color code for the 3rd pixel
	1	G2	G1	G0	B4	B3	B2	B1	B0	
	1									Similarly

BR mode

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
5C	0	0	1	0	1	1	1	0	0	Command byte
	1	B4	B3	B2	B1	B0	G5	G4	G3	Color code for the 1st pixel
	1	G2	G1	G0	R4	R3	R2	R1	R0	
	1	B4	B3	B2	B1	B0	G5	G4	G3	Color code for the 2nd pixel
	1	G2	G1	G0	R4	R3	R2	R1	R0	
	1	B4	B3	B2	B1	B0	G5	G4	G3	Color code for the 3rd pixel
	1	G2	G1	G0	R4	R3	R2	R1	R0	
	1									Similarly

CP mode

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
5C	0	0	1	0	1	1	1	0	0	Command byte
	1	G2	G1	G0	B4	B3	B2	B1	B0	Color code for the 1st pixel
	1	R4	R3	R2	R1	R0	G5	G4	G3	
	1	G2	G1	G0	B4	B3	B2	B1	B0	Color code for the 2nd pixel
	1	R4	R3	R2	R1	R0	G5	G4	G3	
	1	G2	G1	G0	B4	B3	B2	B1	B0	Color code for the 3rd pixel
	1	R4	R3	R2	R1	R0	G5	G4	G3	
	1									Similarly

8-5. Read RAM

This instruction makes transfer of image data from LCD to MPU. By this command, internal column address counter and page address counter is preset to start address.

Read RAM command supports three pixel formats shown below table.

There is a dummy data between command and data.

RB mode

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
5D	0	0	1	0	1	1	1	0	1	Command byte
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Read dummy data
	1	R4	R3	R2	R1	R0	G5	G4	G3	Color code for the 1st pixel
	1	G2	G1	G0	B4	B3	B2	B1	B0	
	1	R4	R3	R2	R1	R0	G5	G4	G3	Color code for the 2nd pixel
	1	G2	G1	G0	B4	B3	B2	B1	B0	
	1	R4	R3	R2	R1	R0	G5	G4	G3	Color code for the 3rd pixel
	1	G2	G1	G0	B4	B3	B2	B1	B0	
	1									Similarly

BR mode

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
5D	0	0	1	0	1	1	1	0	1	Command byte
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Read dummy data
	1	B4	B3	B2	B1	B0	G5	G4	G3	Color code for the 1st pixel
	1	G2	G1	G0	R4	R3	R2	R1	R0	
	1	B4	B3	B2	B1	B0	G5	G4	G3	Color code for the 2nd pixel
	1	G2	G1	G0	R4	R3	R2	R1	R0	
	1	B4	B3	B2	B1	B0	G5	G4	G3	Color code for the 3rd pixel
	1	G2	G1	G0	R4	R3	R2	R1	R0	
	1									Similarly

CP mode

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
5D	0	0	1	0	1	1	1	0	1	Command byte
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Read dummy data
	1	G2	G1	G0	B4	B3	B2	B1	B0	Color code for the 1st pixel
	1	R4	R3	R2	R1	R0	G5	G4	G3	
	1	G2	G1	G0	B4	B3	B2	B1	B0	Color code for the 2nd pixel
	1	R4	R3	R2	R1	R0	G5	G4	G3	
	1	G2	G1	G0	B4	B3	B2	B1	B0	Color code for the 3rd pixel
	1	R4	R3	R2	R1	R0	G5	G4	G3	
	1									Similarly

Note: The " ϕ " mark means "don't care".

8-6. Display Normal

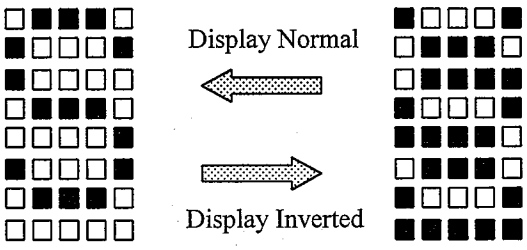
Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
A6	0	1	0	1	0	0	1	1	0	Command byte

Display Normal command is used to display the data of display RAM stored at that time in all display area normally. There is no effect to the stored data of display RAM by execution of this command.

8-7. Display Inverted

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
A7	0	1	0	1	0	0	1	1	1	Command byte

Display Inverted command is used to have inverted display image. There is no effect to the stored data of display RAM by execution of this command. In case of setting at Partial display mode by Low power Enable command, the display image of designated partial area is inverted. The inverted display image is back to original display image by sending Display Normal command.



8-8. Sleep Disable

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
94	0	1	0	0	1	0	1	0	0	Command byte

This is the command to disable sleep mode. After sending this command, display gets out of sleep mode and system becomes ready.

8-9. Sleep Enable

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
95	0	1	0	0	1	0	1	0	1	Command byte

This is the command to enable sleep mode. In sleep mode, display becomes off and operation is stopped in high voltage area. After reset is made, the mode becomes sleep enable.

In sleep mode,

- the data of display RAM is kept.
- the status of operation mode before the execution of power save command is kept.

Although the control to display control and power supply IC is made after the completion of Power OFF sequence, the value of internal register is kept and initialization is not done. Command is acceptable.

8-10. Low Power Enable

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
A8	0	1	0	1	0	1	0	0	0	Command byte
	1	LPS7	LPS6	LPS5	LPS4	LPS3	LPS2	LPS1	LPS0	Start page address to scan from
	1	LPE7	LPE6	LPE5	LPE4	LPE3	LPE2	LPE1	LPE0	End page address to scan up to
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	CNUM	The number of colors.

(Reset: {LPS7～LPS0} = 00H, {LPE7～LPE0} = A1H, {CNUM} = 0H)

ϕ mark is "Don't care"

Low Power Enable command is used to set low power consumption mode. Timing Control (Mode3) にする際には必ず Low Power Enable(CNUM=1)を実行下さい。

Low power consumption is achieved by decrease of number of color, and partial display whose effective display area (effective number of lines) is limited. This command consists of 3 kinds of parameter bytes.

The first parameter tells the page address to scan from, and the second tells the one to scan up to. The LSB of the third parameter byte 'CNUM' shows the number of colors. D1～D7 bit is ignored due to Don't care.

CNUM="0": 65536 color mode
CNUM="1": 8 color mode

Normally, the range of "first parameter < second parameter" should be utilized.

In case that there is no choice but utilizing the range of "first parameter > second parameter", the display data of 162nd should be written by white data. (So, the display of 162nd line will be white.)

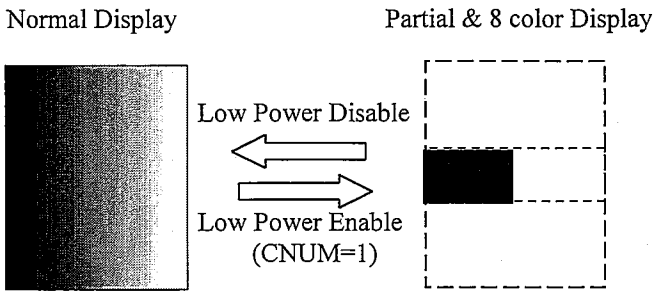
The range of LPS, LPE is limited within 00h～A1h. In case of designating A2h～FFh to LPS, LPE, failure display is come up, but it will be back to normal by resending a correct value, or sending Low Power Disable.

8-11. Low Power Disable

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
A9	0	1	0	1	0	1	0	0	1	Command byte

Low Power Disable command is used to return to normal display mode from low power mode.

When Low Power Disable command is executed, display has picture in all display area with full color (65536 color).



8-12. Display Off

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
AE	0	1	0	1	0	1	1	1	0	Command byte

Display Off command is used to have blank display regardless of data stored in display RAM.

8-13. Display On

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
AF	0	1	0	1	0	1	1	1	1	Command byte

Display On command is used to have display according to data stored in display RAM.

8-14. Volume Control

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
C6	0	1	1	0	0	0	1	1	0	Command byte
	1	CSEL	VC6	VC5	VC4	VC3	VC2	VC1	VC0	Parameter1

Volume Control command is used to adjust embedded electrical volume.
Because it is adjusted by embedded ROM normally, do not use this command at normal case.

8-15. Timing Control

Timing Control sets some conditions for panel driving. The setting of register value of Timing Control parameters have each operational mode shifted, and have optimum adjusted value stored in EEPROM reflected to driver. (Because each register value is optimized after making sample, please have the design at system side in which register value can be set at random in each mode.) Since initial value of Timing Control command cannot operate LCD correctly, be sure to send Timing Control command before Display ON command.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	1	0	1	0	Command byte
1	0	ER_ADD1	ER_ADD0	ER_WR	ER_RD	EROM	AUTO_AMP	P_TYPE	1st parameter
1	0	0	0	0	H_GG	FRAME2	FRAME1	FRAME0	2nd parameter
1	0	0	0	0	LS_STST1	LS_STST0	T_COM1	T_COM0	3rd parameter
1	0	DN_DLY	UP_DLY2	UP_DLY1	UP_DLY0	PMOD	PDM1	PDM0	4th parameter
1	VBLANK4	VBLANK3	VBLANK2	VBLANK1	VBLANK0	VSCAN1	VSCAN0	VBLKE	5th parameter
1	G_PULS	ECK1	ECK0	BLK_COM2	BLK_COM1	BLK_COM0	REV_FRA	REV_TYPE	6th parameter
1	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	7th parameter

8-15-1. Timing Control parameters

1st parameter Register

LCD Module Internal Registers P_TYPE , AUTO_AMP

	AUTO_AMP	P_TYPE
Provisional value	0	0

EEPROM Access Register EROM, ER_RD, ER_WR, ER_ADD0, ER_ADD1

This LCD module stores optimum adjusted value of reference voltage applied for LC in EEPROM, and the optimized value for the reference voltage stored in EEPROM can be read and called up by these registers.

Be sure to call up the value stored in EEPROM at the time of power-on or rest without fail.

EROM	Access EEPROM	notes
0	OFF	
1	ON	

ER_WR	ER_RD	Access EEPROM Mode (EROM="0":void)	notes
0	0	No Access	
0	1	Read From EEPROM & Reflect electronic Volume	
1	0	Write to EEPROM	Don't use
1	1	Write Protect	Don't use

ER_ADD1	ER_ADD0	EEPROM Access Address	notes
0	0	Address 0	For MODE1
0	1	Address 1	For MODE2
1	0	Address 2	For MODE3
1	1	Address 3	Reserve

MODE1: Active Full Display Mode MODE2: Still Full Display Mode MODE3: Partial Display 8 colors

2nd parameter Register

LCD Module Internal Registers FRAME[2,0], H_GG

	H_GG	FRAME2	FRAME1	FRAME0
Provisional value	0	0	1	1

3rd parameter Register

LCD Module Internal Registers LS_STST[1:0] T_COM[1:0]

	LS_STST1	LS_STST0	T_COM1	T_COM0
Provisional Value	0	0	0	0

4th parameter Register

LCD Module Internal Registers DN_DLY ,UP_DLY[2:0] ,PMOD ,PDM[1:0]

	DN_DLY	UP_DLY2	UP_DLY1	UP_DLY0	PMOD	PDM1	PDM0
Provisional value	0	0	0	1	1	0	1

5th parameter Register

ULC Mode Control Register VBLANK[4:0],VSCAN[1:0],VBLAK

These registers are used to decide ON or OFF of panel ULC mode, and ratio between scan frame and blank frame at ULC mode.

Provisional value

	VBLANK4	VBLANK3	VBLANK2	VBLANK1	VBLANK0	VSCAN1	VSCAN0	VBLKE
MODE1	0	0	0	0	0	0	1	1
MODE2	0	0	1	1	0	0	1	1
MODE3	1	0	0	0	0	0	1	1

MODE1: Active Full Display Mode MODE2: Still Full Display Mode MODE3: Partial Display 8 colors

6th parameter Register

LCD Module Internal Registers G_PULS ,ECK[1:0],BLK_COM[2:0],REV_FRA,REV_TYPE

	G_PULS	ECK1	ECK0	BLK_COM2	BLK_COM1	BLK_COM0	REV_FRA	REV_TYPE
Provisional value	0	0	1	0	1	0	0	0

By using G_PULS=1, display quality at low temperature condition can be upgraded, but power consumption is slightly increased.

7th parameter Register

LCD Driver TEST Registers TST[7:0]

	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0
Value	0	0	0	0	0	0	0	0

8-15-2. Timing Control parameters Sheet

Timing Control Parameters decide the following each register.

Because there is the possibility that each register value may change depending on each mode, please pay attention to this when you design your system.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	1	0	1	0	Command byte
1	0	ER_ADD1	ER_ADD0	ER_WR	ER_RD	EROM	AUTO_AMP	P_TYPE	1st parameter
1	0	0	0	0	H_GG	FRAME2	FRAME1	FRAME0	2nd parameter
1	0	0	0	0	LS_STST1	LS_STST0	T_COM1	T_COM0	3rd parameter
1	0	DN_DLY	UP_DLY2	UP_DLY1	UP_DLY0	PMOD	PDM1	PDM0	4th parameter
1	VBLANK4	VBLANK3	VBLANK2	VBLANK1	VBLANK0	VSCAN1	VSCAN0	VBLKE	5th parameter
1	G_PULS	ECK1	ECK0	BLK_COM2	BLK_COM1	BLK_COM0	REV_FRA	REV_TYPE	6th parameter
1	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	7th parameter

Parameters for Active Full Display Mode (MODE1)

(MODE1:LED ON or OFF) **(Panel scan rate=49Hz)** **Provisional value**

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	1	0	1	0	Command byte
1	0	0	0	0	1	1	0	0	1st parameter
1	0	0	0	0	0	0	1	1	2nd parameter
1	0	0	0	0	0	0	0	0	3rd parameter
1	0	0	0	0	1	1	0	1	4th parameter
1	0	0	0	0	0	0	1	1	5th parameter
1	0	0	1	0	1	0	0	0	6th parameter
1	0	0	0	0	0	0	0	0	7th parameter

Parameters for Still Full Display Mode (MODE2)

(MODE2:LED OFF use only) **(Panel scan rate=12Hz)** **Provisional value**

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	1	0	1	0	Command byte
1	0	0	1	0	1	1	0	0	1st parameter
1	0	0	0	0	0	0	1	1	2nd parameter
1	0	0	0	0	0	0	0	0	3rd parameter
1	0	0	0	0	1	1	0	1	4th parameter
1	0	0	1	1	0	0	1	1	5th parameter
1	0	0	1	0	1	0	0	0	6th parameter
1	0	0	0	0	0	0	0	0	7th parameter

Parameters for Partial Display 8 colors Mode (MODE3)

(MODE3:LED OFF use only) **(Panel scan rate=6Hz)** **Provisional value**

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	1	0	1	0	Command byte
1	0	1	0	0	1	1	0	0	1st parameter
1	0	0	0	0	0	0	1	1	2nd parameter
1	0	0	0	0	0	0	0	0	3rd parameter
1	0	0	0	0	1	1	0	1	4th parameter
1	1	0	0	0	0	0	1	1	5th parameter
1	0	0	1	0	1	0	0	0	6th parameter
1	0	0	0	0	0	0	0	0	7th parameter

(Panel scan rate is a rough estimation.)

8-16. Non Operation

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
25	0	0	0	1	0	0	1	0	1	Command byte

8-17. Initial status

Initialization is done when RESX terminal has "L" level. Normally initialization is done with MPU by connecting RESX terminal with MPU reset terminal.

Be sure to make operation for reset at the time of power-on.

Table 9

Item	Description
Memory contents	Indefinite
Column start address	0000h
Column end address	0107h
Page start address	00h
Page end address	A1h
Pixel format	RB mode
Color depth	65536
Sleep mode	Enable
Low power mode	Disable
Display	Off
Display mode	Normal

8-18. Internal Register Read

It is possible to read out the contents of internal register by setting 1 bit of 1st parameter in Display Timing Command to be REGRDEN.

In case of setting register read allowed, only 1st parameter should be set, not executing the setting of parameters onwards.

At this mode (register read allowed), other register bit existing in 1st parameter (ER_ADD1, ER_ADD0, ER_WR, ER_RD, EROM, AUTO_AMP, P_TYPE) should be set to the same code as that of 1st parameter in Display Timing Control, which is set at Display mode.

· Setting register read allowed

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	1	0	1	0	Command byte
1	REGRDEN	ER_ADD1	ER_ADD0	ER_WR	ER_RD	EROM	AUTO_AMP	P_TYPE	1st parameter

REGRDEN = 0 : Register read Not Allowed
REGRDEN = 1 : Register read Allowed
(Reset : REGRDEN = 0)

After setting register read allowed, internal register read is executed by the following commands.

"FF" Code Write → Internal read address Set → Register Read

Internal read address is allotted to 01H～1FH, from which, a preferred address can be selected.

• Setting and Read-out of register read address

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
FF	0	1	1	1	1	1	1	1	1	Command byte
	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	1st parameter(Read address)
	1	Read Data								RDX=0,WRX=1

Read Address	Read Data								Command (Write)
	D7	D6	D5	D4	D3	D2	D1	D0	Hex
01H	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	15
02H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	CS8	
03H	CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0	
04H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	CE8	
05H	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	75
06H	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	
07H	LPS7	LPS6	LPS5	LPS4	LPS3	LPS2	LPS1	LPS0	A8
08H	LPE7	LPE6	LPE5	LPE4	LPE3	LPE2	LPE1	LPE0	
09H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	CNUM	
0AH	ϕ	VCL6	VCL5	VCL4	VCL3	VCL2	VCL1	VCL0	C6
0BH	ϕ	VCW6	VCW5	VCW4	VCW3	VCW2	VCW1	VCW0	
0CH	ϕ	ER_ADD1	ER_ADD0	ER_WR	ER_RD	EROM	AUTO_AMP	P_TYPE	CA
0DH	ϕ	ϕ	ϕ	ϕ	H_GG	FRAME2	FRAME1	FRAME0	
0EH	ϕ	ϕ	ϕ	ϕ	LS_STST1	LS_STST0	T_COM1	T_COM0	
0FH	ϕ	DN_DLY	UP_DLY2	UP_DLY1	UP_DLY0	PMOD	PDM1	PDM0	
10H	VBLANK4	VBLANK3	VBLANK2	VBLANK1	VBLANK0	VSCAN1	VSCAN0	VBLKE	
11H	G_PULS	ECK1	ECK0	BLK_COM2	BLK_COM1	BLK_COM0	REV_FRA	REV_TYPE	
12H	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	
13H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	P1	P0	C8
1FH	ϕ	ϕ	ϕ	ϕ	ON/OFF	LPOW	SLEEP	REV	Command

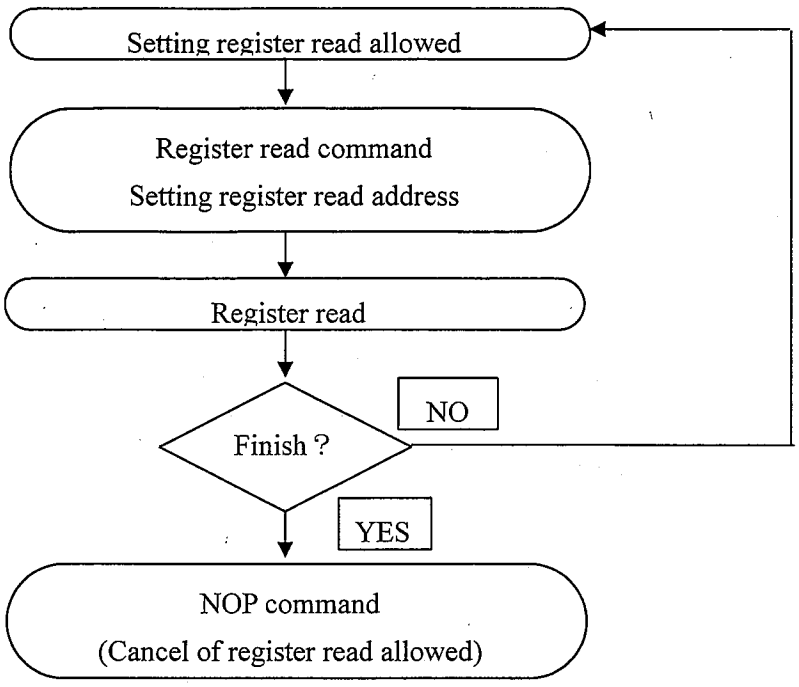
VCL*,VCW* is LCD Module Internal Resisters(Volume Control)

ON/OFF / LPOW / SLEEP / REV="1": Display On / Low Power Enable / Sleep Enable / Display Invert

ON/OFF / LPOW / SLEEP / REV="0": Display Off / Low Power Disable / Sleep Disable / Display Normal

ϕ mark is "Don't care"

The following sequence must be traced when executing register read.



※After executing register read, corresponded NOP command must be executed, in order to cancel register read allowed. REGRDEN bit becomes "0" by executing NOP command.

8-19. Read ID

Read ID1

Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
DA	0	1	1	0	1	1	0	1	0	Command byte
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Read dummy data
	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1 data

ID1 is the code defined as Module manufacturer code.(Fix)
ID1:{ID17,ID16,ID15,ID14,ID13,ID12,ID11,ID10}=1000 0011b=83H

Read ID2

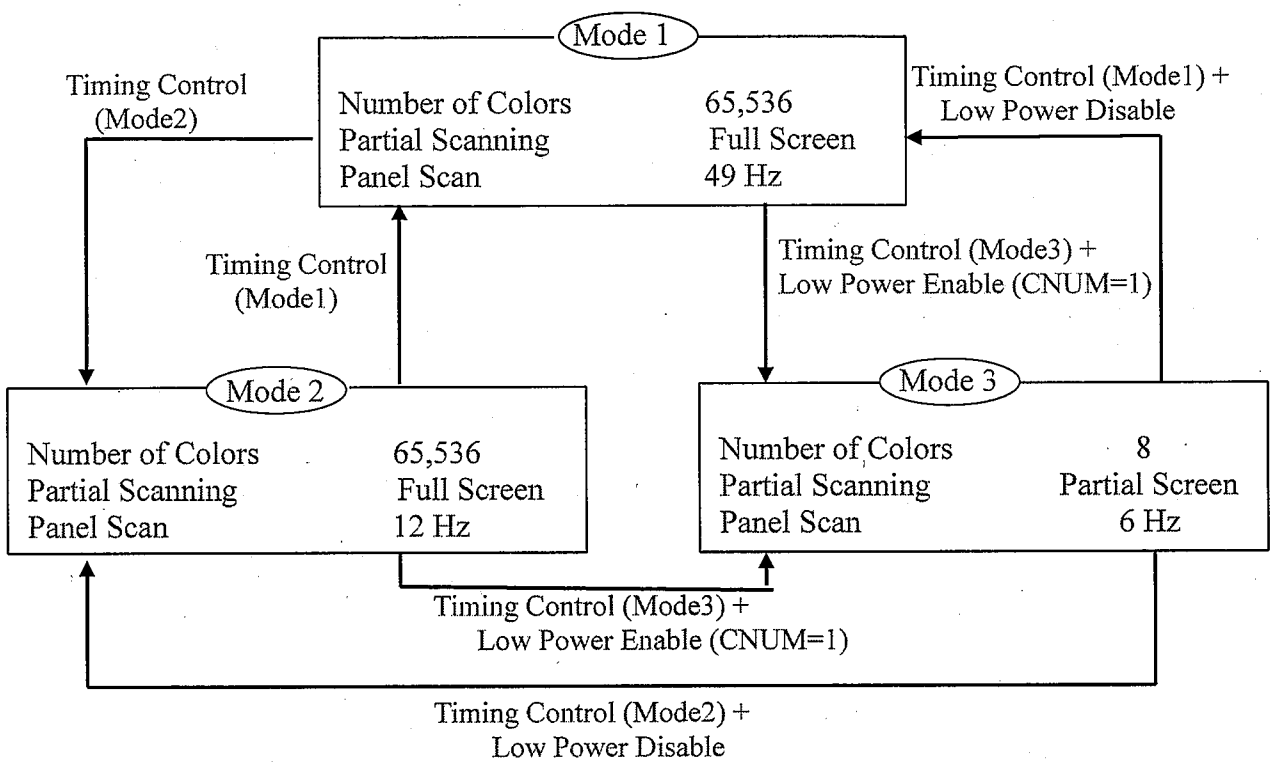
Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
DB	0	1	1	0	1	1	0	1	1	Command byte
	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Read dummy data
	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2 data

ID2 is the code defined as Driver manufacturer & Version number.
(ID27 is fixed, Driver manufacturer's bits use ID26,25,24, Version number use ID23,22,21,20)
Example of ID2
Driver manufacturer 1 => ID2=1000 0000b~1000 1111b=80H~8FH
Driver manufacturer 2 => ID2=1001 0000b~1001 1111b =90H~9FH
Driver manufacturer 3 => ID2=1010 0000b~1010 1111b =A0H~AFH

Records of Driver manufacturer & Version number.

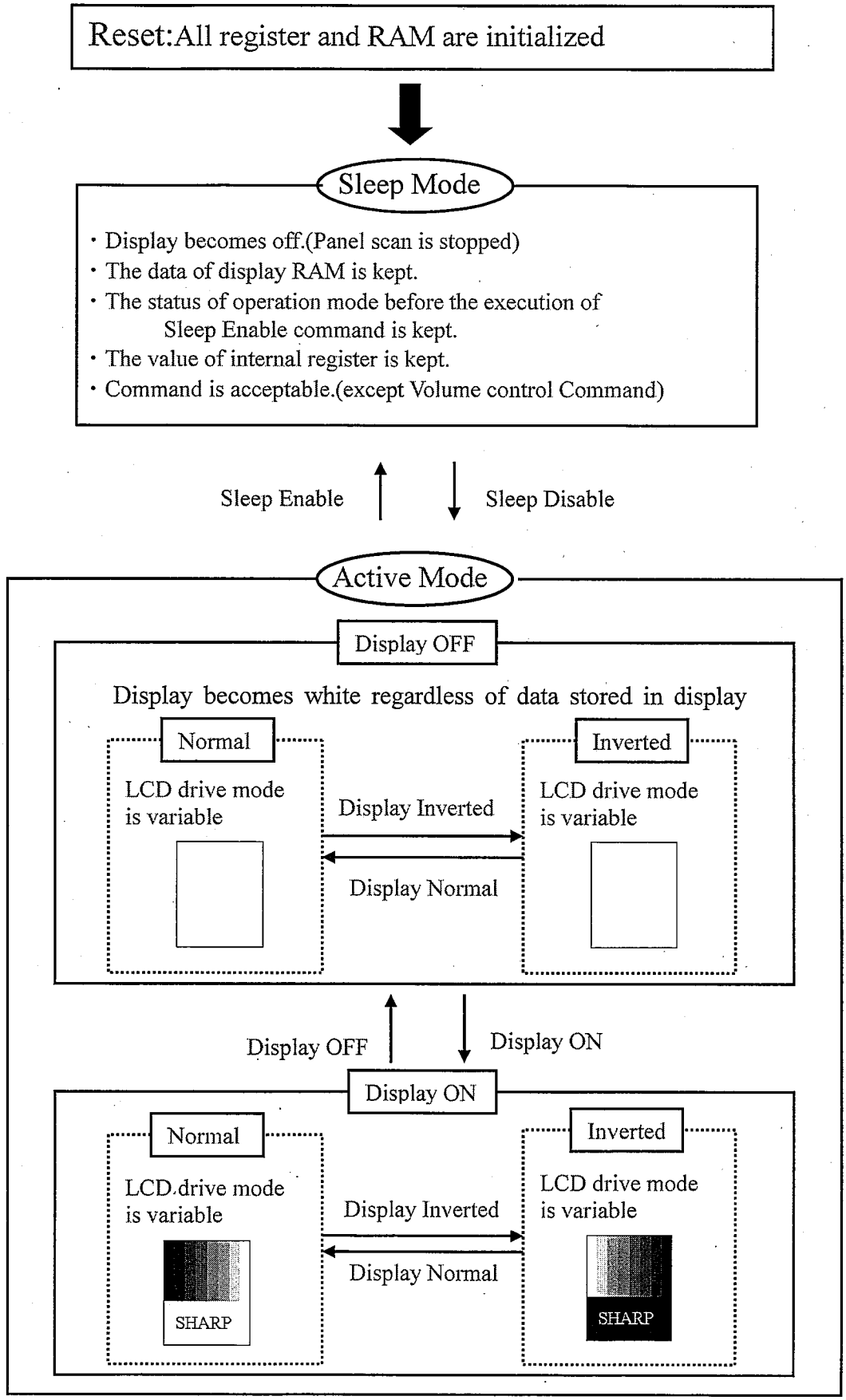
ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	HEX	Description
1	0	0	0	0	0	0	0	80H	Current Version

8-20. LCD Drive Mode Chart



When Timing Control (Mode3) command is executed without Low Power Enable(CNUM=1) command, フリッカ等が発生する可能性があり the display image quality of the LCD module is not assured.

8-21 Module Status Chart



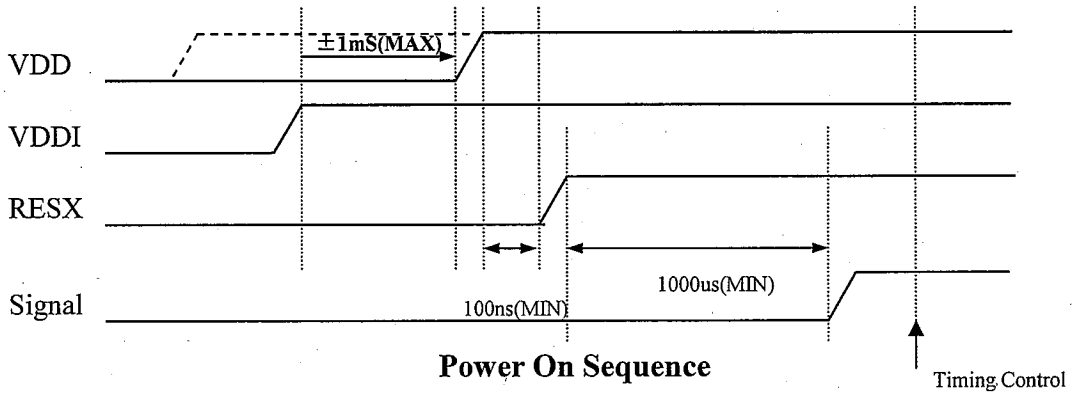
Power ON, Off shall be referred to the next paragraph (9.Power Sequence & Command Flowing).

9. Power Sequence & Command Flowing

9-1. Power ON

9-1-1. Initial configuration

VDDI, VDD power ON with RESX="L"
↓
Power will be stable
↓
Release RESX
↓
----- Setting Display Timing Control -----
Send **Timing Control** command (*)
Set parameters for Active Full Display Mode
↓
WAIT (>**30** ms)
↓
Send **Pixel Format** command
↓
Send **Sleep Disable** command
↓
WAIT (>**200** ms)
↓
End of initial configuration



Power On Sequence

(*) Since initial value of Timing control command cannot operate LCD correctly, be sure to execute mode setting at any of mode1, 2, or 3.

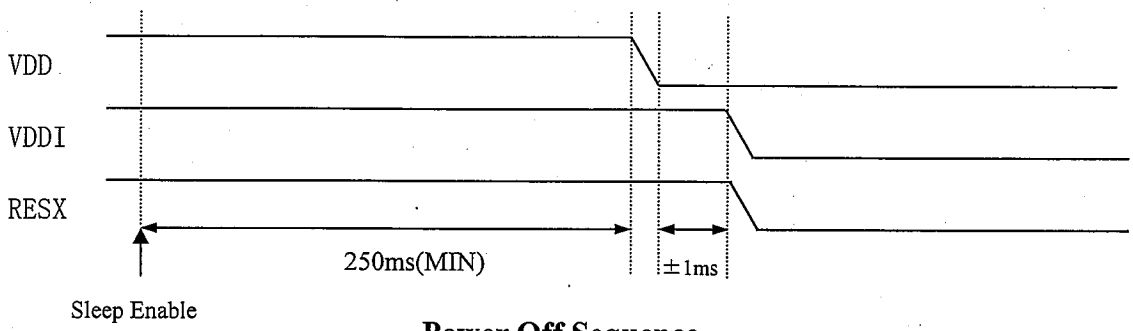
9-1-2. Data Display

End of initial configuration
↓
----- Setting Display Data writing for Full display -----
Send **Column Address** Command
Set Start column address
Set End column address
Send **Page Address** Command
Set Start Page address
Set End Page address
Send **Write RAM** Command
Set Display Data
(Memory is Cleared by writing data)
↓
----- Setting Display Control Command -----
Send **Display Normal** Command
Send **Display On** Command
↓
Data Display

9-2. Power OFF

Active Full Display Mode
↓
[Send **Display Off** Command]
Send **Sleep Enable** Command(*)
↓
WAIT (**>250 ms**)
↓
Power off (VDD→VDDI=±1ms)

[ ] can be omitted.



Power Off Sequence

(*) In case of Power off without executing Sleep Enable, the diplay image remains as afterimage.

9-3. Partial Display

9-3-1. Full display 65,536 colors → Partial display 8 colors

Full display (65,536 colors)
↓
LED-OFF (Active Full Display → Partial display 8 colors)
↓
----- Setting Display Timing Control -----
Send **Timing Control** command
Set parameters for Partial display 8 colors Mode
↓
WAIT (>**30** ms)
↓
----- Setting Low Power Enable -----
Send **Low Power Enable** Command
Set Start page address
Set End page address
Set 8 colors (CNUM=1)
↓
Partial display 8 colors

Power consumption can be reduced by decreasing panel scan rate by Timing Control command.
Power consumption can be reduced by partial mode by Low Power Enable command.
Furthermore, Power consumption can be reduced by 8 color mode because internal gray scale circuit is stopped.

9-3-2. Partial display 8 colors → Full display 65,536 colors

Partial display 8 colors
↓
----- Setting Display Timing Control -----
Send **Timing Control** command
Set parameters for Active Full Display Mode
↓
WAIT (>**30** ms)
↓
----- Setting Low Power Disable -----
Send **Low Power Disable** Command
↓
[**LED-ON**]
↓
Full display (65,536 colors)

[ ] can be omitted.

9-4. Changing Scan Mode

9-4-1. Active Full Display Mode → Still Full Display Mode

Active Full display Mode (65,536 colors)
↓
LED-OFF
↓
----- Setting Display Timing Control -----
Send **Timing Control** command
Set parameters for Still Full Display Mode
↓
WAIT (>**30**ms)
↓
Still Full display Mode (65,536 colors)

9-4-2. Still Full Display Mode → Active Full Display Mode

Still Full display Mode (65,536 colors)
↓
----- Setting Display Timing Control -----
Send **Timing Control** command
Set parameters for Active Full Display Mode
↓
WAIT (>**30**ms)
↓
[**LED-ON**]
↓
Active Full display Mode (65,536 colors)

[ ] can be omitted.

10. Optical Characteristics

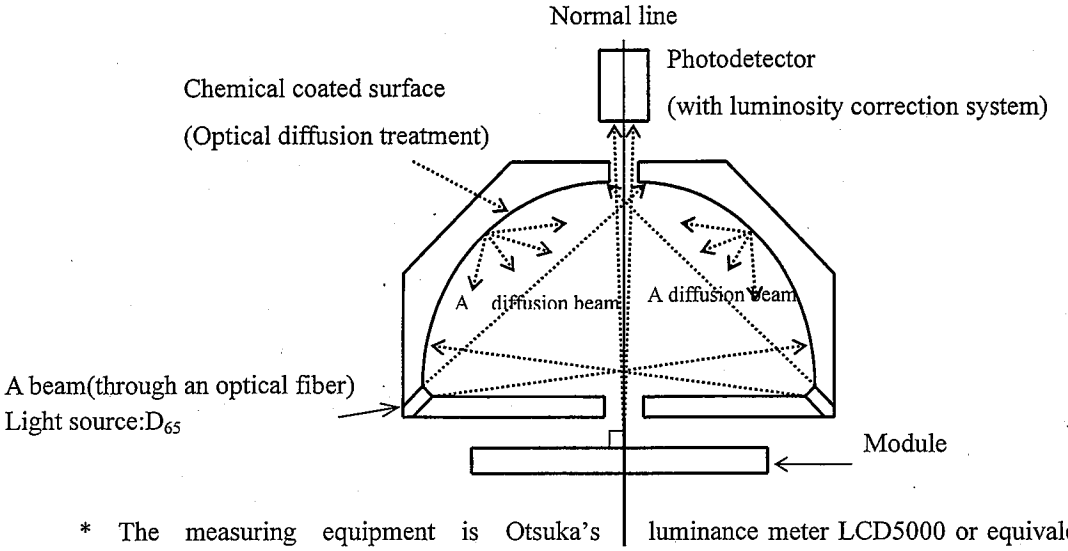
10-1. Optical Characteristics

Main viewing direction of this module is 6 o'clock.
(Main viewing direction: The direction of less reverse image.)
The optical characteristics in details are shown in the below table.

Table 10-1 Ta=25°C

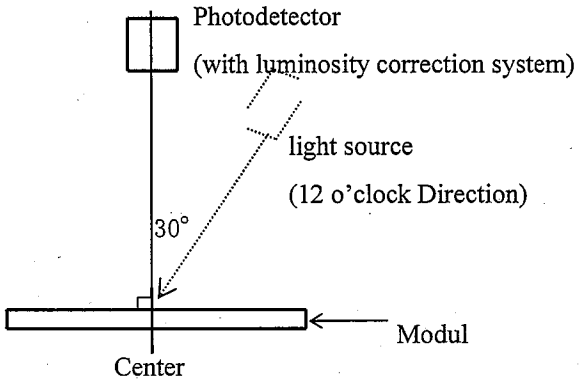
Parameter	Method*	Symbol	Min	Typ	Max	Unit	Remark
Reflective mode (backlight off)							
Reflection ratio	(I)	R_1	8.5	12.6		%	[Note 8-2]
	(II)	R_2	10.7	15.5		%	
White chromaticity	(I)	*Wx*	0.270	0.310	0.350	—	
		Wy	0.305	0.345	0.385	—	
Red chromaticity	(I)	*Rx*	0.375	0.425		—	
		Ry		0.330	0.380	—	
Green chromaticity	(I)	*Gx*		0.310	0.360		
		Gy	0.360	0.410			
Blue chromaticity	(I)	*Bx*		0.185	0.235		
		By		0.255	0.305		
Contrast ratio	(I)	CR ($\theta = 0$)	8	15		—	[Note 8-3]
	(II)	CR ($\theta = 0$)	10	20		—	[Note 8-3]
Viewing angle range (CR≥2)	(I)	θ_{21}, θ_{22}, θ_{11}, θ_{12}	30	45		degree	[Note 8-1]
Response time	(I)	$\tau_r + \tau_d$		30	60	ms	[Note 8-4]
Transmissive mode (backlight on)							
Brightness(Center point)	(III)	*Lc*	60	70		cd/m^2	[Note 8-5,6]
Brightness(The other 8Points)	(III)	*Lm*	50			cd/m^2	[Note 8-5,6]
Brightness uniformity	(III)	δ_L		1.2	1.3		[Note 8-5,6]
White chromaticity	(III)	*Wx*	0.257	0.297	0.337	—	
		Wy	0.286	0.326	0.366	—	
Red chromaticity	(III)	*Rx*	0.540	0.580		—	
		Ry		0.343	0.383	—	
Green chromaticity	(III)	*Gx*		0.310	0.350	—	
		Gy	0.468	0.508		—	
Blue chromaticity	(III)	*Bx*		0.136	0.176	—	
		By		0.165	0.215	—	
Contrast ratio	(III)	CR ($\theta = 0$)	80	120		—	[Note 8-3]
Viewing angle range (CR≥2)	(III)	θ_{21}, θ_{22}, θ_{11}, θ_{12}	30	45		degree	[Note 8-1]
Response time	(III)	$\tau r + \tau d$		50	90	ms	[Note 8-4]

* The methods for measuring the above characteristics are shown in the following figures.



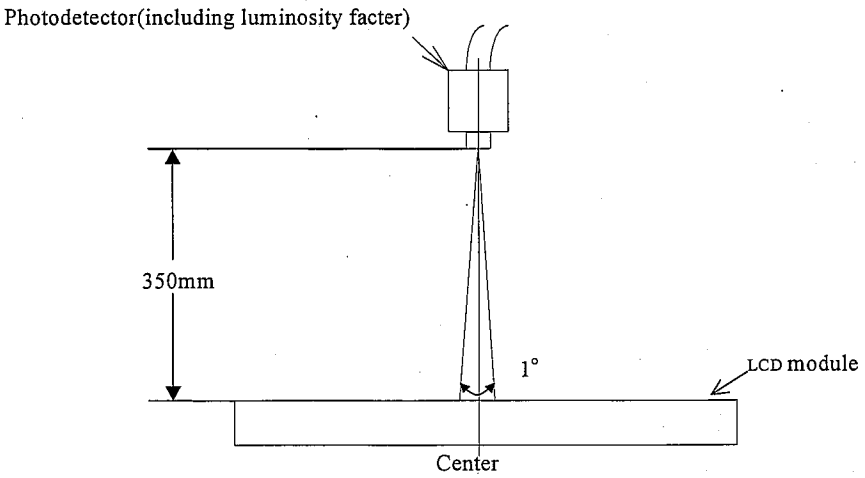
* The measuring equipment is Otsuka's luminance meter LCD5000 or equivalent. (With the diffusion reflection unit.)

Fig. 9 The method for measuring optical characteristics (I)



* The measuring instrument is LCD5000 or equivalent.

Fig. 10 The method for measuring optical characteristics (II)



* The measuring instrument is Topcon BM-5A or equivalent.

Fig. 11 The method for measuring optical characteristics (III)

[Note 8-1] Viewing angles are defined as follows:

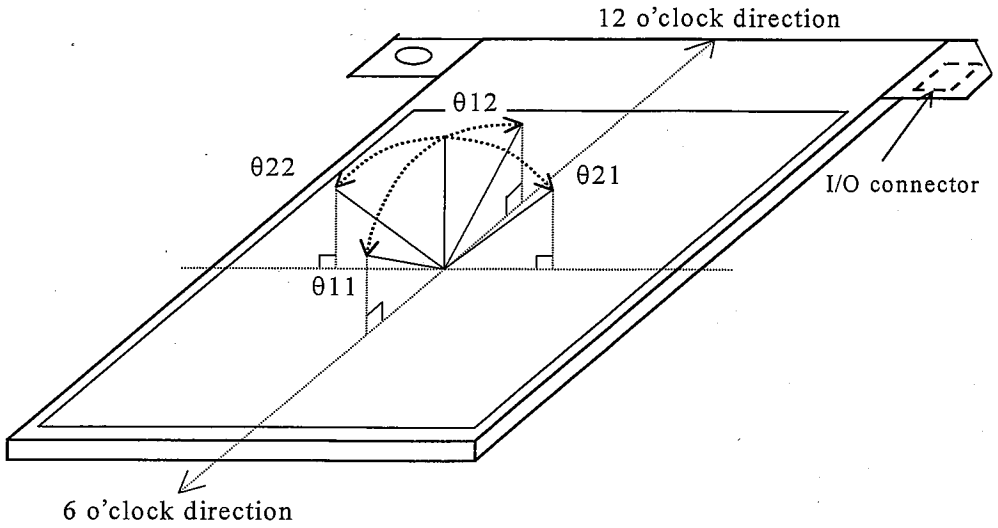


Fig. 12 Viewing angles

[Note 8-2] Definition of reflection ratio

$$\text{Reflection ratio} = \frac{\text{Brightness of glass panel, white image displayed}}{\text{Brightness of white standard board (barium sulfate)}}$$

[Note 8-3] Definition of contrast ratio:

$$\text{Contrast ratio} = \frac{\text{Brightness of the brightest white}}{\text{Brightness of the darkest black}}$$

[Note 8-4] Definition of response time:

Response time is defined as transient time when white image turns into black or otherwise as shown below.

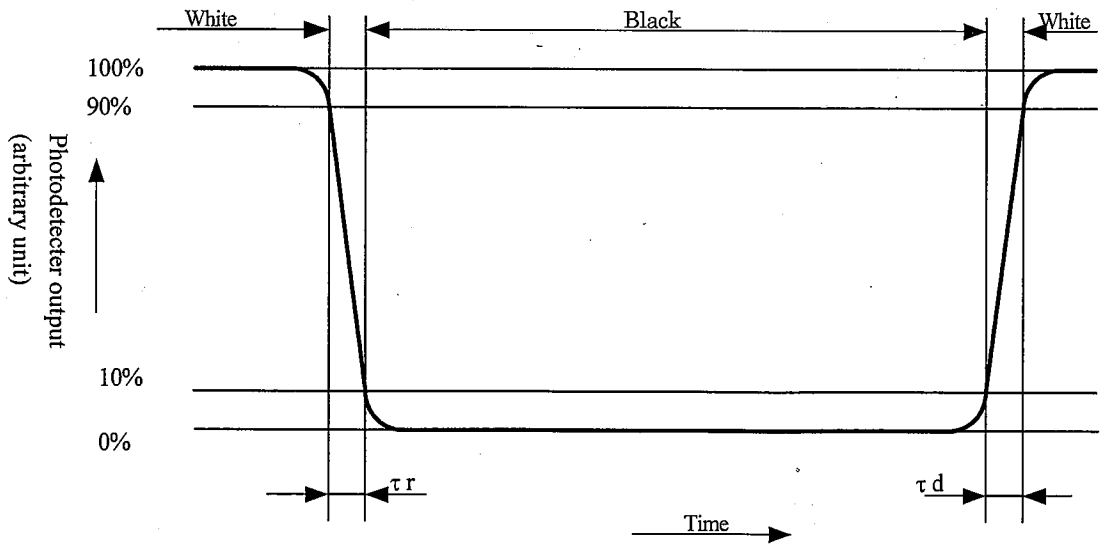


Fig. 13 Response time

[Note 8-5] Measured under condition that the total LED current is 15 mA.

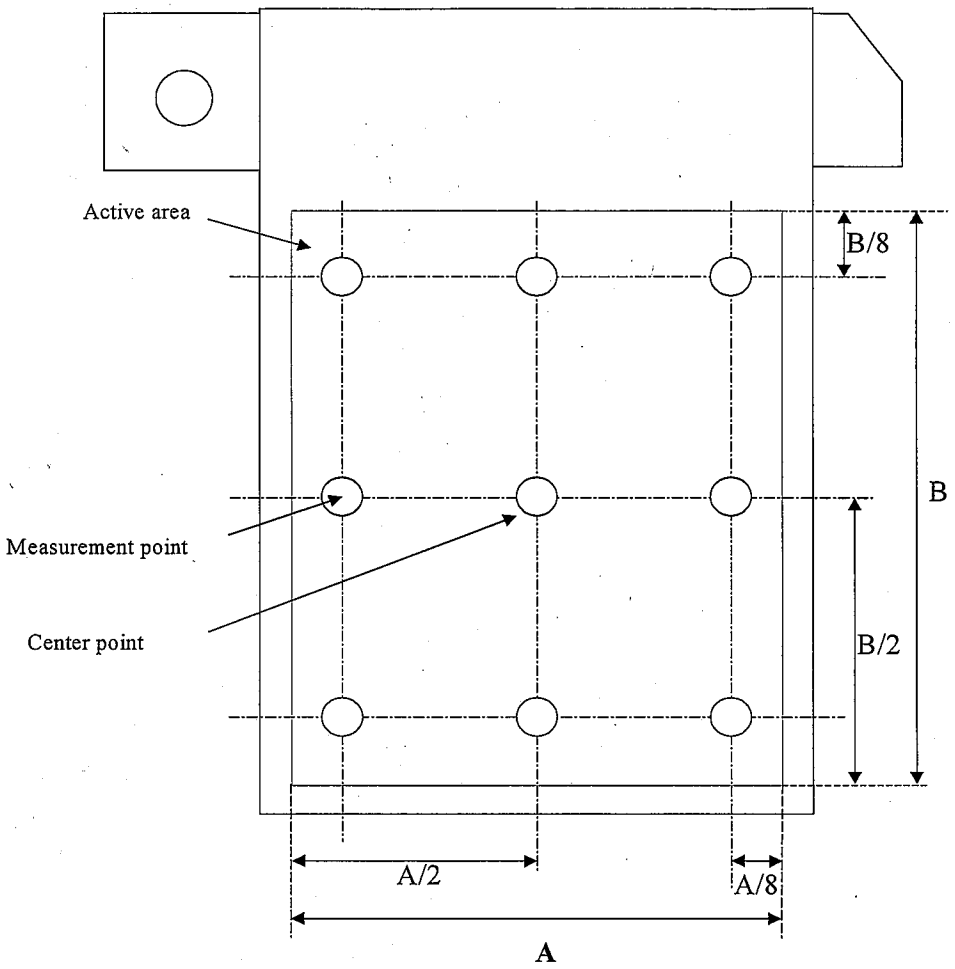
[Note 8-6] Definition of Brightness uniformity and Brightness(Lc,Lm)

$$\delta_L = \frac{\text{Maximum Brightness of the 9 measurement points of the glass panel}}{\text{Minimum Brightness of the 9 measurement points of the glass panel}}$$

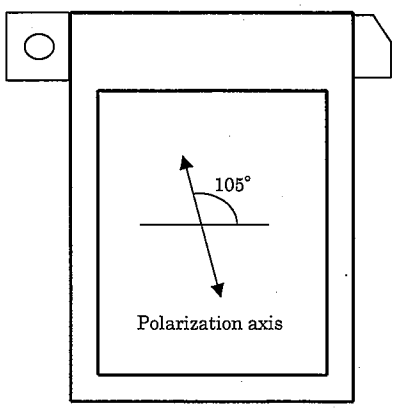
Lc=Brightness of the center point of the glass panel

Lm=Minimum Brightness of the 9 measurement points of the glass panel

The 9 measurement points are shown below, which are represented by circles.



[Note] Polarization axis of the front side of polarizer is shown below.



【Reference】

10-2. Temperature Characteristic of Optical Performance

Optical characteristic Characteristic of LCD module are affected by temperature change. Typical example of temperature characteristics are shown below.

10-2-1. Contrast ratio

Peak contrast ratio decreases due to liquid crystal material characteristics influence at high temperature, or shortage of charge by the TFT characteristics at low temperature. Max contrast angle changes from 12 o'clock to 6 o'clock, and due to ambient temperature change from low to high. Contrast at low or high temperature changes by these factors as the followings.

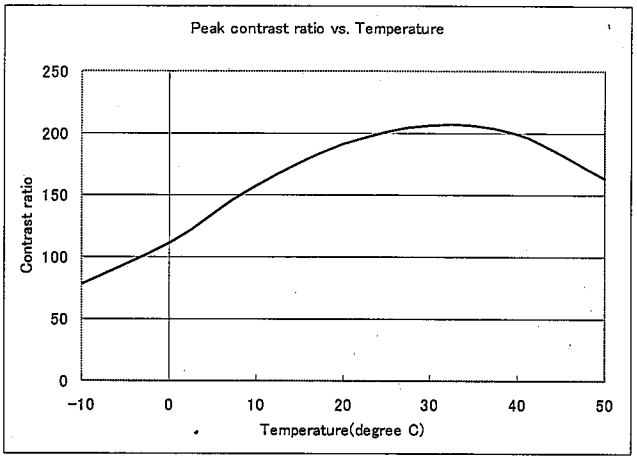


fig1)Peak Contrast ratio vs Temperature (Transmissive mode)

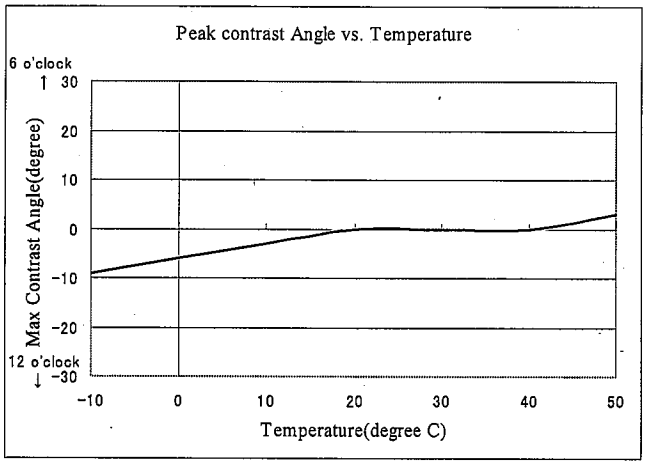


fig2)Max contrast angle vs Temperature (Transmissive mode)

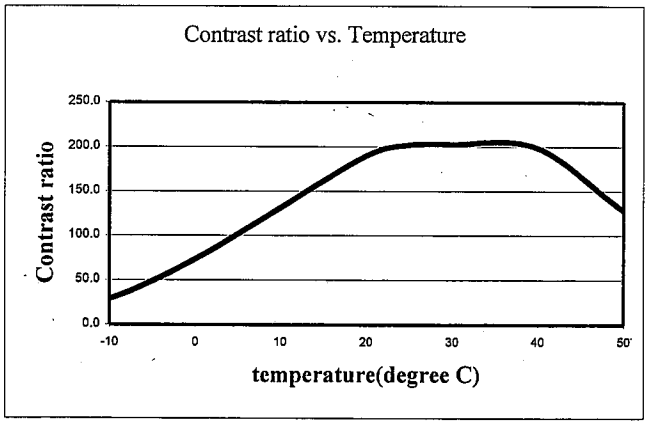


fig3)Temperature Characteristics of Contrast (Transmissive mode)

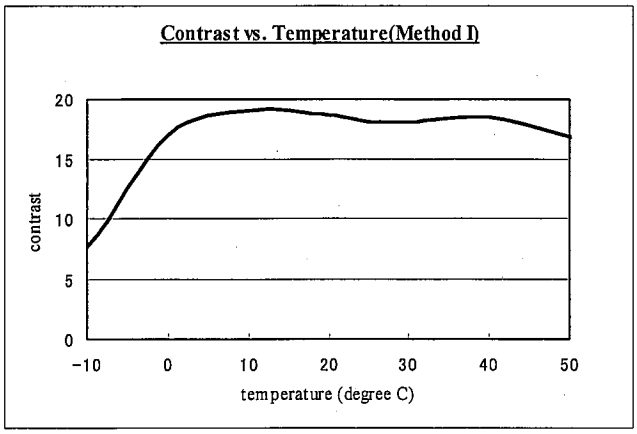


fig4)Contrast vs Temperature
(Reflective mode :method I)

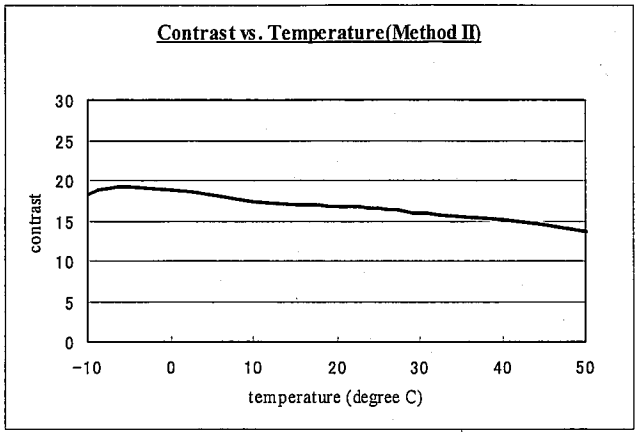


fig5)Contrast vs Temperature
(Reflective mode :method II)

10-2-2. Response time

Response time becomes slower in low temperature by liquid crystal characteristics.

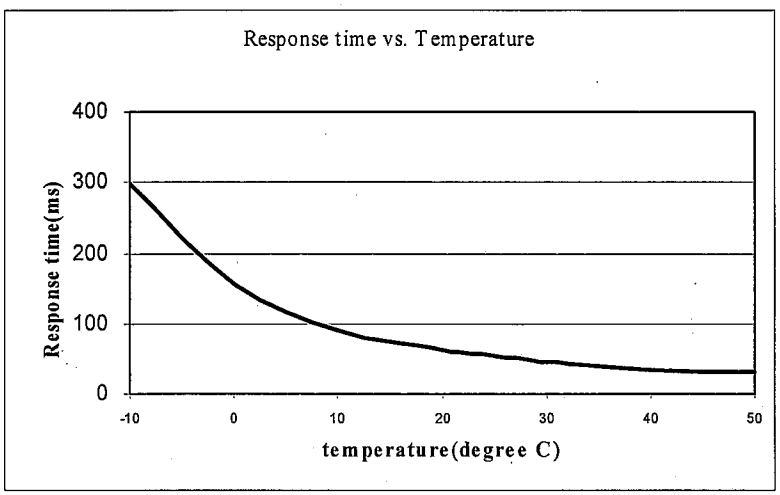


fig6)Response time vs Temperature (Transmissive mode)

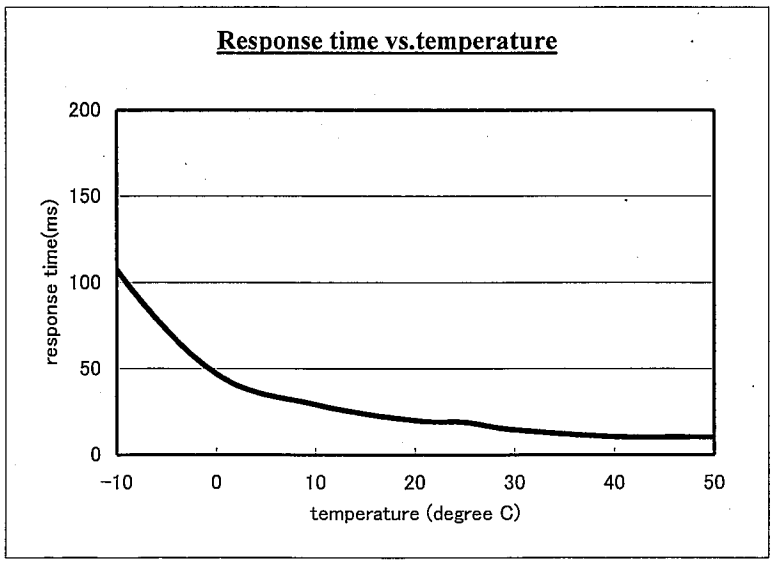


fig7)Response time vs Temperature (Reflective mode)

10-2-3. Color chromaticity

According to the drop of contrast, influence of smaller color reproduction range and temperature characteristics of liquid crystal spectral characteristic make R,G,B,W chromaticity shift.
(Higher temperature makes a shift to blue direction, and lower temperature makes a shift to yellow direction)
Temperature characteristics of LED make a shift to blue direction at higher temperature and to yellow at lower temperature,as well.

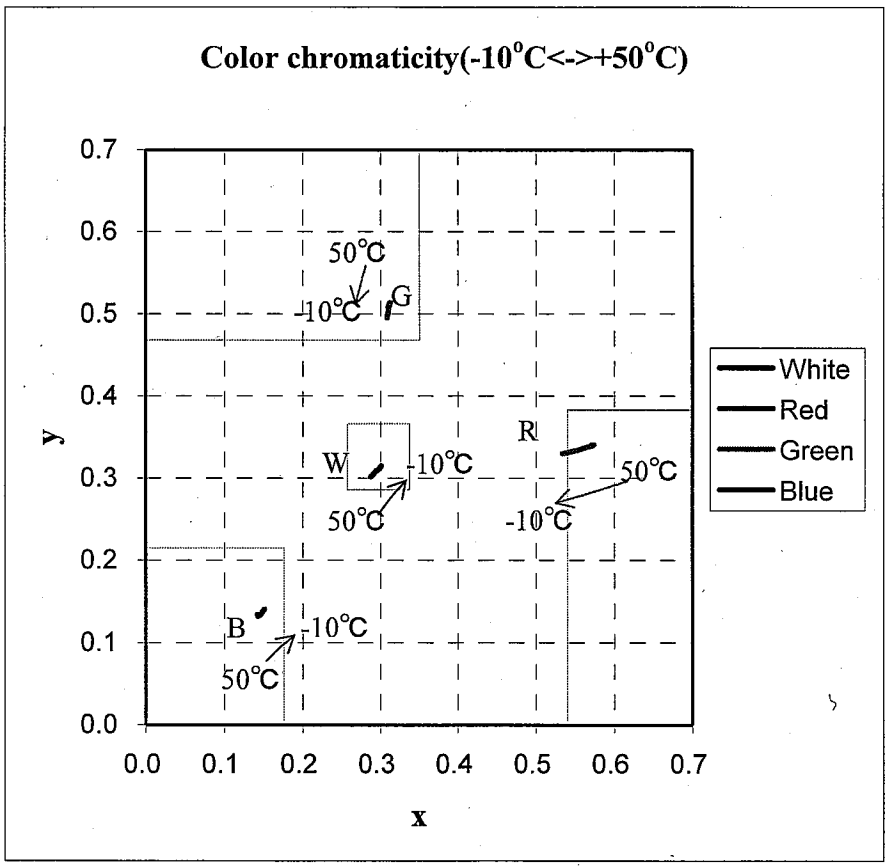


fig8)Temperature Characteristics of Color chromaticity (Transmissive mode)

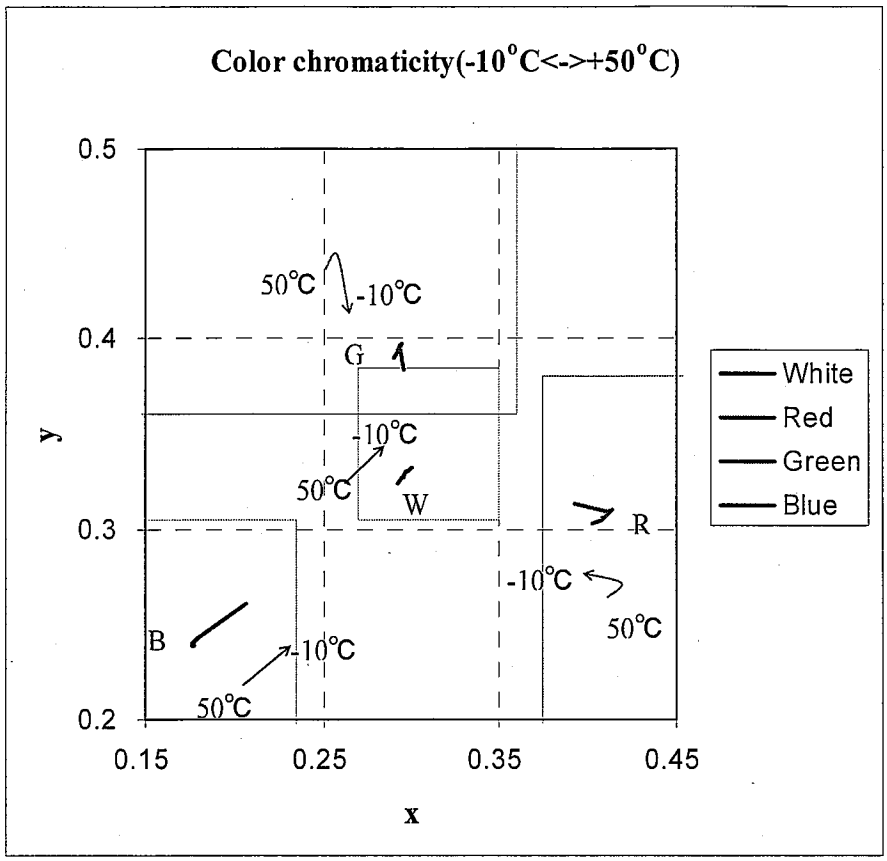


fig9)Temperature Characteristics of Color chromaticity(Reflective mode)

11. Display Quality

The display quality of the color TFT-LCD module shall be in compliance with the newest Incoming Inspection Standard.

12. Handling Precautions

(1) Make sure of turning off the power supplies before connecting or disconnecting the LCD module.
(2) Handle with care. Never hold FPC and pick up. Do not twist the FPC toward the display surface.
(3) Install the product not to be suffered from stress.
(4) As an electrostatic sensitive device, take care of grounding.
(5) Ultraviolet rays may damage liquid crystal. Do not leave it in direct sunlight for many hours.
(6) If the glass should be broken, keep away the contained liquid crystal from mouth.
(7) Since the front polarizer is easily damaged, pay an attention not to scratch it.
(8) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
(9) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
(10) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

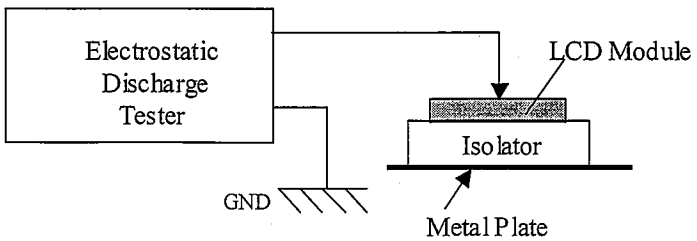
13. Reliability Test Conditions

Table 11

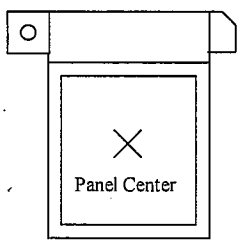
Item	Parameter	Requirement	Duration	Acceptable criteria
Climatic	Cold (Storage)	–40°C Power off	16h Recovery time 2h at room temp	Normal performance after recovery time
	Cold (Operational)	–30°C	16h	Normal performance
	Dry heat (Storage)	85°C Power off	16h Recovery time 2h at room temp	Normal performance after recovery time
	Dry heat (Operational)	70°C	16h + 2h	Normal performance
	Change of temperature	–40°C / 85°C Power off Change time < 3	5 cycles 1 cycle 2h + 2h Recovery time 2h at room temp	Normal performance: –30°C to +70°C Reduced performance: –40°C to +85°C
	Damp heat cyclic	+25°C / +55°C 90 to 100% RH	12h+12h 6 cycles Recovery time 2h	Normal performance after recovery time
	Solar radiation	1120 W/m^2 +55°C Power off	8h 16h dark 10 cycles	Normal performance
Mechanics	Vibration (Sinusoidal)	2-8Hz / 7.5 mm 8-200Hz / 19.6 m/s^2 Search for resonance	90 min at the worst resonance frequency	Normal performance
	Vibration (Random)	10-100Hz; 3m^3/s^2 100-500Hz; –3 dB/oct	3 × 1h (Three axes)	Normal performance
	Bump	Duration 6ms 245 m/s^2	3 × 1000	Normal performance
ESD	ESD (electrostatic discharge)	±2, 4, 8 kV contact ±4, 8, 10, 15 kV air C=150pF, R=330 Ω	> 10 + 10 discharges, Center on display	Normal performance ± 15 kV interrupted function, no permanent damage
	HBM	±2000V, C=100pF, R=1.5k Ω	1 time on each I/O terminals	Normal performance
	MM	±200V, C=200pF, R=0 Ω	1 time on each I/O terminals	Normal performance

※ Electrostatic Discharge Test Method & Test Point

Test Method



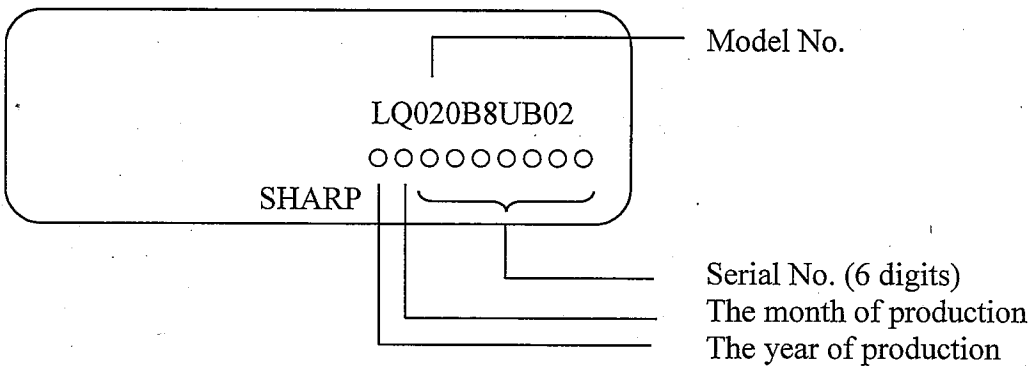
Test Point



14. Forwarding Form

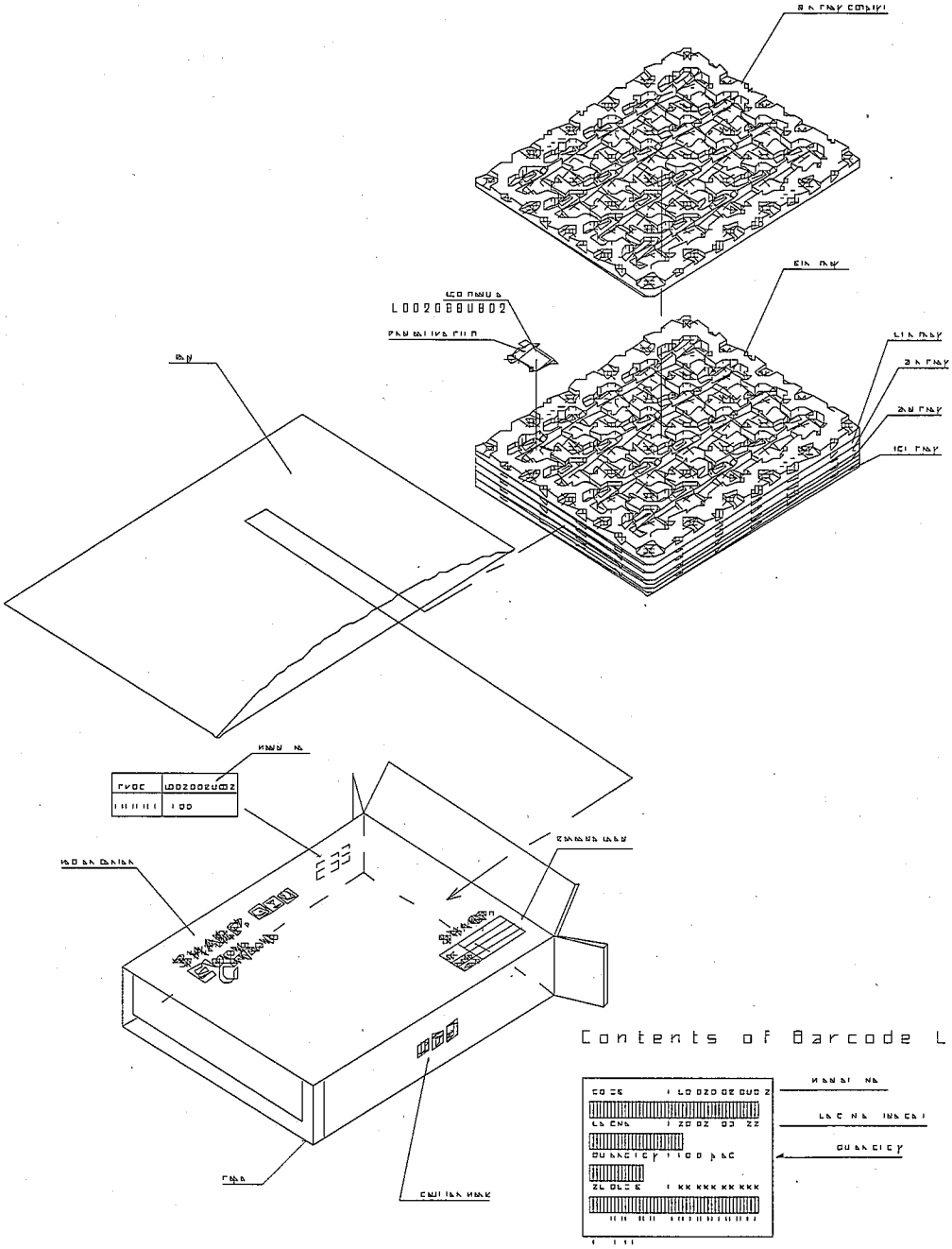
(1) Piling number of cartons: Max. 20 boxes
(2) Package quantity in one carton: 100 modules
(3) Carton Size: 503 mm x 408 mm x 88 mm
(4) Total mass of 1 carton filled with full modules: Max. 3.0kg
(5) Conditions for storage
Environment
Temperature: 0~40°C
Humidity: 60%RH or less (at 40°C)
No dew condensation at low temperature and high humidity
Atmosphere: Harmful gas, such as acid or alkali which bites electronic components and/or wires, must not be detected.
Period: 3 monthes
Opening of the package: In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.

(6) Indication of Lot number
The lot number is shown on the back side of module. The location is shown in Apendix1 (Outline Dimensions).



Back side of Module

(7) Packing Process



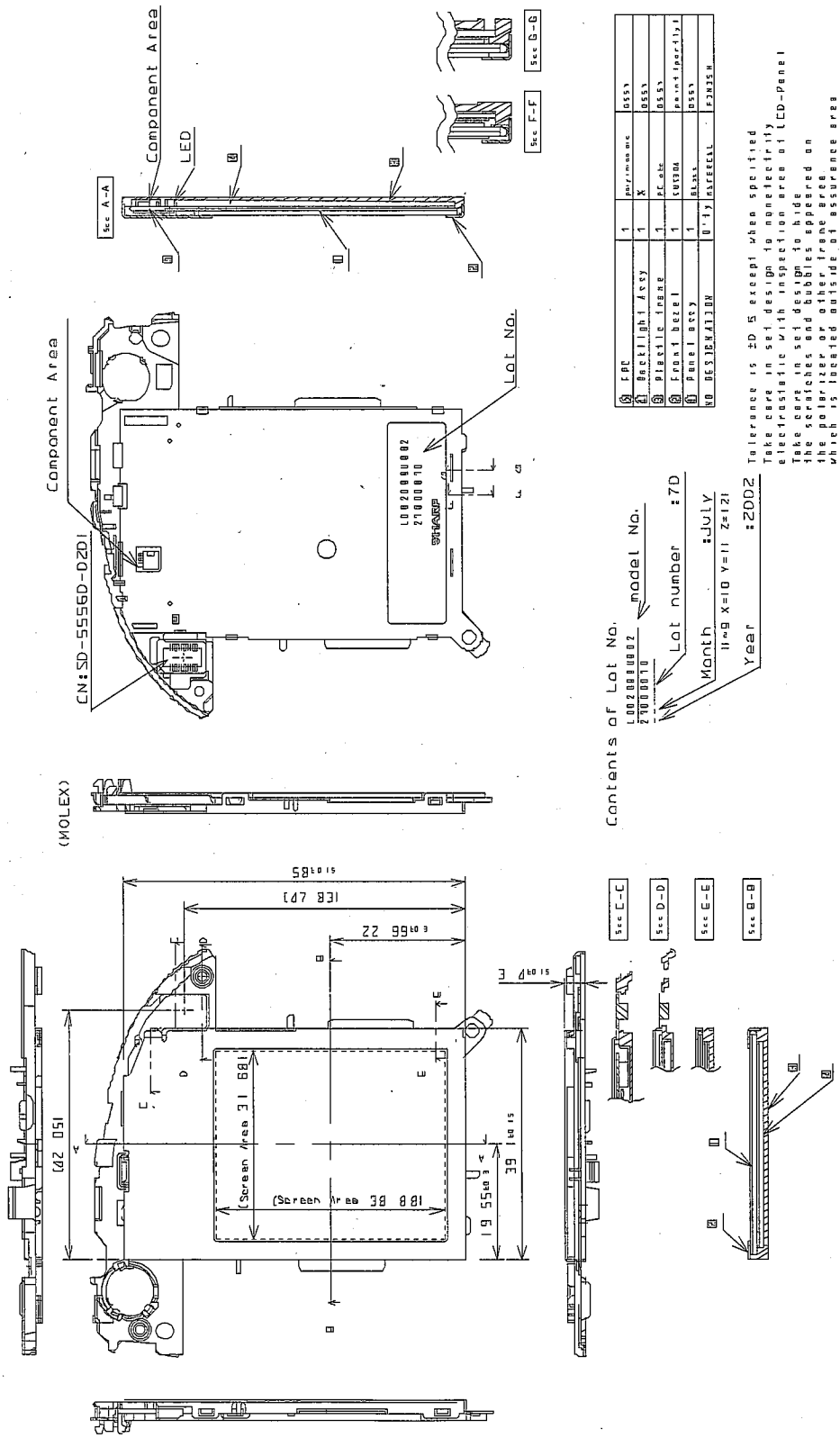
Contents of Barcode Label

15. Miscellaneous

1) Disassembling the module can cause permanent damage and should be strictly avoided.
2) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
3) If some problems arise about mentioned items in this document and other items, the user of the TFT-LCD module and Sharp will cooperate and make efforts to solve the problems with mutual respect and good will.
4) Since Volume control of module is adjusted to optimized value at the time of delivery from Sharp. Therefore, please do not change the adjusted value. It may cause a generation of flicker, or lower contrast, to be out of specification, in case that the initial adjusted value is changed.
Please refer to Appendix G for the detail.
5)Since this module has no fuse in power supply lines(VDDI, VDD), please make an appropriate design for power supply in the phone set.

Appendix

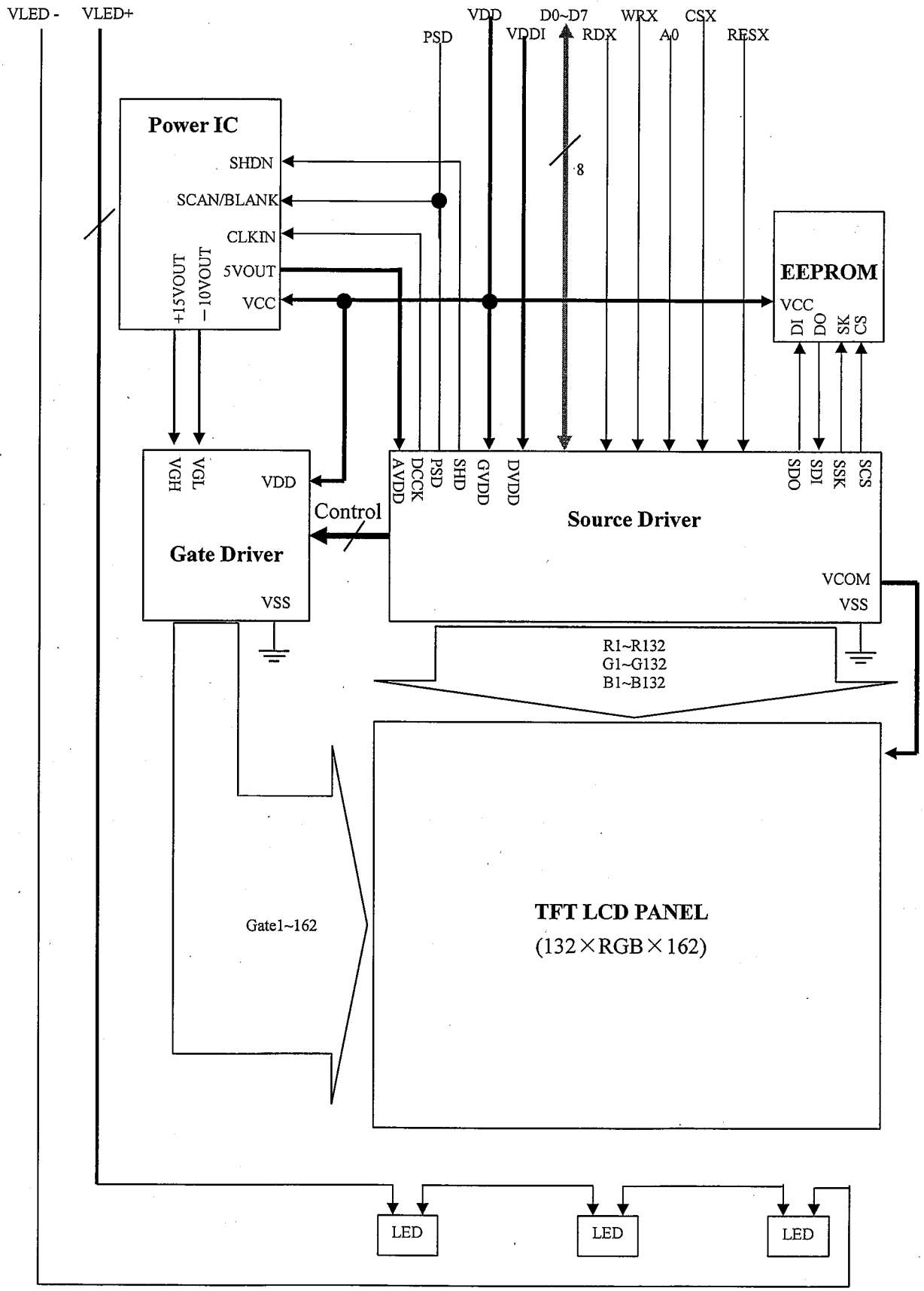
Appendix A : Outline Dimensions



Appendix B : LCD-Module Assy

Appendix C : Assignment of I/O Pin

Appendix D : System Block Diagram



Appendix E : FPC Circuit Diagram

Appendix F : Parts mounted on FPC Diagram

Appendix G : Volume control value and contrast, flicker

This module incorporates EEPROM, memorizing volume control value.
Contrast, flicker is changed when volume control value is changed.
Below is the explanation of unnecessity of changing volume control value after the shipment from Sharp.

Contrast adjustment function by manually changing volume control is only needed for STN LCD display, which cannot set optimized contrast in various usage condition, due to rapid Vth, as well as large temperature dependency of Vth.
On contrary, TFT LCD display has a slow V-T and stable characteristics against temperature change, so that extremely higher contrast ratio compared with STN is available, and no need to re-adjust the contrast once optimized.
In the meantime, DC level of counter-electrode voltage needs to be adjusted so that LC can be alternating driven correctly. This adjustment can achieve flicker to be minimized, and contrast to be optimized. This adjustment is done in LCD module before shipment from Sharp.